Charge Pump DC-DC Voltage Converter

CE7660

CE7660 is a charge pump dc-to-dc voltage converter using Si-gate CMOS technology and optimization design. It converters a +2.5V to +10V input to a corresponding -2.5V to -10V output using only two external capacitors, eliminating inductors and their associated cost, size and EMI. The on-board oscillator operates at a nominal frequency of 10KHz. Operation below 10 KHz (for lower supply current applications) is possible by connecting an external capacitor from OSC to ground.

Features

- Wide input voltage range: 2.5V~10V
- Efficient voltage conversion:99.9%
- Good power efficiency: 98%
- Low power supply: 50uA @5V input
- Easy to use: only two external capacitors required
- Compatible with RS232 negative power supply standard
- High ESD protection: up to 4KV
- No Dx diode needed for high voltage operation
- Package : SOP8, DIP8

Applications

- LCD Display Module
- Specially designed for LCD module
- Instrument product
- RS-232 Power supply
- Operation amplifier supply
- On board negative supply for dynamic RAMS

Pin Configuration



Pin Description

PIN Number	PIN NAME	FUNCTION
1	NC	No connection
2	CAP⁺	Connecting external capacitor(+) pin
3	GND	Ground pin
4	CAP ⁻	Connecting external capacitor(-) pin
5	Vout	Voltage output pin
6	LV	Low voltage selection pin
7	OSC	Connecting oscillation capacitor pin
8	VDD	Power supply pin

Block Diagram



Absolute Maximum Ratings

PARAM	ETER	SYMBOL	RATINGS	UNITS
Input vo	oltage	VIN	+13V	V
LV PIN inp	out voltage	V _{LX}	-0.3~(V ⁺ +0.3) (if V ⁺ <5.5V)	V
OSC PIN inp	out voltage	Vosc	(V ⁺ -5.5V)∼(V ⁺ +0.3V) (if V ⁺ >5.5V)	v
Output Short Dut ≤5.5	ration (Vsupply 5V)		œ	
ContinuousTotal Power	SOP8	Pd	470	mW
Dissipation (T _A ≤75℃)	DIP8	Pd	730	mW
Operating Ambie	nt Temperature	T _{Opr}	-40~+85	°C
Storage Ter	nperature	T _{stg}	-65~+150	°C
Soldering temper	rature and time	T _{solder}	260 ℃, 10 s	

Electrical Characteristics(VDD=5V,Cosc=0)

Symbol	Item	Conditions	Min	Тур	Мах	Unit
I+	Supply Current	R _L =∞	—	50	100	μA
VDD	Supply Voltage		2.5	—	10	V
Rout	Output Resistance	I _{OUT} =20mA T _A =25℃		60		Ω
Fosc	Oscillator Frequency	Pin 7 open	—	10	—	kHz
PEFF	Power Efficiency	RL=5k Ω	95	98	_	%
VOUTEFF	Voltage Conversion Efficiency	R _L =∞	98	99.9	_	%

Test Circuits



Type Characteristics

1. Vout VS lout:







Operation

CE7660 together with two external capacitors C1 $\$ C2 complement a voltage Inverter. Capacitor C1 is charged to a voltage V⁺, for the first half cycle when switches S1 and S3 are closed (while switches S2 and S4 are open during this half cycle); During the second half cycle of operation, switches S2 and S4 are closed, with S1 and S3 open, thereby shifting capacitor C2 negatively to -V⁺.



Charge Pump Voltage Converter operating process

Theoretical Power Efficiency Considerations

In theory, a capacitive charge pump can approach 100% efficiency if certain conditions are met:

- 1. The drive circuitry consumes no power.
- 2. The output switches have extremely low ON resistance and no offset when operation.
- 3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

Notes:

- 1. Supply voltage should not exceed maximum rating;
- 2. Do not short the output to VDD supply for voltages above 5.5V for extended periods;
- 3. Polarized capacitors should be connected as the figure above.

Typical Application



Above figure is the basic application circuit to provide a negative supply from -2.5V~ -10V while a positive supply from +2.5V ~ +10V is available. When VDD=+5V, the output resistance is about 60Ω ; The output voltage is -4.5V while the load current is 10mA.



CE7660 may be paralleled to reduce output resistance (see the above figure) Rout(Paralleled)=Rout/N



VDL O T NC VDE E T NC VDE -2 CAFT osc 🔂 osc 🗧 10ab -<u>2</u> CAF I LV (- 🗄 GND 1(0) - 🗄 GND LV ζ EVDE -I CAF Vout 打 <u>-</u> -**4** CAF Voat 5 CE7660 CE7660 Rub 10a)

CE7660 may be cascaded as shown above to produce larger negative output voltage (-10V). However, The output resistance is approximately double that of a single chip resistance. CE7660 may be cascaded as shown above to produce larger negative output voltage (-15V). However, The output resistance is approximately double that of a single chip resistance.



To increase the conversion efficiency, the oscillator frequency may be lowered by connecting a capacitor from pin 7 and pin 8 as shown above.



CE7660 may be applied to achieve positive voltage multiplication using the circuit shown in the above figure



In above figure, C1、C3 are the pump and reservoir capacitors respectively for the generation of the negative voltage; C2、C4 are the pump and reservoir capacitors respectively for the multiplied positive voltage. When +5V supply is provided, +9V and -5V can be generated.



In some noise-sensitive applications, it desirable to increase the may be oscillator frequency. This can be achieved by overdriving the oscillator from an external clock as shown in the above figure. The external clock output should connect a 1k Ω resistor to prevent device latch-up. Besides, the pump frequency will be half of the clock frequency because of the internal circuit.

Package Diomensions



Sumbal Dimensions In Millimeters Dimensions In Inches
Min Max Min Max
A 3. 710 4. 310 0. 146 0. 170
A1 0.510 0.020
A2 3.200 3.600 0.126 0.142
B 0.380 0.570 0.015 0.022
B1 1. 524 (BSC) 0. 060 (BSC)
C 0. 204 0. 360 0. 008 0. 014
D 9.000 9.400 0.354 0.370
E 6. 200 6. 600 0. 244 0. 260
E1 7. 320 7. 920 0. 288 0. 312
e 2. 540 (BSC) 0. 100 (BSC)
L 3.000 3.600 0.118 0.142
E2 8,400 9,000 0,331 0,354