■ INTRODUCTION:

The CE8310 is a high efficiency boost switching regulator designed for single cell lithium or two cells alkaline, NiMH, or NiCd battery powered applications. It generates an output voltage of up to 5.5V from an input voltage as low as 1.6V. Ideal for applications where space is limited, it switches at 1MHz, allowing the use of tiny, low cost and low profile external components, minimizes solution footprint. Its internal 3A, 100mΩ NMOS switch provides high efficiency even at heavy load, while the constant frequency, current mode architecture results in low, predictable output noise that is easy to filter. Internal frequency compensation is designed to accommodate ceramic output capacitors, further reducing noise.

■ FEATURES:

- 1MHz Switching Frequency
- Built-in 100mΩ N-CH Power MOSFET Switch
- PWM/PFM Auto Switching Maintains High Efficiency Overall Load Current Range
- Up to 90% Efficiency:
  Delivers 1A@5V from Single Li Cell
- Wide Input Voltage Range: 1.6V to 6.0V
- Wide Output Voltage Range: 2.8V to 6.0V
- Output Current: 1.2A@V_{IN}=3.0V
- 600mV Feedback Voltage
- Low Shutdown Current: 0.1μA(Typ.)
- Over-Current Protection
- Over-Thermal Protection
- Uses Small,Low Profile External Components
- Ceramic Capacitor Compatible

■ APPLICATIONS：

- Back-up Battery
- Solar Battery Charger
- Portable Applications Using Single Li+ Cel
- Bus Powered USB Hosts
- USB Hosts Without Native 5-V Supplies
- 3G/4G Wireless Routers
- Networking card powered from PCI or PCI-express slots
- Portable Audio Players
- Personal Medical Products

■ ORDER INFORMATION(1)

Operating free air temperature range	Output Voltage	Package	Device No.
-40~+85℃	Adjustable	SOT-23-5	CE8310CM
-40~+85℃	5.1V	SOT-23-5	CE8310C51M
-40~+85℃	Adjustable	SOT-23-6	CE8310CE
-40~+85℃	Adjustable	SOP8-PP	CE8310CES
-40~+85℃	Adjustable	DFN3X3-10	CE8310CFC10

(1) Contact Chipower to check availability of other fixed output voltage versions.

■ TYPICAL APPLICATION CIRCUIT

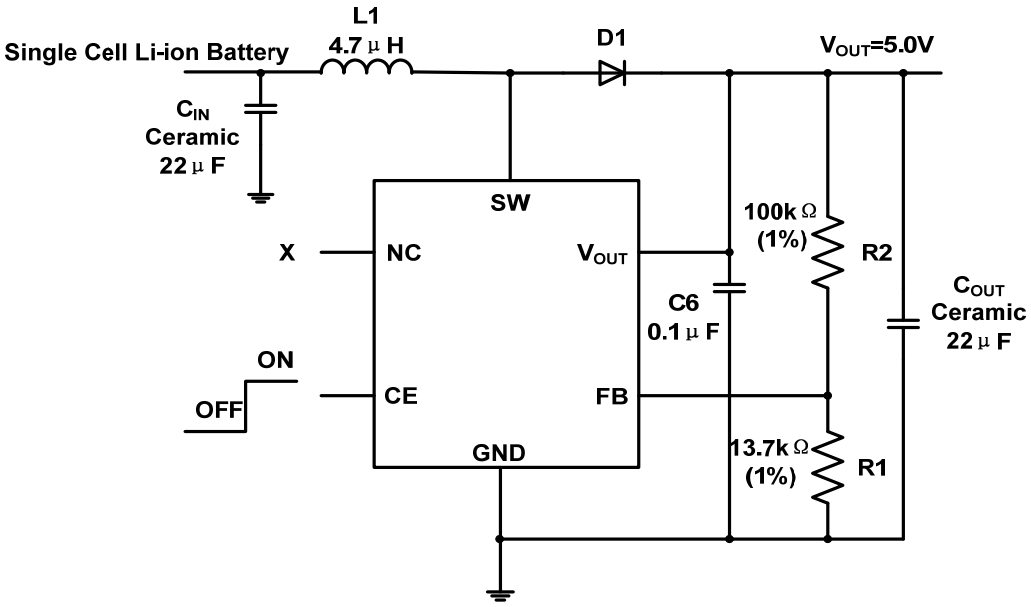
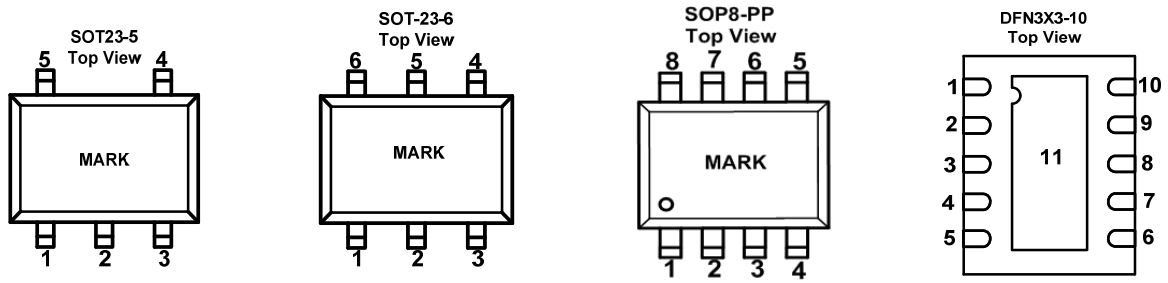


Figure 1 Standard Application Circuit

■ PIN CONFIGURATION:



SOT-23-5

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SW	I	**Switch Pin**. Connect inductor between SW and IN. A Schottky diode is connected between SW and V_{OUT}. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.
2	GND	P	**Signal and Power Ground**. Connect GND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors.. This pin should be connected to a continuous PCB ground for high-current power converter as close as to the device by several vias directly under the CE8310CM or CE8310C50M for electrical contact and rated thermal performance. It dissipates the heat from the IC.
3	FB/NC	I	**Feedback Input / No Connect (for fixed Voltage)**. Feedback Input to the gm Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 3.0V to 5.5V by: V_{OUT}=0.6V•[1+(R2/R1)] The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor, SW、inductor and Schottky diode switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.
4	CE	I	**Chip Enable**. CE = High: Normal free running operation CE = Low: Shutdown, quiescent current < 1μA. Typically, CE should be connected to IN through a 1M pull-up resistor.
5	V_{OUT}	I	**Chip Supply Voltage & Output Voltage Sense Input**. The V_{OUT} pin should be connected to the negative terminal of the schottky diode and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{OUT} pin, and the CE8310CE GND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{OUT} pin and the GND pin.

(1) I = input; O = output; P = power

SOT-23-6

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SW	I	**Switch Pin**. Connect inductor between SW and IN. A Schottky diode is connected between SW and V_{OUT}. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.
2	GND	P	**Signal and Power Ground**. Connect GND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors.. This pin should be connected to a continuous PCB ground for high-current power converter as close as to the device by several vias directly under the CE8310CE for electrical contact and rated thermal performance. It dissipates the heat from the IC.
3	FB/NC	I	**Feedback Input / No Connect (for fixed Voltage)**. Feedback Input to the gm Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 3.0V to 5.5V by: V_{OUT}=0.6V•[1+(R2/R1)] The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor, SW、inductor and Schottky diode switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.
4	CE	I	**Chip Enable**. CE = High: Normal free running operation CE = Low: Shutdown, quiescent current < 1μA. Typically, CE should be connected to IN through a 1M pull-up resistor.
5	V_{OUT}	I	**Chip Supply Voltage & Output Voltage Sense Input**. The V_{OUT} pin should be connected to the negative terminal of the schottky diode and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{OUT} pin, and the CE8310CE GND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{OUT} pin and the GND pin.
6	NC		**Not Connect**.

(2) I = input; O = output; P = power

SOP8-PP

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	AGND	I	**Analog Ground**. The analog ground ties to all of the noise sensitive signals. Provide a clean ground for the analog control circuitry and should not be in the path of large currents. Return for output voltage set resistor divider.
2	FB	I	**Feedback Input**. Feedback Input to the gm Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 3.0V to 5.5V by: V_{OUT}=0.6V•[1+(R2/R1)] The feedback networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the AGND pin. If no analog ground plane is available, then the ground connection of the feedback network must tie directly to the AGND pin. Connecting the network to the PGND can inject noise into the system and effect performance. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor, SW、inductor and Schottky diode switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.
3	NC		**No Connect**.
4	SW	I	**Switch Pin**. Connect inductor between SW and IN. A Schottky diode is connected between SW and V_{OUT}. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.
5	PGND	P	**Power Ground**. Ground connection for high-current power converter node. High current return for the low-side driver and power N-MOSFET. Connect PGND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors. Only connect to AGND through the Exposed Pad underneath the IC.
6	V_{OUT}	I	**Chip Supply Voltage & Output Voltage Sense Input**. The V_{OUT} pin should be connected to the negative terminal of the schottky diode and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{OUT} pin, and the CE8310CES ground pins. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{OUT} pin and the AGND pin.
7	NC		**No Connect**.
8	CE	I	**Chip Enable**. CE = High: Normal free running operation CE = Low: Shutdown, quiescent current < 1μA. Typically, CE should be connected to IN through a 1M pull-up resistor.
9	EP	P	**Exposed Paddle (bottom)**. Provide a short direct PCB path between exposed pad and negative terminals of the input and output capacitor(s). This pin should be connected to a continuous PCB ground for high-current power converter as close as to the device by several vias directly under the CE8310CES for electrical contact and rated thermal performance. It dissipates the heat from the IC.

(3) I = input; O = output; P = power

DFN3X3-10

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	NC		**No Connect**.
2	FB	I	**Feedback Input**. Feedback Input to the gm Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 3.0V to 5.5V by: V_{OUT} =0.6V•[1+(R2/R1)] The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor, SW、inductor and Schottky diode switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.
3	NC		**No Connect**.
4/5	SW	I	**Switch Pin**. Connect inductor between SW and IN. A Schottky diode is connected between SW and V_{OUT}. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.
6	NC		**No Connect**.
7	V_{OUT}	I	**Chip Supply Voltage & Output Voltage Sense Input**. The V_{OUT} pin should be connected to the negative terminal of the schottky diode and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{OUT} pin, and the CE8310CFC10 ground pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{OUT} pin and the GND pin.
8	NC		**No Connect**.
9	CE	I	**Chip Enable**. CE = High: Normal free running operation CE = Low: Shutdown, quiescent current < 1μA. Typically, CE should be connected to IN through a 1M pull-up resistor.
10	NC		**No Connect**.
11	GND	P	**Signal and Power Ground**. Connect PGND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors.. This pin should be connected to a continuous PCB ground for high-current power converter as close as to the device by several vias directly under the CE8310CFC10 for electrical contact and rated thermal performance. It dissipates the heat from the IC.

(1) I = input; O = output; P = power

■ ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, T_A=25°C)[1]

PARAMETER		SYMBOL	RATINGS	UNITS
Output Voltage range [2]		V_{OUT}	-0.3~7	V
SW Voltage[2]			-0.3~7	V
CE, FB Voltage[2]			-0.3~7	V
Peak SW Sink Current		I_{SWMAX}	3	A
Power Dissipation[3]	SOT-23	P_D	400	mW
	SOP8-PP		1200	mW
	DFN3x3-10		2200	mW
Operating Junction Temperature Range		T_j	-40~150	°C
Storage Temperature		T_{stg}	-40~125	°C
Lead Temperature(Soldering, 10 sec)		T_{solder}	260	°C
ESD rating[4]		Human Body Model - (HBM)	4000	V
		Machine Model- (MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = [T_J(MAX)-T_A]/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

(4) ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Chipower recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

■ RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNITS
Supply voltage at V_{IN}	1.8		5.5	V
Output voltage at V_{OUT}	3.0		5.5	V
Operating free air temperature range[1], T_A	-40		85	°C
Operating junction temperature range, T_j	-40		125	°C

(1) The CE8310 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

■ ELECTRICAL CHARACTERISTICS

Typical values are at T_A=25℃, unless otherwise specified, specifications apply for condition V_{IN}=V_{CE}=3.6V, V_{OUT}=5.0V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP(1)	MAX	UNITS
SUPPLY						
Operating quiescent current into V_{OUT}	I_Q	Measured On V_{OUT}, V_{FB}=0.75V		130	300	μA
Shutdown Current into IN	$I_{SHDNVIN}$	V_{CE}=0V		0.1	1	μA
LOGIC SIGNAL CE						
CE High-level Voltage	V_{CEH}	V_{CE} Falling, Device ON	1.5		V_{IN}	V
CE Low-level Voltage	V_{CEL}	V_{CE} Rising, Device Off			0.4	V
CE Leakage Current	I_{CE}	V_{CE}=5.0V		±0.1	±1	μA
OSCILLATOR						
Oscillator Frequency	f_{osc}			1.0		MHz
Max Duty Cycle	D_{MAX}	V_{FB}=0V	80	87		%
POWER SWITCH						
N-CH MOSFET On Resistance(2)	$R_{DS(ON)}$			100		mΩ
N-CH MOSFET Switch Leakage	I_{SWLEAK}	V_{CE}=0V,V_{SW}=5.0V		±0.01	±1	μA
NMOS Cycle by Cycle Current Limit(3)	I_{CL}	V_{OUT}=5.0V		3.0		A
Current Limit Delay to Output(4)				40		nS
OUTPUT						
Output Voltage Range(5)	V_{OUT}		3.0		5.5	V
Feedback regulation voltage	V_{FB}		0.588	0.600	0.612	V
Feedback Input bias Current(6)	I_{FB}	V_{FB}=0.75V			0.1	μA
OVER TEMPERATURE PROTECTION						
Thermal Shutdown	T_{TSD}			140		℃
Thermal Shutdown Hysteresis	T_{TSDHYS}			20		℃

(1) Typical numbers are at 25°C and represent the most likely norm.

(2) Does not include the bond wires. Measured directly at the die.

(3) Duty cycle affects current limit due to ramp generator.

(4) Specification is guaranteed by design and not 100% tested in production.

(5) The fixed voltage version effective output voltage.

(6) Bias current flows into FB pin. Specification is guaranteed by design and not 100% tested in production.

■ TYPICAL PERFORMANCE CHARACTERISTICS

(T_A=25℃, unless otherwise specified, Test Figure1 above)

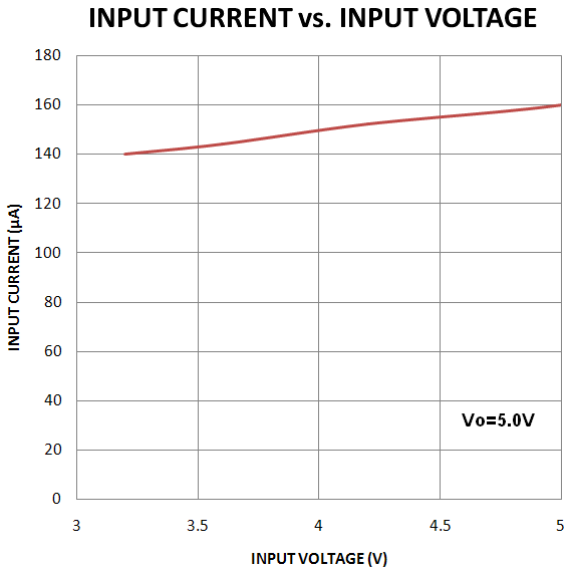


Figure 2

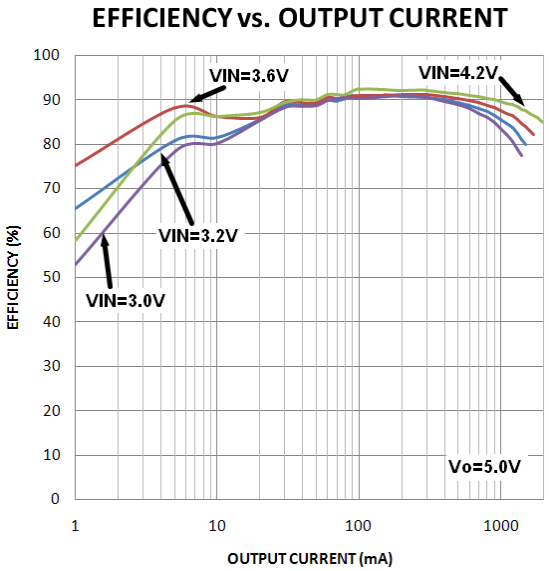
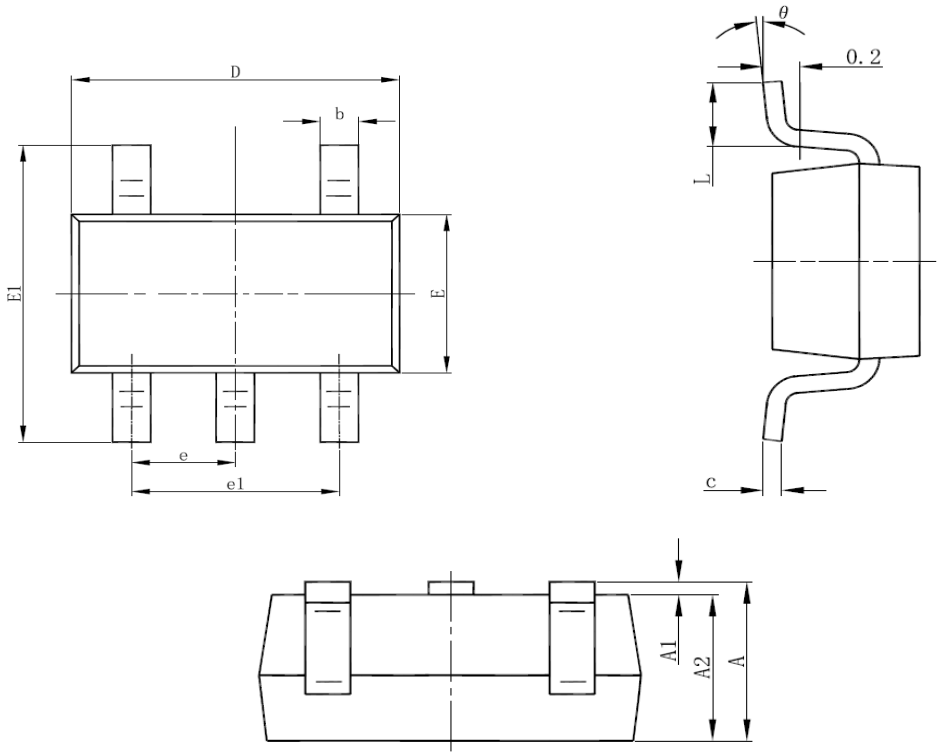


Figure 3

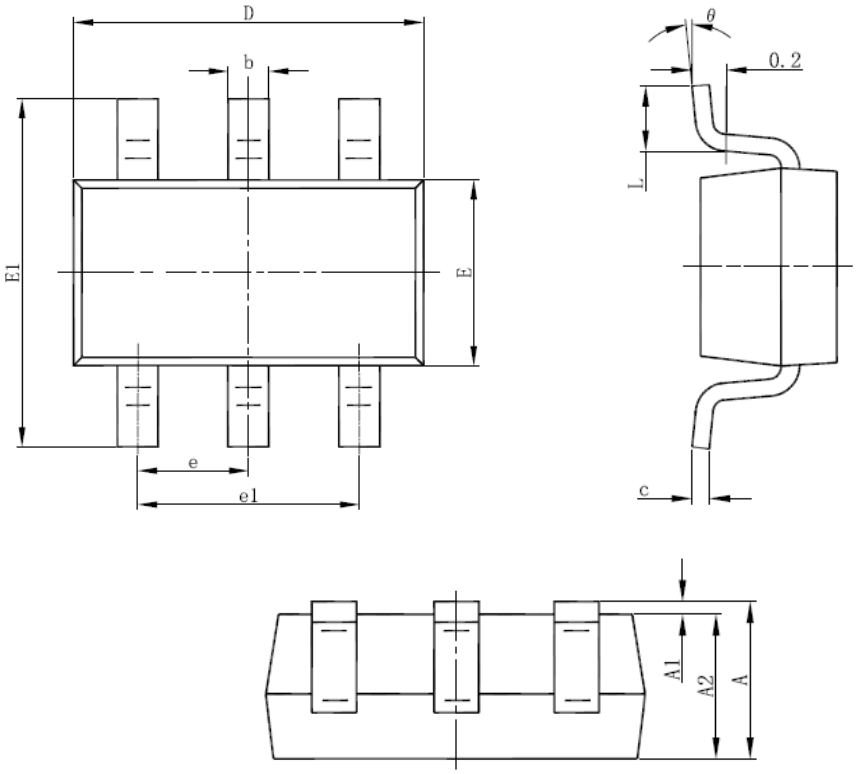
■ PACKAGING INFORMATION

● SOT-23-5 Package Outline Dimensions



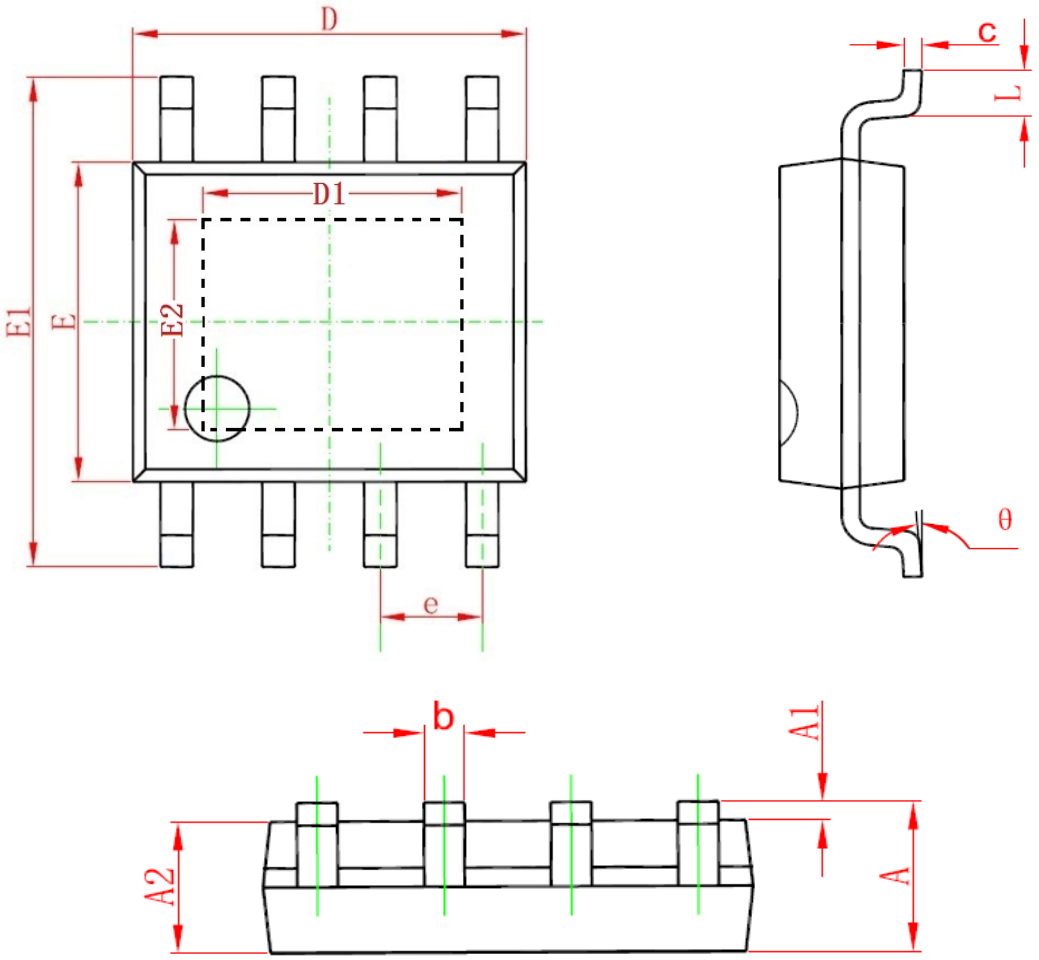
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

- **SOT-23-6 Package Outline Dimensions**



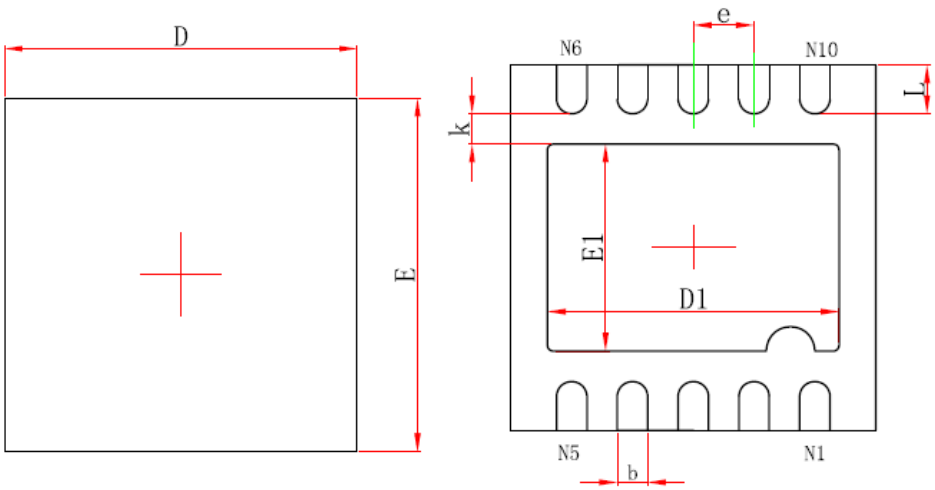
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

- **SOP8-PP Package Outline Dimensions**

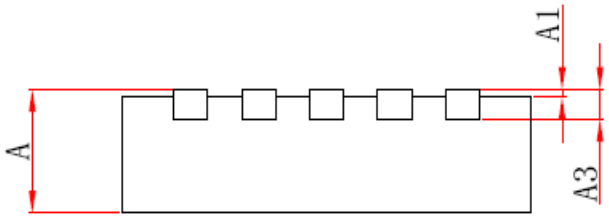


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0. 250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.100	3.500	0.122	0.137
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.200	2.600	0.086	0.102
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

- **DFN3x3-10 Package Outline Dimensions**



Top View **Bottom View**



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	2.300	2.500	0.091	0.098
E1	1.600	1.800	0.063	0.071
k	0.200MIN		0.008MIN	
b	0.180	0.300	0.007	0.012
e	0.500TYP		0.020TYP	
L	0.300	0.500	0.012	0.020