■ INTRODUCTION:

The CE8331 is a external power MOSFET boost controller designed for single-cell lithium or two cell alkaline, NiMH, or NiCd battery powered applications. A switching frequency of 1.0MHz minimizes solution footprint by allowing the use of tiny, low cost and low profile inductor and ceramic capacitors. The current mode PWM design is internally compensated. The CE8331 is rated over the -40°C to +85°C temperature range.

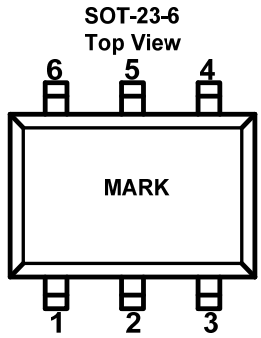
■ FEATURES:

- 1.0MHz Switching Frequency
- PWM/PFM Auto Switching Maintains High Efficiency Overall Load Current Range
- 600mV Feedback Voltage
- Over-Thermal Protection
- 88% efficiency @ Output 5V/2.5A Input 3.3V
- 86% efficiency @ Output 5V/3.0A Input 3.3V
- Ceramic Capacitor Compatible
- Tiny SOT23-6L Package

■ APPLICATIONS：

- Back-up Battery Charger
- Tablet PC
- 3G/4G Wireless Routers
- Mobile Internet Device
- Networking card powered from PCI

■ PIN CONFIGURATION:



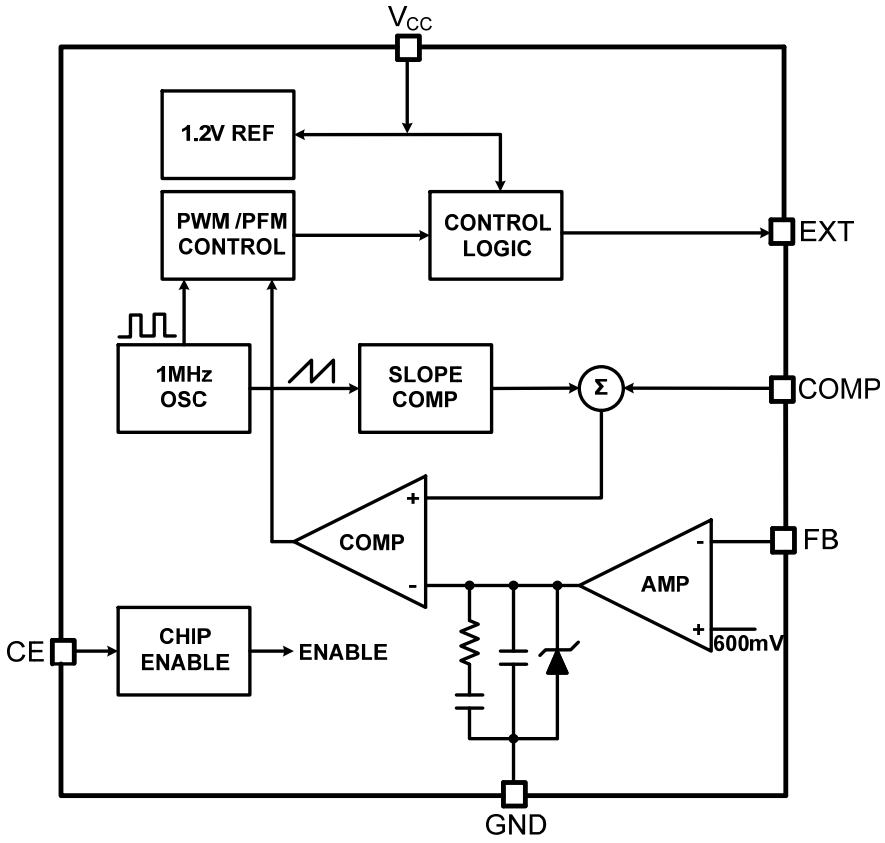
PIN NUMBER	PIN NAME	FUNCTION
1	COMP	Current Mode Compensation
2	GND	Signal and Power Ground
3	FB/V_{OUT}	Feedback Input / Output Voltage for fixed Voltage Version
4	CE	Chip Enable. High Active
5	V_{CC}	Chip Supply Voltage
6	EXT	External Power MOSFET Gate Drive

■ ORDER INFORMATION:

CE8331①②③④

DESIGNATOR	SYMBOL	DESCRIPTION
①	C	With Enable
②③	Integer	Output Voltage e.g.5.0V=②:5, ③:0 Adj=②:, ③:
④	E	Package：SOT-23-6L

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(unless otherwise specified , T_{opr}=25°C)[1]

PARAMETER		SYMBOL	RATINGS	UNITS
Supply Voltage[2]		V_{CC}	V_{SS}-0.3~V_{SS}+7	V
CE,COMP,FB Voltage[2]			V_{SS}-0.3~V_{CC}+0.3	V
Power Dissipation	SOT-23-6	P_d	350	mW
Operating Junction Temperature		T_j	150	℃
Storage Temperature		T_{stg}	-40~+125	℃
Soldering Temperature & Time		T_{solder}	260℃, 10s	
ESD rating[3]		Human Body Model - (HBM)	2	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

■ ELECTRICAL CHARACTERISTICS

Typical values are at T_{opr}=25℃, unless otherwise specified, specifications apply for condition V_{CC} = V_{CE} = 3.6 V, V_{OUT} = 5.0 V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Feedback Voltage	V_{FB}		588	600	612	mV
Supply voltage	V_{CC}		2.0		5.5	V
Quiescent Current	I_{CC}	V_{FB}=750mV		200	400	μA
Shutdown Current	I_{SHDN}	V_{CE}=GND		0.1	1	μA
Max Duty Cycle		V_{FB}=GND	80	87		%
Oscillator Frequency	f_{osc}			1.0		MHz
CE "High" Voltage(1)			1.5		V_{CC}	V
CE "Low" Voltage(2)					0.4	V
CE Leakage Current	I_{CE}	V_{CE}=5.0V		0.1	1	μA
Over Thermal Shutdown				140		℃
Over Thermal Hysteresis				20		℃
Soft Start Time	tss			2		ms
EXT Pin Output Current	I_{EXTH}	V_{EXT}= V_{CC} -0.4V		-300		mA
	I_{EXTL}	V_{EXT}=0.4V		200		mA

NOTE :

1. High Voltage level：Forcing CE above 1.5V enables the part.
2. Low Voltage level：Forcing CE below 0.4V shuts down the device. In shutdown, all functions are disabled drawing <1μA supply current. Do not leave CE floating.

■ TYPICAL APPLICATION CIRCUITS

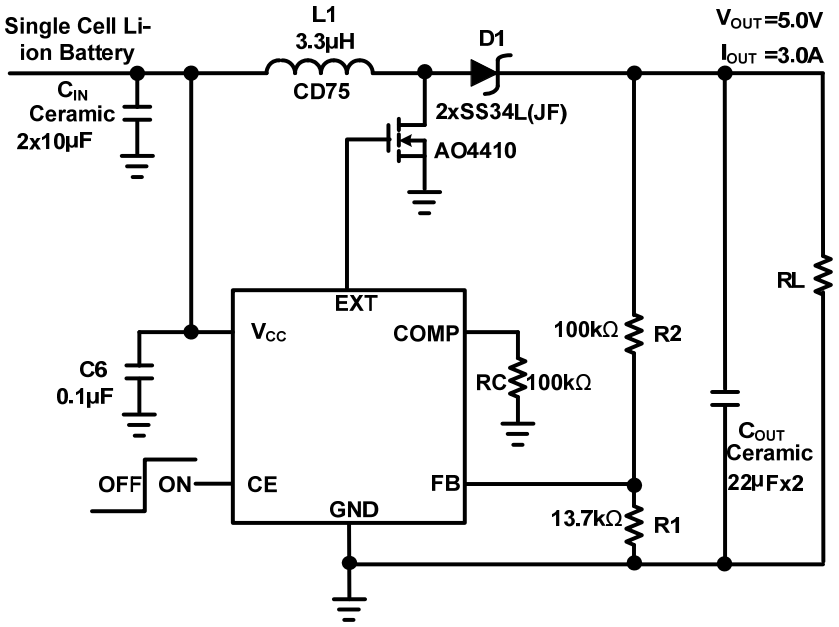
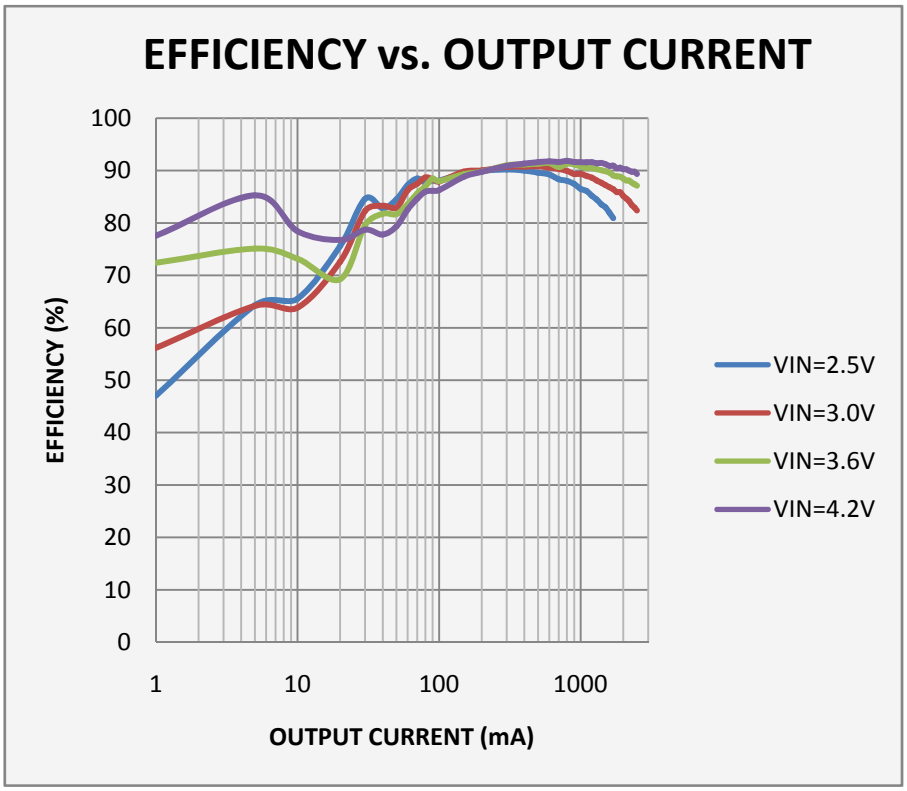


Figure1 Standard Application Circuit

■ TYPICAL PERFORMANCE CHARACTERISTICS

(T_{opr}=25℃, unless otherwise specified, Test Figure1 above)



■ OPERATION

The CE8331 boost controller is targeted for single-cell or dual-cell or triangle-cell alkaline, NiMH, and NiCd and single-cell lithium-ion battery applications. The high 1.0MHz switching frequency of the CE8331 facilitates output filter component size reduction for improved power density and reduced overall footprint.

SLOPE COMPENSATION

Slope compensation provides stability in constant frequency architecture by preventing sub-harmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 50%. This slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for excellent load and line response.

CURRENT SENSING

A signal representing NMOS switch current is summed with the slope compensator. The summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. The current signal is blanked for 40ns to enhance noise rejection.

PWM/PFM AUTO SWITCHING

The CE8331 offers PWM/PFM automatic switching operation. The PWM operation is shifted to the PFM operation automatically at light load so that it maintains high efficiency over a wide range of load currents.

■ APPLICATION INFORMATION

The basic CE8331 application circuits are shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

INDUCTOR SELECTION

Inductance value is decided based on different condition. 2.2μH to 4.7μH inductor value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency. Also, it avoid inductor saturation which will cause circuit system unstable and lower core loss at 1 MHz.

There are several considerations in choosing this inductor.

1.Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 30% of the maximum average input current. The inductance is calculated as:

$$\mathbf{L} = \left(\frac{\mathbf{V_{IN}}}{\mathbf{V_{OUT}}}\right)^2 \frac{(\mathbf{V_{OUT}} - \mathbf{V_{IN}})}{\mathbf{f_{osc}} * \mathbf{I_{OUT.MAX}} * \mathbf{40\%}}$$

where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The CE8331 boost controller is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2.The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$\mathbf{I_{SAT.MIN}} > \left(\frac{\mathbf{V_{OUT}}}{\mathbf{V_{IN}}}\right) * \mathbf{I_{OUT.MAX}} + \left(\frac{\mathbf{V_{IN}}}{\mathbf{V_{OUT}}}\right)^2 \frac{(\mathbf{V_{OUT}} - \mathbf{V_{IN}})}{\mathbf{2} * \mathbf{f_{osc}} * \mathbf{L}}$$

3.The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good overall efficiency.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the CE8331 requires to operate.

INPUT CAPACITOR SELECTION

For the input capacitor (C_{IN} in Figure 1), the ripple current through input capacitor is calculated as:

$$\mathbf{I_{CIN\_RMS}} = \frac{\mathbf{V_{IN}} \cdot (\mathbf{V_{OUT}} - \mathbf{V_{IN}})}{\mathbf{2\sqrt{3} \cdot L \cdot f_{osc} \cdot V_{OUT}}}$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the V_{IN} and GND. Care should be taken to minimize the loop area formed by C_{IN}, and V_{IN}/GND. In this case, a 1210 sized 22μF/10V X5R low ESR ceramic capacitor is recommended. If desired, a smaller, 0805 sized, 10μF/10V, X5R low ESR ceramic capacitor can be substituted for the input capacitor (C_{IN}).

OUTPUT CAPACITOR SELECTION

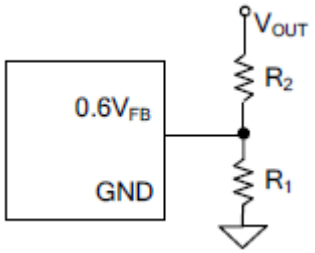
For the output capacitor (C_{OUT} in Figure 1), it is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use two 22μF/10V X5R or better grade ceramic

capacitors in parallel for stability, transient, and ripple performance.

FEEDBACK RESISTOR DIVIDERS R1 AND R2:

The output voltage is set by a resistive voltage divider from the output voltage to FB. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10k and 1M is recommended for both resistors. If R2=100k is chosen, then R1 can be calculated to be:

$R1= (R2X0.6V)/(V_{OUT} - 0.6V)$



DIODE SELECTION

Schottky diode is a good choice for high efficiency operation, because of its low forward voltage drop and fast reverse recovery time. Ensure the diode average and peak current rating must be higher than the average output current and peak inductor current. The schottky diode reverse breakdown voltage should be larger than the output voltage.

For 5V/2A output application, use a schottky diode with SMC package such as SS54, SK54 or equivalent with rated current over 5A. Do not use ordinary rectifier diodes, since the slow recovery times will compromise efficiency.

MOSFET SELECTION

Use an Nch power MOS FET such as AO4410. A MOS FET that has low ON-resistance (RON) and input capacitance (CISS) is ideal for gaining efficiency.

The ON-resistance and input capacitance generally have a tradeoff relationship. ON-resistance is efficient in the range where the output current is high with relatively low frequency switching, and input capacitance is efficient in the range where the output current is medium to low with high frequency switching. Therefore, select a MOS FET for which the ON-resistance and input capacitance are optimum under your usage conditions.

COMPENSATION RESISTOR SELECTION

The CE8331 incorporates a transconductance amplifier in its feedback path to allow the user some adjustment on the transient response and better regulation. The CE8331 uses current mode control architecture which has a fast current sense loop and a slow voltage feedback loop. The slow voltage loop does not require any compensation. The fast current feedback loop must be compensated for stable operation. Different from other circuit, the CE8331compensation network is a resistor RC from COMP pin to ground.

COMP is a sensitive node. Please keep it away from L and D switching node on the PCB layout to avoid the noise problem. The RC resistor value is recommended for general application circuit in table 1 as a matter of experience.

Table 1 The RC resistor value

V_{OUT}/V_{IN}	R_{min} (K Ω)	R_{typ} (K Ω)	R_{max} (K Ω)
1-2	40	100	220
2-3	10	20	40
3-4	2	4	10

PCB LAYOUT GUIDANCE

The layout design of CE8331 boost controller is relatively simple.

For the best efficiency and minimum noise problems, the following suggestions should be taken. These items are also illustrated graphically in Figure 1.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) The power traces, consisting of the GND trace, the switching trace and the V_{IN} trace should be kept short, direct and wide to allow large current flow. Put enough multiply-layer pads when they need to change the trace layer.

3) Place the (+) plate of C_{IN} near V_{IN} as closely as possible and the loop area formed by C_{IN} and GND must be minimized to maintain input voltage steady and filter out the pulsing input current.

4) The GND of the IC, the (-) plate of C_{IN} and C_{OUT} should be connected as close as possible, together directly to a ground plane.

5) The PCB copper area associated with L and D switching node must be minimized to avoid the potential noise problem and reduce EMI.

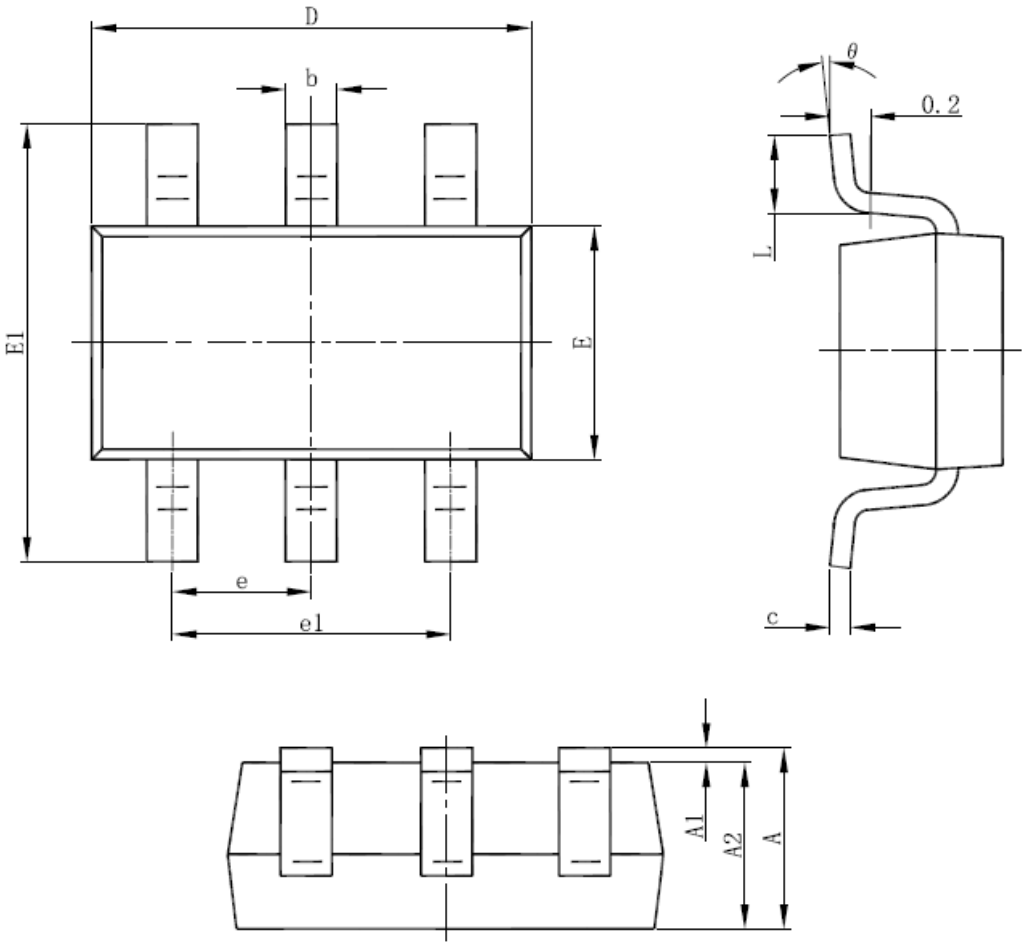
6) The resistive divider R1 and R2 must be connected to FB pin directly as closely as possible. And FB is a sensitive node. Please keep it away from L and D switching node on the PCB layout to avoid the noise problem.

7) COMP is a sensitive node. Please keep it away from L and D switching node on the PCB layout to avoid the noise problem.

8) If the system chip interfacing with the CE pin has a high impedance state at shutdown mode and the V_{CC} is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the CE and GND pins to prevent the noise from falsely turning on the boost regulator at shutdown mode.

■ PACKAGING INFORMATION

● SOT-23-6 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°