■ INTRODUCTION:

The CE8406 devices provide a power supply solution for products powered by either a one-cell, two-cell, or three-cell alkaline, NiCd or NiMH, or one-cell Li-ion or Li-polymer battery. The boost converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency, which contain an internal NMOS switch and PMOS synchronous rectifier. The maximum peak current in the boost switch is typically limited to a value of 1.2A.

A switching frequency of 1.2MHz minimizes solution footprint by allowing the use of tiny, low profile inductors and ceramic capacitors. The current mode PWM design is internally compensated, reducing external parts count. Anti-ringing control circuitry reduces EMI concerns by damping the inductor in discontinuous mode. The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. The device features low shutdown current less than 1μA.

■ FEATURES:

- Up to 96% Efficiency
- True Output Load Disconnect During Shutdown
- Delivers 100mA@3.3V from Single AA Cell
- Delivers 300mA@5V from Two AA Cells
- Delivers 600mA@5V from Single Li Cell
- Low Voltage Start-Up: 0.85V
- Continuous Switching at Light Loads
- Internal Synchronous Rectifier
- Current Mode Control with Internal Compensation
- 1.2MHz Fixed Frequency Switching
- Input Range: 0.5V to 4.5V
- Output Range: 2.5V to 4.3V (Up to 5.5V with Schottky)
- Logic Controlled Shutdown(<1μA)
- Anti-ringing Control Minimizes EMI
- 1.2A Peak Switch Current Limit
- Over Temperature Protection
- Tiny External Components
- Low Profile (1mm) SOT-23 Package

■ APPLICATIONS：

- Digital Still and Video Cameras
- Portable Applications Using Single Li+ Cell
- Bus Powered USB Hosts
- USB Hosts Without Native 5-V Supplies
- Portable Audio Players
- LCD Bias Supplies White LED Lighting
- Wireless Handsets
- GPS Receivers
- Personal Medical Products

■ ORDER INFORMATION(1)

Operating free air temperature range	Output Voltage	Package	Device No.
-40~+85℃	Adjustable	SOT-23-6	CE8406AE
-40~+85℃	3.3V		CE8406A33E
-40~+85℃	5.0V		CE8406A50E

(1) Contact Chipower to check availability of other fixed output voltage versions.

■ TYPICAL APPLICATION CIRCUIT

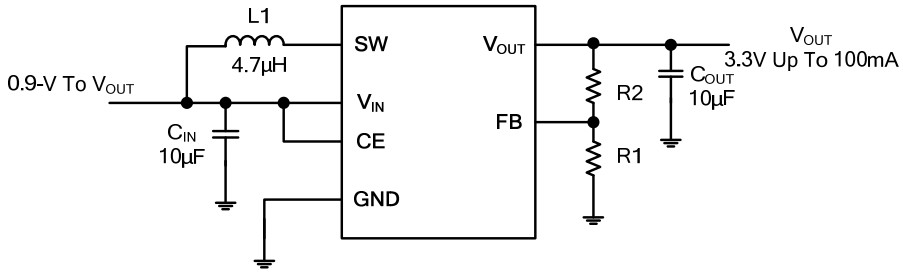


Figure 1 Standard Application Circuit

■ PIN CONFIGURATION:

PIN ASSIGNMENTS

(TOP VIEW)

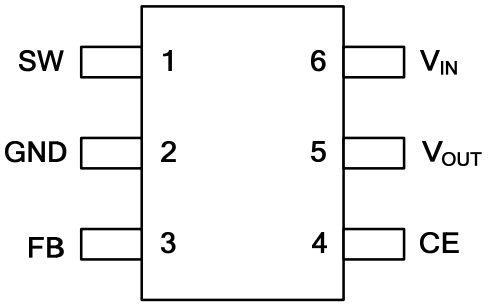


Table 1. SOT23-6 Pin Description

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SW	I/O	**Switch Pin**. Connect an inductor between this pin and V_{IN}. Keep the PCB trace lengths as short and wide as is practical to reduce EMI and voltage overshoot. If the inductor current falls to zero, or pin CE is low, an internal anti-ringing switch is connected from this pin to V_{IN} to minimize EMI.
2	GND	P	**Signal and Power Ground**. Connect GND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors.. This pin should be connected to a continuous PCB ground for high-current power converter as close as to the device by several vias directly under the IC for electrical contact and rated thermal performance. It dissipates the heat from the IC.
3	FB/NC	I	**Feedback Input / Not Connect (for fixed Voltage)**. Feedback Input to the gm Error Amplifier. Connect resistor divider tap to this pin. The output voltage can be adjusted from 2.5V to 5.5V by: V_{OUT} =1.23V•[1+(R2/R1)] The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor, SW、inductor and Schottky diode switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.
4	CE	I	**Chip Enable**. CE=High: Normal free running operation, 1.2MHz typical operating frequency. CE=Low: Shutdown; quiescent current <1μA. Output capacitor can be completely discharged through the load or feedback resistors. An anti-ringing switch is internally connected between SW and V_{IN}. If CE is undefined, pin SW may ring.
5	V_{OUT}	I/O	**Output Voltage Sense Input and Drain of the Internal Synchronous Rectifier P-MOSFET**. Bias is derived from V_{OUT} when V_{OUT} exceeds 2.3V. PCB trace length from V_{OUT} to the output filter capacitor(s) should be as short and wide as possible. Care should be taken to minimize the loop area formed by the output filter capacitor(s) connections, the V_{OUT} pin, and the CE8406 ground pin. The minimum recommended output filter capacitance is 4.7μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{OUT} pin and the GND pin. V_{OUT} is completely disconnected from V_{IN} when CE is low, due to the output

			disconnect feature.
6	V_{IN}	I	**Battery Input Voltage**. The device gets its start-up bias from V_{IN}. Once V_{OUT} exceeds 2.3V, bias comes from V_{OUT}. Thus, once started, operation is completely independent from V_{IN}. Operation is only limited by the output power level and the battery's internal series resistance. PCB trace length from V_{IN} to the input filter capacitor(s) should be as short and wide as possible. Care should be taken to minimize the loop area formed by the input filter capacitor(s) connections, the V_{IN} pin, and the CE8406 ground pin. The minimum recommended input filter capacitance is 4.7μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{IN} pin and the GND pin.

(1) I = input; O = output; P = power

■ ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, T_A=25°C)[1]

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage[2]	V_{IN}	-0.3~7	V
SW Voltage[2]		-0.3~7	V
CE, FB Voltage[2]		-0.3~7	V
Output Voltage range [2]	V_{OUT}	-0.3~7	V
Peak SW Sink and Source Current	I_{SWMAX}	1.5	A
Operating Virtual Junction Temperature Range	T_j	-40~150	℃
Storage Temperature	T_{stg}	-40~125	℃
Lead Temperature(Soldering, 10 sec)	T_{solder}	260	℃
ESD rating[3]	Human Body Model - (HBM)	4000	V
	Machine Model- (MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Chipower recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision

integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

■ DISSIPATION RATINGS(1)

PACKAGE	θ_{JA}(2)	T_A≤25℃ POWER RATING	DERATING FACTOR ABOVE T_A=25℃
SOT-23-6	250°C /W	400mW	4mW/°C

(1) Exceeding the maximum junction temperature will force the device into thermal shutdown.

(2) θ_{JA} is measured in the natural convection at T_A=25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

■ RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNITS
Supply voltage at V_{IN}	0.9		5.5	V
Output voltage at V_{OUT}	2.5		5.5	V
Operating free air temperature range(1), T_A	-40		85	℃
Operating junction temperature range, T_j	-40		125	℃

(1) The CE8406 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85 °C operating temperature range are assured by design, characterization and correlation with statistical process controls.

■ ELECTRICAL CHARACTERISTICS

Typical values are at T_A=25℃, unless otherwise specified, specifications apply for condition V_{IN}=V_{CE}=1.2V, V_{OUT}=3.3 V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP(1)	MAX	UNITS
POWER SUPPLIES						
Minimum Start-Up Voltage	V_{START}	I_{LOAD}=1mA		0.85	1	V
Minimum Operating Voltage(2)	$V_{IN(MIN)}$	V_{CE}=V_{IN}		0.5	0.65	V
Operating quiescent current into V_{OUT}	I_Q	Measured On V_{OUT}, Nonswitching		300	500	μA
Shutdown Current into IN	$I_{SHDN-IN}$	V_{CE}=0V		0.1	1.0	μA
CHIP ENABLE INPUT LOGIC SIGNAL CE						
CE High-level Voltage	V_{CEH}	V_{CE} Falling, Device ON	1.5		V_{IN}	V
CE Low-level Voltage	V_{CEL}	V_{CE} Rising, Device Off			0.4	V
CE Leakage Current	I_{CE}	V_{CE}=5.0V		±0.1	±1	μA
OSCILLATOR						
Oscillator Frequency	f_{osc}		0.9	1.2	1.5	MHz
Max Duty Cycle	D_{MAX}	V_{FB}=1.15V	80	87		%

POWER SWITCH						
N-CH MOSFET On Resistance(3)	$R_{DS(ON)}$	V_{OUT}=3.3V		350		mΩ
		V_{OUT}=5.0V		200		
P-CH MOSFET On Resistance(3)		V_{OUT}=3.3V		450		
		V_{OUT}=5.0V		300		
N-CH MOSFET Switch Leakage	I_{SWLEAK}	V_{SW}=5.0V		±0.01	±1	μA
P-CH MOSFET Switch Leakage		V_{SW}=5.0V, V_{OUT}=0V		±0.01	±1	μA
NMOS Cycle by Cycle Current Limit(4)	I_{CL}	V_{OUT}=5.0V		1.2		A
Current Limit Delay to Output(5)				40		nS
OUTPUT						
Output Voltage Range(6)	V_{OUT}		2.5		5.5	V
Feedback regulation voltage	V_{FB}		1.192	1.230	1.268	V
Feedback Input bias Current(7)	I_{FB}	V_{FB}=1.30V			±50	nA
OVER TEMPERATURE PROTECTION						
Thermal Shutdown	T_{TSD}			150		℃
Thermal Shutdown Hysteresis	T_{TSDHYS}			15		℃

(1) Typical numbers are at 25°C and represent the most likely norm.

(2) Minimum V_{IN} operation after start-up is only limited by the battery's ability to provide the necessary power as it enters a deeply discharged state.

(3) Does not include the bond wires. Measured directly at the die.

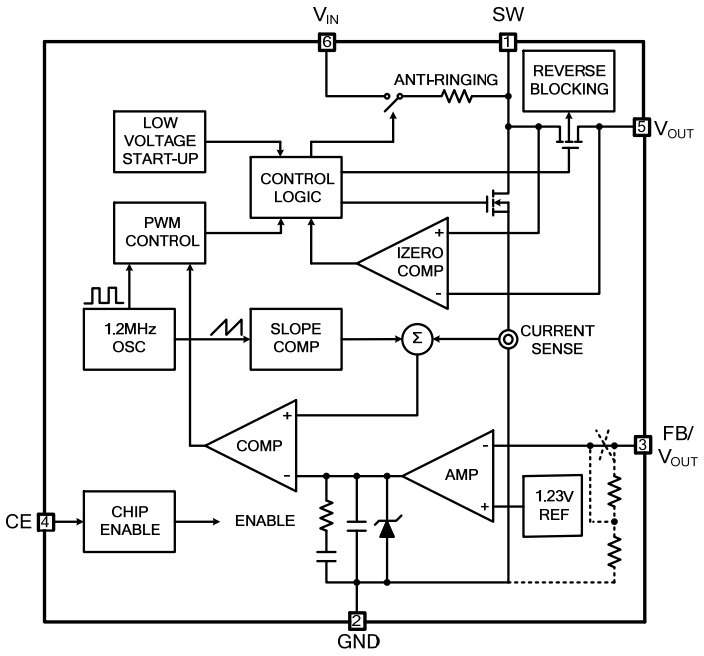
(4) Duty cycle affects current limit due to ramp generator.

(5) Specification is guaranteed by design and not 100% tested in production.

(6) The fixed voltage version effective output voltage.

(7) Bias current flows into FB pin. Specification is guaranteed by design and not 100% tested in production.

■ BLOCK DIAGRAM



Future 2. Functional Block Diagram

■ DETAILED DESCRIPTION

The CE8406 is a 1.2MHz synchronous boost converter housed in a 6-lead thin SOT-23 package. Able to operate from an input voltage below 1V, the devices feature fixed frequency, current mode PWM control for exceptional line and load regulation. With its low $R_{DS(ON)}$ and gate charge internal MOSFET switches, the devices maintain high efficiency over a wide range of load current. Its high 1.2MHz switching frequency facilitates output filter component size reduction for improved power density and reduced overall footprint. It also provides greater bandwidth and improved transient response over other lower frequency boost converters.

Operation can be best understood by referring to the Functional Block Diagram.

CONTROLLER CIRCUIT

The controller circuit of the device is based on a fixed frequency multiple feed-forward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So, changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the

switch and the inductor. The typical peak-current limit is set to 1.2A. An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

SYNCHRONOUS RECTIFICATION

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier, which improves efficiency and eliminates the need of an external Schottky diode. Because the commonly used discrete Schottky rectifier is replaced with a low $R_{DS(on)}$ PMOS switch, which reduces the conduction loss , the power conversion efficiency reaches values above 90%.

SLOPE COMPENSATION

The CE8406 is based on a slope compensated current mode PWM control topology. It operates at a fixed frequency of 1.2MHz. At the beginning of each clock cycle, the main switch (NMOS) is turned on and the inductor current starts to ramp.

After the maximum duty cycle or the sense current signal equals the error amplifier (EA) output, the main switch is turned off and the synchronous switch (PMOS) is turned on. Slope compensation provides stability in constant frequency architecture by preventing sub-harmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 50%.This control topology features stable switching and cycle-by-cycle current limiting which can prevent the main switch from overstress and the external inductor from saturating, it provides excellent load and line response.

LOW VOLTAGE START-UP

The CE8406 includes an independent start-up oscillator designed to start up at a typical V_{IN} voltage of 0.85V or higher. In this mode, the IC operates completely open-loop and the current limit is also set internally to 600mA typically. The low voltage start-up circuitry controls the internal NMOS switch up to a maximum peak inductor current of 600mA typically, with an approximate 0.5ms (approx.) off-time during start-up, allowing the devices to start up into an output load. Once the output voltage exceeds 2.3V, the start-up circuitry is disabled and normal close-loop fixed frequency PWM operation is initiated. In this mode, the CE8406 power themselves from V_{OUT} instead of V_{IN} and operates independent of V_{IN}, allowing extended operating time as the battery voltage can droop to several tenths of a volt without affecting the circuit operation. The only limiting factor for the application becomes the ability of the battery to supply sufficient energy to the output. The current limit is also set internally to 1.2A typically

LOW NOISE FIXED FREQUENCY OPERATION

Oscillator: The frequency of operation is internally set to 1.2MHz.

Error Amplifier: The error amplifier is an internally compensated transconductance type (current output). The internal 1.23V reference voltage is compared to the voltage at the FB pin to generate an error signal

at the output of the error amplifier. A voltage divider from V_{OUT} to ground programs the output voltage via FB from 2.5V to 5.5V using the equation:

V_{OUT}=1.23V•[1+(R2/R1)]

Current Sensing: Lossless current sensing converts a signal representing NMOS switch current to a voltage to be summed with the internal slope compensation. The summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. Peak switch current is limited to approximately 1.2A independent of input or output voltage. The switch current signal is blanked for 40ns to enhance noise rejection.

Zero Current Comparator: The zero current comparator monitors the inductor current to the output and shuts off the synchronous rectifier once this current reduces to approximately 27mA. This prevents the inductor current from reversing in polarity thereby improving efficiency at light loads.

Antiringing Control: The antiringing control circuitry prevents high frequency ringing of the SW pin as the inductor current goes to zero in discontinuous mode by placing a resistor across the inductor to damp the resonant circuit formed by L and C_{SW} (capacitance on SW pin).

OUTPUT DISCONNECT AND INRUSH LIMITING

The CE8406 is designed to allow true output disconnect by eliminating backgate diode conduction of the internal PMOS rectifier. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. However, this device uses a special circuit which takes the cathode of the backgate diode of the high-side PMOS and disconnects it from the source when the converter is not enabled (CE=low).

The benefit of this feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components must be added to the design to make sure that the battery is disconnected from the output of the converter. This allows V_{OUT} to go to zero volts during shutdown, drawing zero current from the input source.

It also allows for inrush current limiting at start-up, minimizing surge currents seen by the input supply. Note that to obtain the advantage of output disconnect, there must not be an external Schottky diode connected between the SW pin and V_{OUT}.

Board layout is extremely critical to minimize voltage overshoot on the SW pin due to stray inductance. Keep the output filter capacitor as close as possible to the V_{OUT} pin and use very low ESR/ESL ceramic capacitors tied to a good ground plane. For applications with V_{OUT} over 4.3V, a Schottky diode is required to limit the peak SW voltage to less than 6V unless some form of external snubbing is employed. This diode must also be placed very close to the pins to minimize stray inductance.

See the Applications Information.

DEVICE SHUTDOWN

When CE is set logic high, the CE8406 is put into active mode operation. If CE is set logic low, the device

is put into shutdown mode and draws less than 1μA current from battery. After start-up, the internal circuitry is supplied by V_{OUT}, however, if shutdown mode is enabled, the internal circuitry will be supplied by the input source again.

If CE is driven from a logic-level output, the logic high-level (on) should be referenced to V_{OUT} to avoid intermittently switching the device on.

Note:

If pin CE is not used, it should be connected directly to pin V_{OUT}.

In cases where there is residual voltage during shutdown, some small amount of energy will be transferred from pin V_{OUT} to pin V_{IN} immediately after shutdown, resulting in a momentary spike of the voltage at pin V_{IN}. The ratio of C_{IN} and C_{OUT} partly determine the size and duration of this spike, as does the current-sink ability of the input device.

Thermal Shutdown

If the die temperature reaches 150°C, the part will go into thermal shutdown, all switches will be turned off The part will be enabled again when the die temperature drops by about 15°C.

■ TYPICAL PERFORMANCE CHARACTERISTICS

(T_A=25℃, unless otherwise specified, Test Figure1 above)

Table of Graphs

			FIGURE
η	Efficiency	vs Output Current and Input Voltage	Figure3
			Figure5
			Figure7
			Figure9
ΔV_{OUT}	Load Regulation	vs Output Current and Input Voltage	Figure4
			Figure6
			Figure8
			Figure10
V_{START}	Minimum Start-Up Voltage	vs Output Current	Figure11
Waveforms	SW Pin Antiringing Operation		Figure12
	SW Pin Fixed Frequency, Continuous Inductor Current Operation		Figure13
	V_{OUT} Load transient response		Figure14

Efficiency vs Output Current

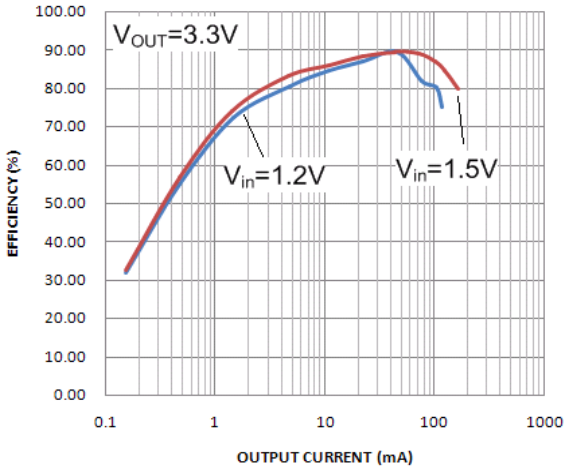


Figure 3

Load Regulation

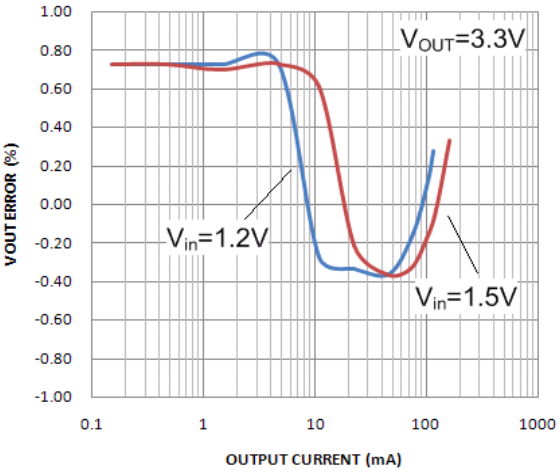


Figure 4

Efficiency vs Output Current

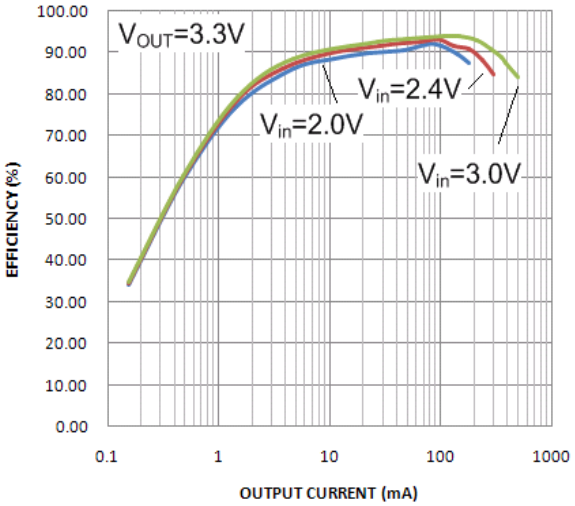


Figure 5

Load Regulation

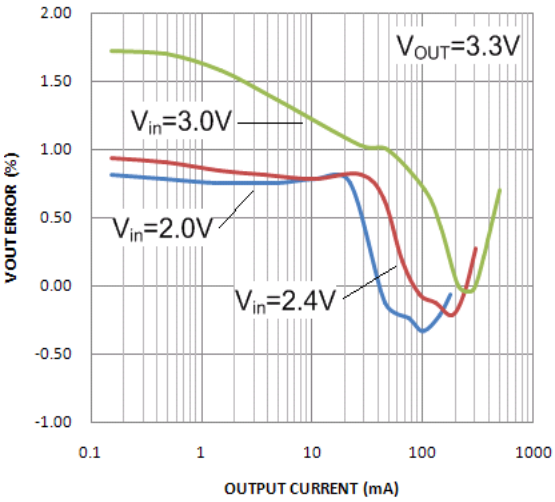


Figure 6

Efficiency vs Output Current

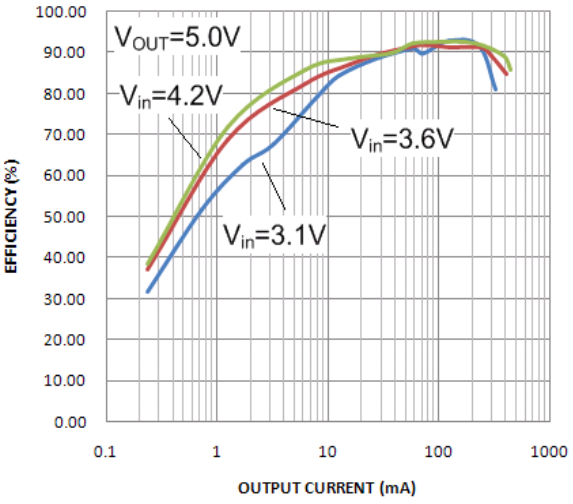


Figure 7

Load Regulation

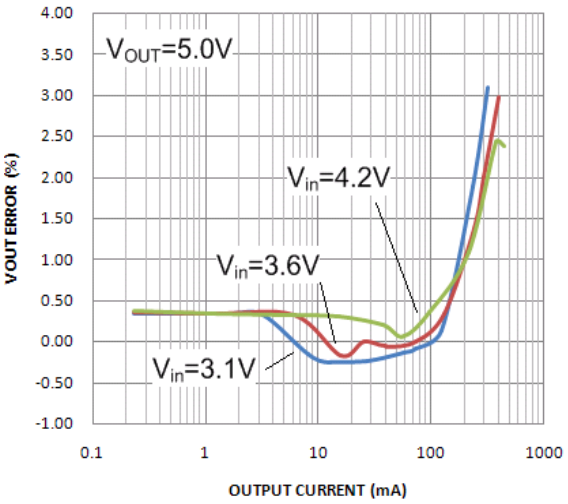


Figure 8

Efficiency vs Output Current

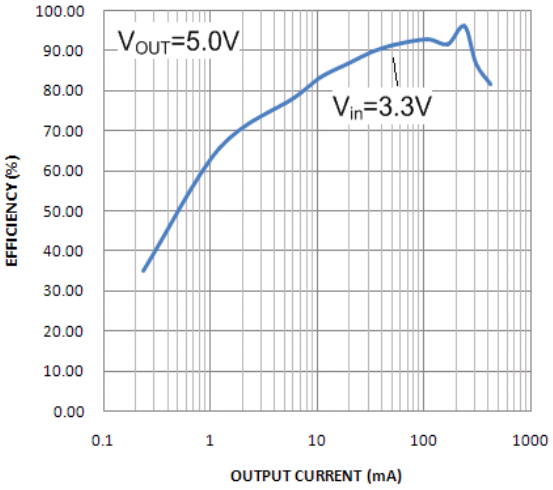


Figure 9

Load Regulation

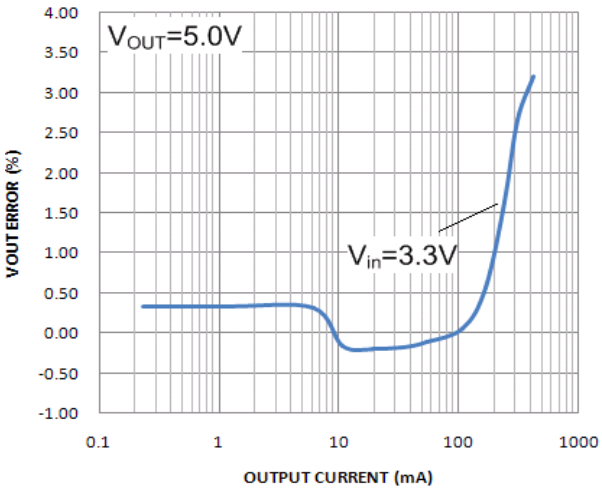


Figure 10

Minimum Start-Up Voltage vs Output Current

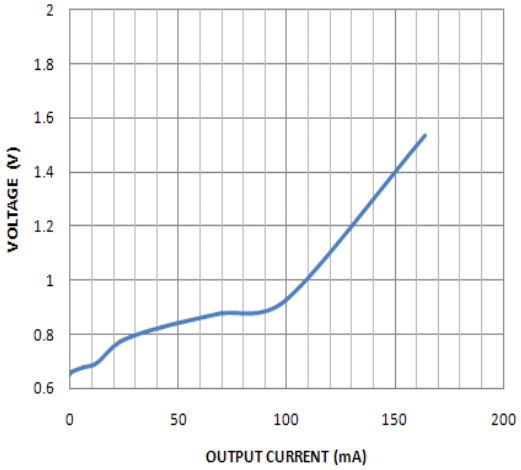


Figure 11

SW Pin Antiringing Operation

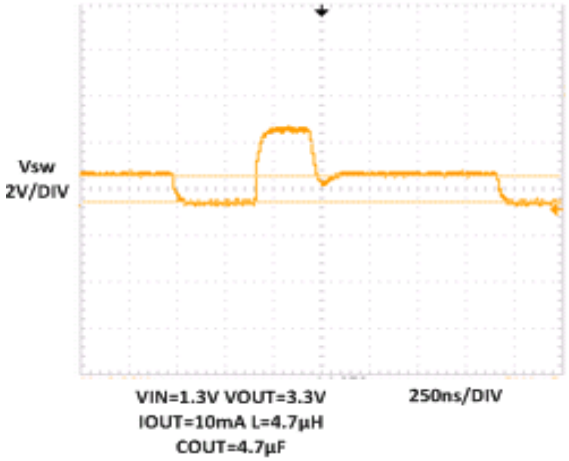


Figure 12

SW Pin Fixed Frequency,

Continuous Inductor Current Operation

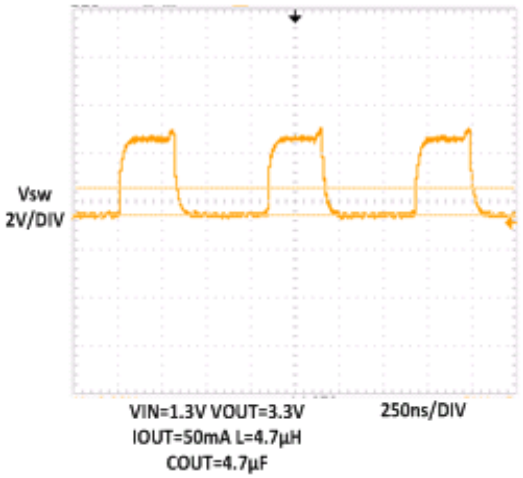


Figure 13

V_{OUT} Load Transient Response

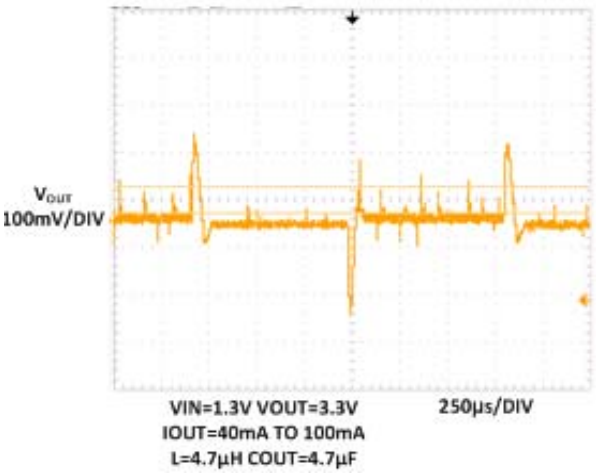


Figure 14

■ APPLICATION INFORMATION

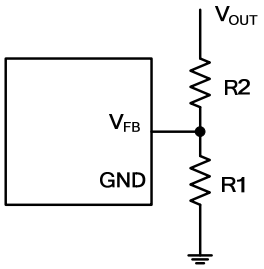
DESIGN PROCEDURE

The CE8406 dc-dc converter is intended for systems powered by a single-cell, up to triple-cell alkaline, NiCd, NiMH battery with a typical terminal voltage between 0.9V and 4.5V. It can also be used in systems powered by one-cell Li-ion or Li-polymer with a typical voltage between 2.7V and 4.2V. Additionally, any other voltage source with a typical output voltage between 0.9 V and 4.5 V can power systems where the CE8406 is used. Due to the nature of boost converters, the output voltage regulation is only maintained when the input voltage applied is lower than the programmed output voltage.

Setting The Output Voltage

For the CE8406 adjustable output version, the internal 1.23V reference voltage is compared to the voltage at the FB pin to generate an error signal at the output of the error amplifier. A voltage divider from V_{OUT} to ground programs the output voltage via FB from 2.5V to 5.5V using the equation:

$$V_{OUT}=1.23V•[1+(R2/R1)]$$



The use of 1% accuracy metal film resistor is recommended for the better output voltage accuracy. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2.

Table1 lists the recommended values for particular output voltage settings.

Table 1. Resistor Selection for V_{OUT} Setting

V_{OUT}	R2(Ω)	R1(Ω)
3.3V	1.02M	604K
5.0V	1.02M	332K

Fixed Output Voltage

The CE8406 has two fixed output voltage options: 3.3V and 5V. An internal resistor divider is connected to the FB pin internally, which eliminates the need for external feedback resistors. When designing with the fixed output voltage option, remember to leave the FB pin open; otherwise the output voltage will be affected. However, a feed-forward capacitor can still be added between the FB pin and V_{OUT} pin to enhance the control loop performance.

Inductor Selection

The CE8406 can utilize small surface mount and chip inductors due to its fast 1.2MHz switching frequency. Typically, a 4.7μH inductor is recommended for most applications. Larger values of inductance will allow greater output current capability by reducing the inductor ripple current. Increasing the inductance above 10μH will increase size while providing negligible improvement in output current capability.

The approximate output current capability of the CE8406 versus inductance value is given in the equation below:

$$I_{OUT(MAX)} = \eta \bullet (I_{CL} - \frac{V_{IN} \bullet D}{2L \bullet f_{osc}}) \bullet (1 - D)$$

where:

η = estimated efficiency;

I_{CL} = peak current limit value (1.2A);

V_{IN} = input (battery) voltage;

D = steady-state duty ratio = $(V_{OUT} - V_{IN})/V_{OUT}$;

f_{OSC} = switching frequency (1.2MHz typ.);

L = inductor value.

The minimum inductance value is given by:

$$L > \frac{V_{IN(MIN)} \bullet (V_{OUT(MAX)} - V_{IN(MIN)})}{Ripple \bullet V_{OUT(MAX)} \bullet f_{osc}}$$

where:

Ripple = Allowable inductor current ripple (amps peak-peak)

$V_{IN(MIN)}$ = Minimum input voltage

$V_{OUT(MAX)}$ = Maximum output voltage

The inductor current ripple is typically set for 20% to 40% of the maximum inductor current (I_P). High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low ESR (series resistance of the windings) to reduce the I^2R power losses, and must be able to handle the peak inductor current without saturating. Molded chokes and some chip inductors usually do not have enough core to support the peak inductor currents of 1.2A seen on the CE8406. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor. See Table 2 for some suggested components and suppliers.

Table2. Representative SMD Inductors

Part Number	Value (μH)	Max DCR (mΩ)	Rated DC Current (A)	Size L×W×H (mm^3)
Sumida CDRH	3.3	85	1.10	3.8×3.8×1.8
	4.7	105	0.90	

3D16	6.8 10	170 210	0.73 0.55	
Sumida CR43	3.3 4.7 6.8 10	86.2 108.7 131.2 182	1.44 1.15 0.95 1.04	4.8×4.3×3.5
Sumida CDRH 4D18	3.3 4.7 6.8 10	110 162 200 200	1.04 0.84 0.76 0.61	5.0×5.0×2.0

Different core materials and shapes will change the size/current and price/current relationship of an inductor. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements than on what the CE8406 requires to operate. Table 2 shows some typical surface mount inductors that work well in CE8406 applications.

Output and Input Capacitor Selection

Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 4.7μF to 15μF output capacitor with 10V voltage rating is sufficient for most applications. Larger values up to 22μF may be used to obtain extremely low output voltage ripple and improve transient response. An additional phase lead capacitor may be required with output capacitors larger than 10μF to maintain acceptable phase margin. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges.

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 10μF input capacitor with 10V voltage rating is sufficient for virtually any application. Larger values may be used without limitations.

Table 3 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers directly for detailed information on their entire selection of ceramic capacitors.

Table 3. Capacitor Vendor Information

SUPPLIER	WEBSITE
TDK	www.tdk.com
AVX	www.avxcorp.com
Murata	www.murata.com

Applications Where V_{OUT} > 4.3V

When the output voltage is programmed above 4.3V, it is necessary to add a Schottky diode either from SW to V_{OUT}, or to add a snubber network in order to maintain an acceptable peak voltage on the SW pin. The Schottky diode between SW and V_{OUT} will provide a peak efficiency improvement but will negate the output disconnect feature. If output disconnect is required, an active snubber network is suggested as shown below. Examples of Schottky diodes are: MBR0520L, PMEG2010EA, 1N5817 or equivalent.

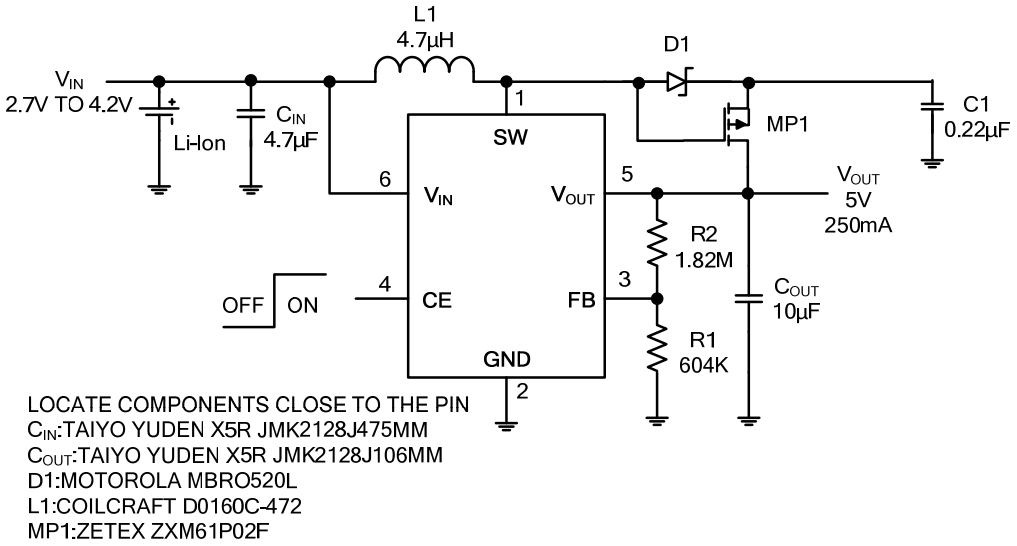


Figure 15. Application Circuit for V_{OUT} > 4.3V Where Inrush Current Limiting and Output Disconnect are Required

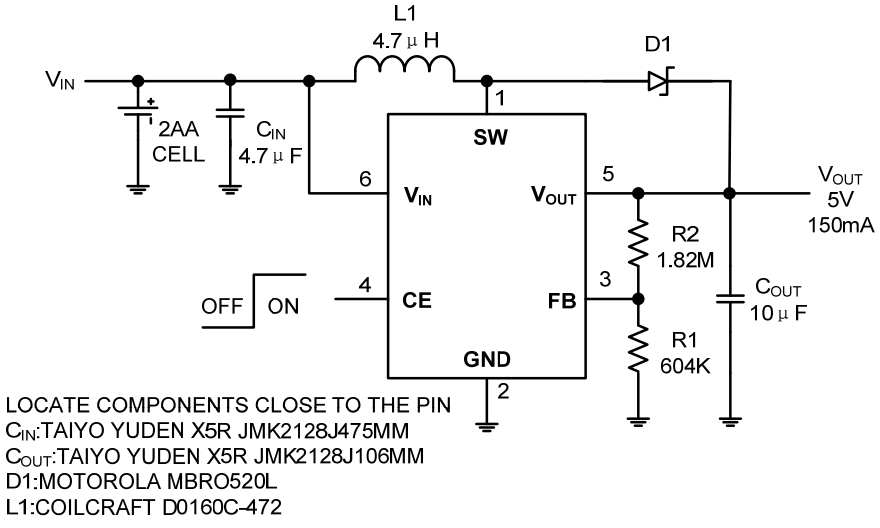


Figure 16. Application Circuit for V_{OUT} > 4.3V Where Inrush Current Limiting and Output Disconnect are Not Required

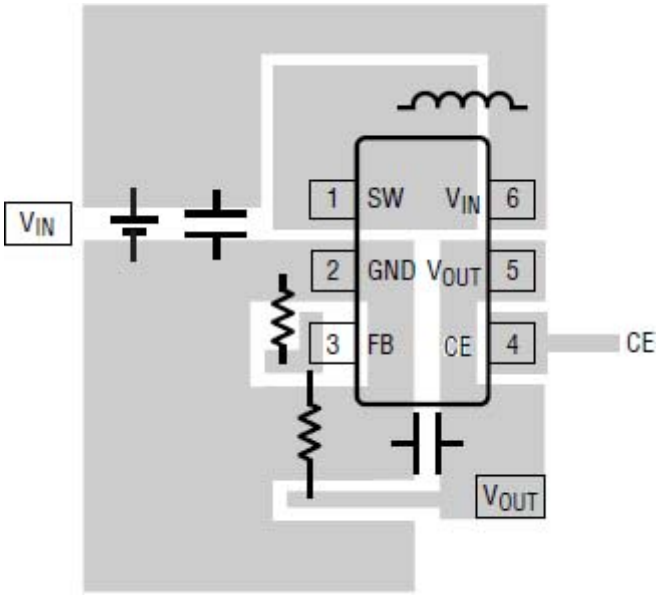
PCB LAYOUT CONSIDERATIONS

The high speed operation of the CE8406 demands careful attention to board layout. You will not get advertised performance with careless layout.

In the CE8406 boost regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the filter inductor, to the SW pin, to the internal NMOS switch, to the ground and back to the input capacitor, when the main switch turns on. The second loop starts from input capacitor, to the filter inductor, to the SW pin, to the internal PMOS switch, to the V_{OUT} pin, to the ground and back to the input capacitor, when the main switch is off(while the synchronous switch is on).

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency.

Figure 17 shows the recommended component placement.



RECOMMENDED COMPONENT PLACEMENT. TRACES CARRYING HIGH CURRENT ARE DIRECT. TRACE AREA AT FB PIN IS SMALL. LEAD LENGTH TO BATTERY IS SHORT

Figure 17. Recommended Component Placement for Single Layer Board

For the best electric and thermal performance, the following suggestions should be taken. These items are also illustrated graphically in Figure 17.

1) The GND pin of the IC is the ground connection for high-current power converter node. High current return for the low-side driver and power N-MOSFET. Connect GND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors. It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. A multilayer board with a separate ground plane is ideal, but not absolutely necessary.

2) Place the (+) plate of C_{IN} near V_{IN} as closely as possible and the loop area formed by C_{IN} and GND must be minimized to maintain input voltage steady and filter out the pulsing input current. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN}, close to the V_{IN}, to shunt any high frequency noise to ground.
3) The output capacitor, C_{OUT}, should be placed as closely as possible to the V_{OUT} pin. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple. For additional output voltage filtering, a low ESR ceramic bypass capacitor can be placed in parallel with C_{OUT}, to shunt any high frequency noise to ground. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{OUT} pin, and the CE8406 GND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{OUT} pin.
4) The GND of the IC, the (-) plate of C_{IN} and C_{OUT} should be connected as closely as possible, together directly to a ground plane.
5) Make the current trace from IN to inductor to SW pin (when internal main NMOS turn on) as short as possible to reduce power dissipation and increase overall efficiency. Also the current trace from IN to inductor to SW pin and the current trace from V_{OUT} pin to C_{OUT} to GND (when internal synchronous PMOS turn on) should be as short as possible. Put enough multiply-layer pads when they need to change the trace layer.
6) The PCB copper area associated with SW、inductor switching node must be minimized to reduce EMI and avoid the potential noise problem.
7) The feedback network, resistors R1 and R2 must be connected to FB pin directly as closely as possible. And FB is a sensitive signal node, trace area at FB pin should be small, please keep it away from SW、 inductor switching node on the PCB layout to avoid the noise inject into the system.
8) If the system chip interfacing with the CE pin has a high impedance state at shutdown mode and the V_{IN} is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the CE and GND pins to prevent the noise from falsely turning on the boost regulator at shutdown mode.
9) Pour copper plane on all unused board area and connect it to stable DC nodes, like V_{IN}, ground or V_{OUT}.

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance follow.

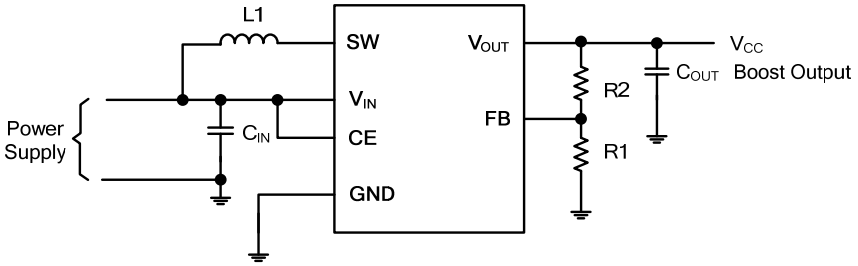
- Improving the power dissipation capability of the PCB design

- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the CE8406 devices is 125°C. The thermal resistance of the 6-pin thin SOT-23 package is θ_{JA}=250°C/W. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 308mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)}=\frac{(T_{J(MAX)}-T_A)}{\theta_{JA}}=\frac{125°C-85°C}{250°C/W}=160mW$$

APPLICATION EXAMPLES



List of Components:

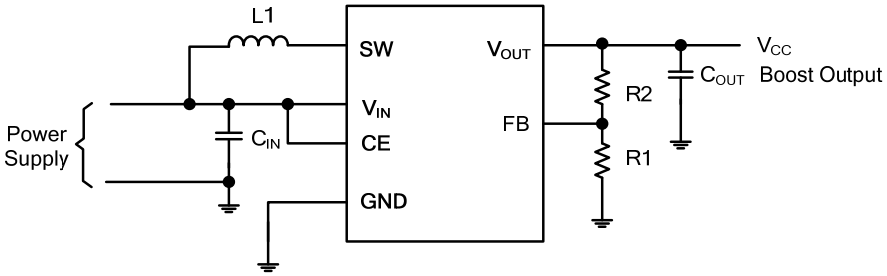
U1 = CE8406AE

L1 = 4.7μH Wurth Elektronik 744031004

C_{IN} = 2 x 4.7μF, 0603, X7R/X5R Ceramic

C_{OUT} = 2 x 4.7μF, 0603, X7R/X5R Ceramic

Figure18. Power Supply Solution for Maximum Output Power Operating from a Single or Dual Alkaline Cell



List of Components:

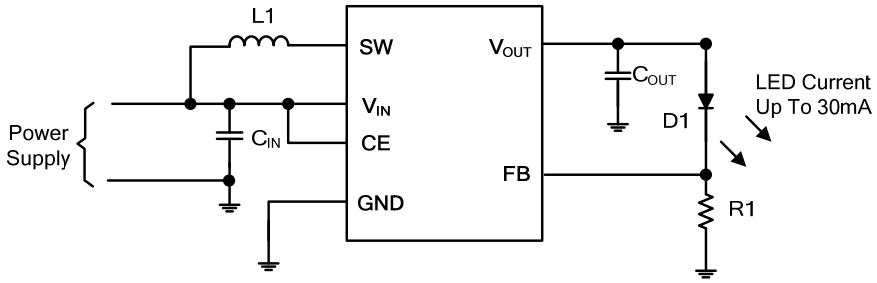
U1 = CE8406AE

L1 = 4.7μH Taiyo Yuden CB2016B4R7M

C_{IN} = 1 x 4.7μF, 0603, X7R/X5R Ceramic

C_{OUT} = 2 x 4.7μF, 0603, X7R/X5R Ceramic

Figure 19. Power Supply Solution Having Small Total Solution Size



List of Components:

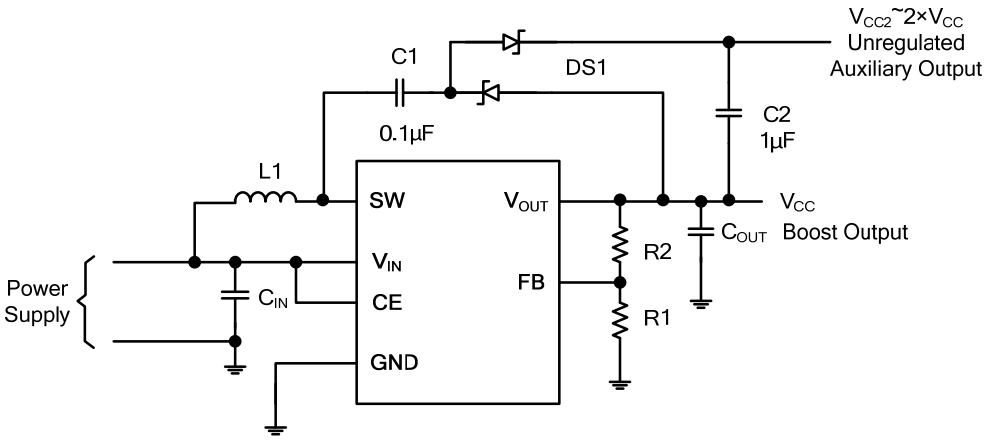
U1 = CE8406AE

L1 = 4.7μH Taiyo Yuden CB2016B4R7M

C_{IN} = 1 x 4.7μF, 0603, X7R/X5R Ceramic

C_{OUT} = 2 x 4.7μF, 0603, X7R/X5R Ceramic

Figure 20. Power Supply Solution for Powering White LEDs in Lighting Applications



List of Components:

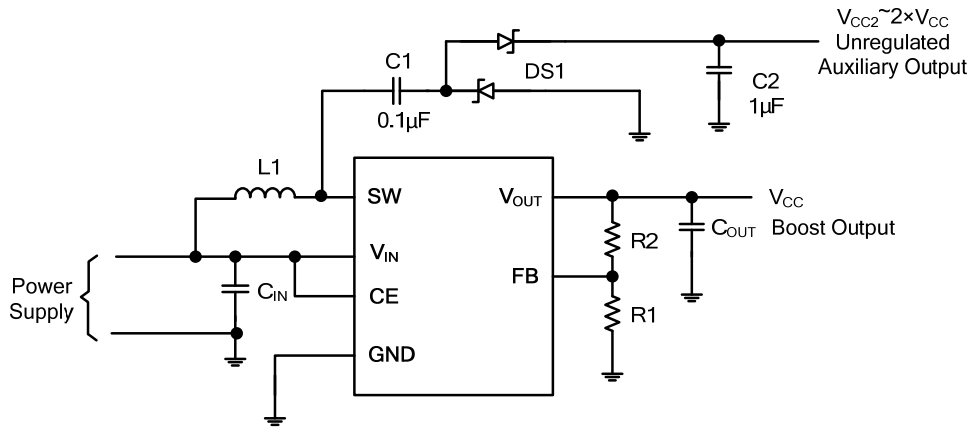
U1 = CE8406AE

L1 = 4.7μH Wurth Elektronik 744031004

C_{IN} = 2 x 4.7μF, 0603, X7R/X5R Ceramic

C_{OUT} = 2 x 4.7μF, 0603, X7R/X5R Ceramic

Figure 21. Power Supply Solution With Auxiliary Positive Output Voltage



List of Components:

U1 = CE8406AE

L1 = 4.7μH Wurth Elektronik 744031004

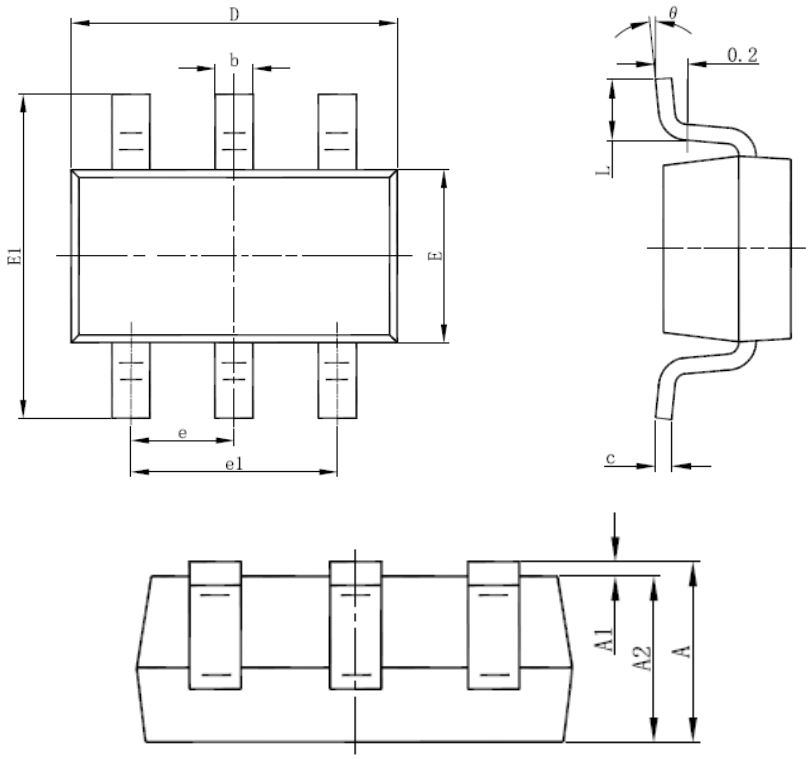
C_{IN} = 2 x 4.7μF, 0603, X7R/X5R Ceramic

C_{OUT} = 2 x 4.7μF, 0603, X7R/X5R Ceramic

Figure 22. Power Supply Solution With Auxiliary Negative Output Voltage

■ PACKAGING INFORMATION

■ SOT-23-6 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°