

■ INTRODUCTION:

The CE9401 provides a constant current drive for 1W or 3W LED applications. It is a high efficiency boost converter that operates from 1 or 2 NiMH or alkaline cells and generates 350mA/1A of constant current with up to 4V of compliance. The LED current can be programmed by the external current sense resistor, R_{SET} , connected between the feedback pin (FB) and ground. A low 95mV feedback voltage reduces the power loss in the R_{SET} for better efficiency. With its internal 2A, 100mΩ NMOS switch, the device can provide high efficiency even at heavy load. The device switches at a 1MHz constant frequency, allowing for the use of small value external inductor and ceramic capacitors.

The CE9401 limits the output voltage to 5.1V if the output load is disconnected. The feedback loop is internally compensated to minimize component count.

The CE9401 is available in the 6-lead SOT-23-6, 8-SOP-PP, and 3mm x 3mm DFN10 package.

■ FEATURES:

- 350mA/1A Constant Current Output
- 2.8V to 4V Output Compliance
- 1- or 2-Cell NiMH or Alkaline Input
- Low $R_{DS(ON)}$: 100mΩ (Typ.)
- 95mV Feedback Voltage
- 1MHz Switching Frequency
- Uses small, Low Profile External Components
- Ceramic Capacitor Compatible
- LED Power Efficiency: up to 90%
- Current Accuracy: 5%
($V_{IN}=3.6V$ to $1.8V @ V_F=3.7V$)
- Low Start-Up Voltage: 0.9V($I_{LED} = 270mA$)
- Low Hold Voltage: 0.75V($I_{LED} = 200mA$)
- Open LED Output Limited to 5.1V
- Over-Current Protection
- Over Temperature Protection
- Pb-Free Package

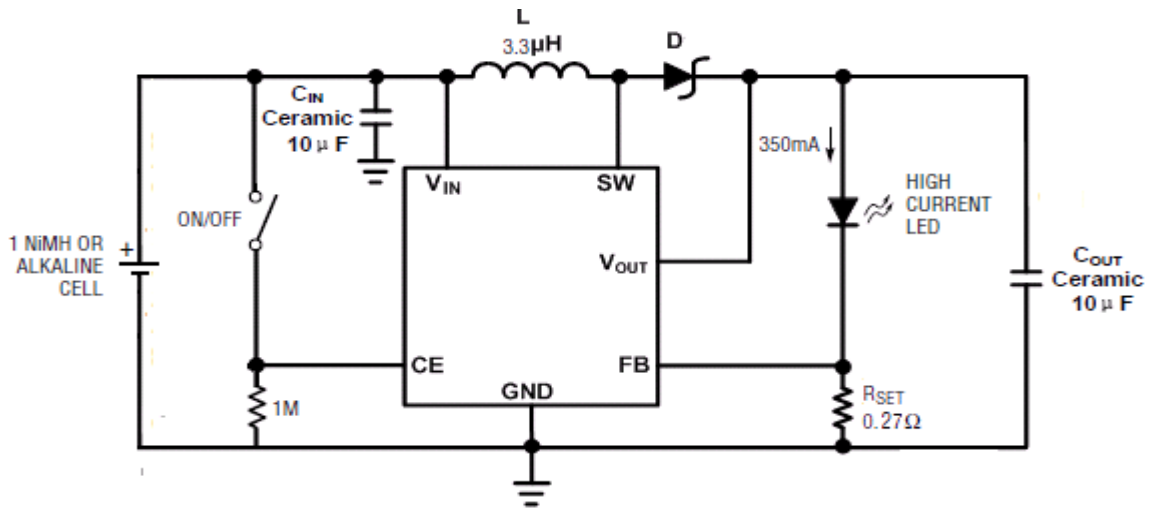
■ APPLICATIONS:

- Portable Lighting
- Rechargeable Flashlight

■ ORDER INFORMATION

Operating free air temperature range	Package	Device No.
-40~+85°C	SOT-23-6	CE9401AE
-40~+85°C	SOP8-PP	CE9401AES
-40~+85°C	DFN3X3-10	CE9401AFC10

■ TYPICAL APPLICATION CIRCUITS



R_{SET} Resistor Value Selection:

TYP. (mΩ)	I _{LED} (mA)
127	750
270	351.8

CS05FTGR127N(0805, 1%, TCR300,127 mΩ)

CS05FTGR270(0805, 1%, TCR300,270 mΩ)

Figure1. Single Cell Minimum Component LED Driver

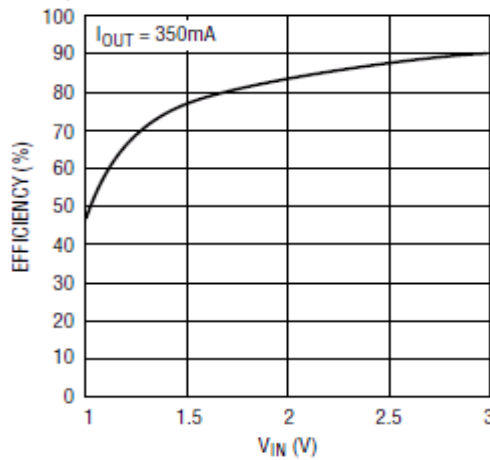
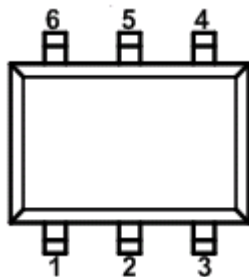
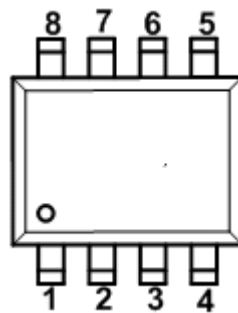


Figure 2. Efficiency vs V_{IN} at V_{LED}=3.5V

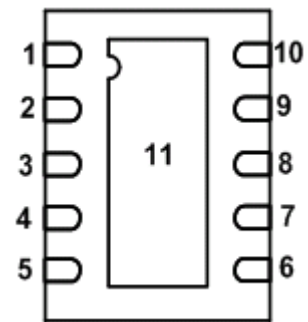
■ PIN CONFIGURATION:



SOT-23-6 Top View



SOP8-PP Top View



DFN3X3-10 Top View

SOT-23-6

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	SW	I	<p>Switch Pin. Connect inductor between SW and V_{IN}. A Schottky diode is connected between SW and V_{OUT}. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.</p>
2	GND	P	<p>Signal and Power Ground. Connect GND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors.. This pin should be connected to a continuous PCB ground for high-current power converter as close as to the device by several vias directly under the CE9401AE for electrical contact and rated thermal performance. It dissipates the heat from the IC.</p>
3	FB	I	<p>Feedback Input. Feedback Input to the gm Error Amplifier. Reference voltage is 95mV. Connect LEDs and a resistor at this pin. LED current is determined by the resistance: $I_{LED} = 95mV / R_{SET}$ The feedback network should be connected directly to a dedicated ground plane and this ground plane must connect to the GND pin. If no ground plane is available, then the ground connection of the feedback network must tie directly to the GND pin. The feedback network should be kept close to the FB pin, and away from the inductor, SW, inductor and Schottky diode switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.</p>
4	CE	I	<p>Chip Enable. CE = High: Normal free running operation CE = Low: Shutdown, quiescent current < 1μA. Typically, CE should be connected to V_{IN} through a 1M pull-up resistor.</p>
5	V _{OUT}	I	<p>Chip Supply Voltage and Output Voltage Sense Input. The V_{OUT} pin should be connected to the negative terminal of the schottky diode and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{OUT} pin, and the CE9401AE GND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{OUT} pin and the GND pin.</p>
6	V _{IN}	I	<p>Internal Supply Voltage Input. The V_{IN} pin should be connected to the positive terminal of the input capacitor and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{IN} pin, and the CE9401AE GND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{IN} pin and the GND pin.</p>

(1) I = input; O = output; P = power

SOP8-PP

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	AGND	I	Analog Ground. The analog ground ties to all of the noise sensitive signals. Provide a clean ground for the analog control circuitry and should not be in the path of large currents.
2	FB	I	Feedback Input. Feedback Input to the gm Error Amplifier. Reference voltage is 95mV. Connect LEDs and a resistor at this pin. LED current is determined by the resistance: $I_{LED} = 95mV/R_{SET}$ The ground connection of the feedback network must tie directly to the PGND pin. The feedback network should be kept close to the FB pin, and away from the inductor, SW, inductor and Schottky diode switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.
3	NC		Not Connect.
4	SW	I	Switch Pin. Connect inductor between SW and V _{IN} . A Schottky diode is connected between SW and V _{OUT} . Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.
5	PGND	P	Power Ground. Ground connection for high-current power converter node. High current return for the low-side driver and power N-MOSFET. Connect PGND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors. Only connect to AGND through the Exposed Pad underneath the IC.
6	V _{IN}	I	Internal Supply Voltage Input. The V _{IN} pin should be connected to the positive terminal of the input capacitor and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V _{IN} pin, and the CE9401AES AGND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V _{IN} pin and the AGND pin.
7	V _{OUT}	I	Chip Supply Voltage and Output Voltage Sense Input. The V _{OUT} pin should be connected to the negative terminal of the schottky diode and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V _{OUT} pin, and the CE9401AES AGND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V _{OUT} pin and the AGND pin.
8	CE	I	Chip Enable. CE = High: Normal free running operation CE = Low: Shutdown, quiescent current < 1μA. Typically, CE should be connected to V _{IN} through a 1M pull-up resistor.
9	EP	P	Exposed Paddle (bottom). This pin should be connected to a continuous analog ground plane as close as to the device by several vias directly under the CE9401AES for electrical contact and rated thermal performance. It dissipates the heat from the IC.

(1) I = input; O = output; P = power

DFN3X3-10

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	FB	I	<p>Feedback Input. Feedback Input to the gm Error Amplifier. Reference voltage is 95mV. Connect LEDs and a resistor at this pin. LED current is determined by the resistance:</p> $I_{LED} = 95mV/R_S$ <p>The ground connection of the feedback network must tie directly to the PGND pin. The feedback network should be kept close to the FB pin, and away from the inductor, SW, inductor and Schottky diode switching node on the PCB layout to minimize copper trace connections that can inject noise into the system.</p>
2/3/4	NC		Not Connect.
5	SW	I	<p>Switch Pin. Connect inductor between SW and V_{IN}. A Schottky diode is connected between SW and V_{OUT}. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage overshoot.</p>
6	PGND	P	<p>Power Ground. Ground connection for high-current power converter node. High current return for the low-side driver and power N-MOSFET. Connect PGND with large copper areas directly to the input and output supply returns and negative terminals of the input and output capacitors. Only connect to AGND through the Exposed Pad underneath the IC.</p>
7	V _{IN}	I	<p>Internal Supply Voltage Input. The V_{IN} pin should be connected to the positive terminal of the input capacitor and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{IN} pin, and the CE9401AFC10 AGND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{IN} pin and the AGND pin.</p>
8	AGND	I	<p>Analog Ground. The analog ground ties to all of the noise sensitive signals. Provide a clean ground for the analog control circuitry and should not be in the path of large currents.</p>
9	V _{OUT}	I	<p>Chip Supply Voltage and Output Voltage Sense Input. The V_{OUT} pin should be connected to the negative terminal of the schottky diode and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the V_{OUT} pin, and the CE9401AFC10 AGND pin. The minimum recommended bypass capacitance is 100nF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the V_{OUT} pin and the AGND pin.</p>
10	CE	I	<p>Chip Enable. CE = High: Normal free running operation CE = Low: Shutdown, quiescent current < 1μA. Typically, CE should be connected to V_{IN} through a 1M pull-up resistor.</p>
11	EP	P	<p>Exposed Paddle (bottom). This pin should be connected to a continuous analog ground plane as close as to the device by several vias directly under the CE9401AFC10 for electrical contact and rated thermal performance. It dissipates the heat from the IC.</p>

(1) I = input; O = output; P = power

■ ABSOLUTE MAXIMUM RATINGS

(Unless otherwise specified, $T_{opr}=25^{\circ}\text{C}$)⁽¹⁾

PARAMETER		SYMBOL	RATINGS	UNITS
Output Voltage range ⁽²⁾		V_{IN}	$V_{SS}-0.3\sim V_{SS}+7$	V
Voltage range on V_{OUT} , CE, SW, FB pins ⁽²⁾			$V_{SS}-0.3\sim V_{OUT}+0.3$	V
Peak SW Sink Current		I_{SWMAX}	3	A
Power Dissipation	SOT-23-6	P_d	400	mW
	SOP8-PP		1200	
	DFN3x3-10		2200	
Operating free air temperature range ⁽³⁾		T_{opr}	-40~+85	$^{\circ}\text{C}$
Junction Temperature		T_j	150	$^{\circ}\text{C}$
Storage Temperature		T_{stg}	-40~+125	$^{\circ}\text{C}$
Soldering Temperature & Time		T_{solder}	260 $^{\circ}\text{C}$, 10s	
ESD rating ⁽⁴⁾		Human Body Model - (HBM)	2	kV
		Machine Model- (MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) The CE9401 is guaranteed to meet performance specifications from 0 $^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$. Specifications over the -40 $^{\circ}\text{C}$ to 85 $^{\circ}\text{C}$ range are assured by design, characterization and correlation with statistical process controls.

(4) ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5k Ω resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

■ RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNITS
Supply voltage at V_{IN}	1.0		3.2	V
Output voltage at V_{OUT}	2.8		4.0	V
Operating free air temperature range, T_{opr}	0		85	$^{\circ}\text{C}$
Operating junction temperature range, T_j	-40		125	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS

Typical values are at $T_{opr}=25^{\circ}\text{C}$, unless otherwise specified, specifications apply for condition $V_{IN}=2.4\text{ V}$, $I_{LED}=750\text{ mA}$, $V_{CE}=2.4\text{ V}$, $L=2.2\mu\text{H}$, $C_{IN}=10\mu\text{F}$, $C_{OUT}=10\mu\text{F}$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNITS
SUPPLY						
Input Voltage Range	V_{IN}		0.9		3.2	V
Minimum Start-Up Voltage ⁽²⁾	V_{START}	$V_{IN}: 0\text{V}\rightarrow 3\text{V}$, $I_{LED}=270\text{mA}$		0.9		V
Operating quiescent current into V_{OUT}	I_Q	Measured On V_{OUT} , $V_{OUT}=3.4\text{V}$, $I_{LED}=0\text{mA}$, $V_{FB}=130\text{mV}$, Device Not Switching		130	300	μA
Shutdown Current into V_{IN}	$I_{SHDNVIN}$	$V_{CE}=\text{GND}$		0.1	1	μA
LOGIC SIGNAL CE						
CE High-level Voltage	V_{CEH}^*	$V_{IN}=1.8\text{V}$, V_{CE} Rising, Device ON	1.5		V_{IN}	V
CE Low-level Voltage	V_{CEL}^*	$V_{IN}=1.8\text{V}$, V_{CE} Falling, Device Off			0.4	V
CE Leakage Current	I_{CE}	$V_{CE}=5.0\text{V}$		± 0.1	± 1	μA
OSCILLATOR						
Oscillator Frequency	f_{osc}			1.0		MHz
Max Duty Cycle	D_{MAX}	$V_{FB}=\text{GND}$	80	87		%
POWER SWITCH						
N-CH MOSFET On Resistance ⁽³⁾	$R_{DS(ON)}$	$V_{OUT}=3.4\text{V}$		100		m Ω
N-CH MOSFET Switch Leakage	I_{SWLEAK}	$V_{CE}=\text{GND}$, $V_{SW}=5.0\text{V}$		± 0.01	± 1	μA
NMOS Cycle by Cycle Current Limit ⁽⁴⁾	I_{CL}	$V_{OUT}=3.4\text{V}$	2.0	3.0		A
OUTPUT						
Output Compliance Voltage Range	V_{OUT}		2.8		4.0	V
Output Voltage Overvoltage Limit	$V_{OUT(OVL)}$	Open LED		5.1	5.5	V
Feedback regulation voltage	V_{FB}		90	95	100	mV
Feedback Input bias Current ⁽⁵⁾	I_{FB}	$V_{FB}=130\text{mV}$			0.1	μA
Maximum Output Current Range	$I_{OUT(MAX)}$		750			mA
Efficiency	η	$I_{LED}=750\text{mA}$		90		%
OVER TEMPERATURE PROTECTION						
Thermal Shutdown	T_{TSD}			140		$^{\circ}\text{C}$
Thermal Shutdown Hysteresis	T_{TSDHYS}			20		$^{\circ}\text{C}$

(1) Typical numbers are at 25°C and represent the most likely norm.

(2) The CE9401 input voltage may drop below the minimum start-up voltage once the V_{OUT} voltage has risen above 2.3V.

(3) Does not include the bond wires. Measured directly at the die.

(4) Duty cycle affects current limit due to ramp generator.

(5) Bias current flows into FB pin. Specification is guaranteed by design and not 100% tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

($T_{opr}=25^{\circ}C$, unless otherwise specified, Test Figure1 above)

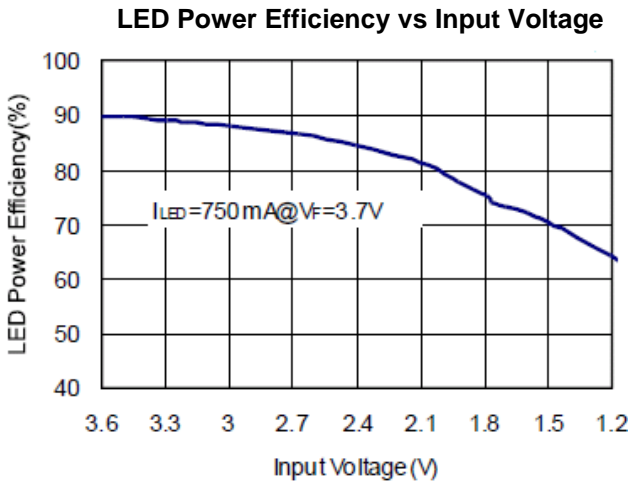


Figure 3

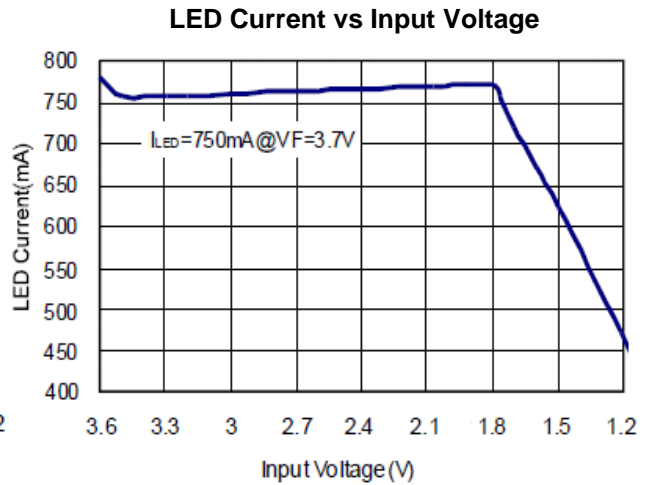


Figure 4

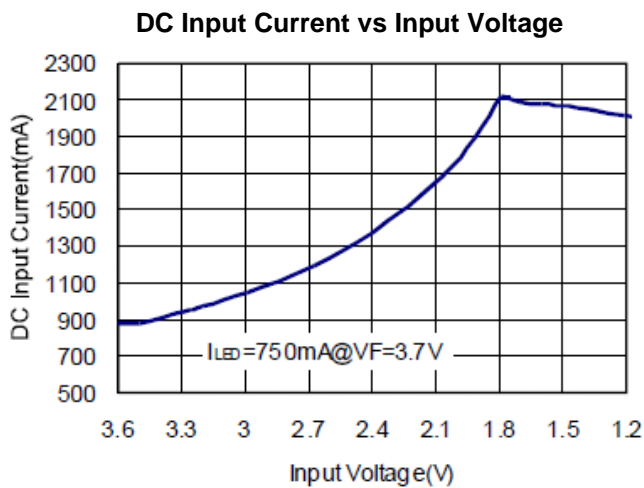


Figure 5

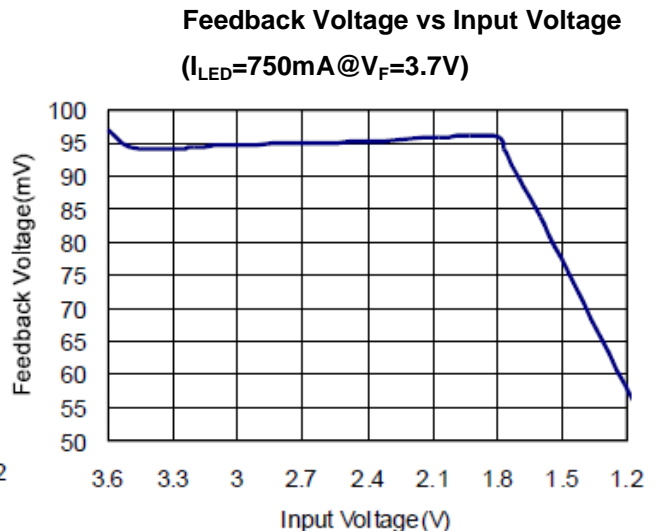


Figure 6

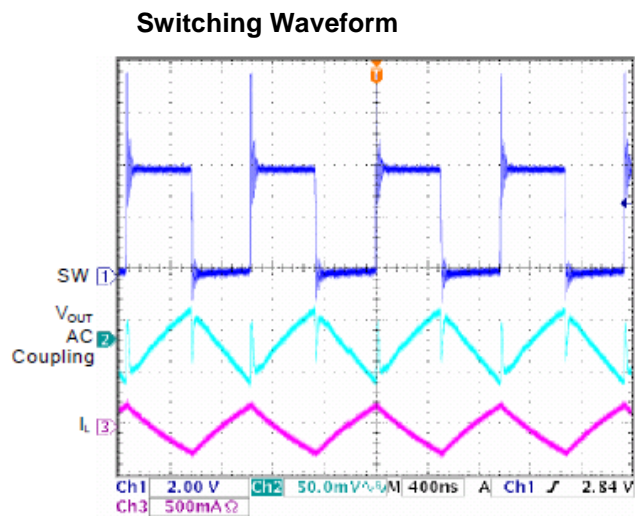


Figure 7

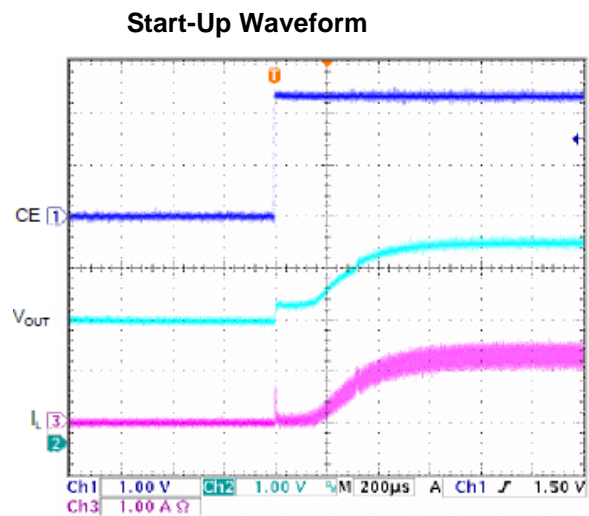


Figure 8

■ OPERATION

The CE9401 is a high efficiency, constant current source for 1W or 3W high intensity white LEDs. These high intensity LEDs require a fixed current of 350mA or 750mA with a voltage compliance of 2.8V to 4V.

The CE9401 operates with 1 or 2 NiMH or alkaline cells. It functions as a boost converter with a current sense resistor providing the control feedback. It features a low voltage start-up circuit that will start with an input voltage of only 0.9V. Once the drive voltage exceeds 2.3V, the circuit operates from the drive voltage.

All of the loop compensation is internal; only the main filter capacitor is needed for stable operation.

LED Current Setting

The LED current is set by the single external R_{SET} resistor connected to the FB pin as shown in the typical application circuit on page 2. The typical FB reference is internally regulated to 95mV. The LED current is 95mV/R_S. It's recommended to use a 1% or better precision resistor for the better LED current accuracy. Table 1 shows several typical 1% R_{SET} values. For other LED current values, use the following equation to choose R_{SET}:

$$R_{SET} = 95mV / I_{LED} \tag{1}$$

Table 1. R_{SET} Resistor Value Selection

I _{LED} (mA)	R _{SET} Value
528	0.18
633	0.15
792	0.12
950	0.10

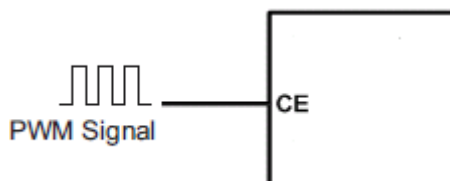
Dimming Control

The LED illumination level can be controlled using both digital and analog methods.

There are four different types of dimming control circuits:

1. Using a PWM Signal to CE Pin

PWM brightness control provides the widest dimming range (greater than 20:1). With the PWM signal applied to the CE pin, the CE9401 is turned on or off by the PWM signal. The LEDs operate at either zero or full current. The average LED current increases proportionally with the duty cycle of the PWM signal. A 0% duty cycle will turn off the CE9401 and corresponds to zero LED current. A 100% duty cycle corresponds to full current. The PWM signal frequency should be set below 1KHz due to the delay time of device startup. The magnitude of the PWM signal should be higher than the minimum CE voltage high. The switching waveforms of the CE pin PWM control are shown in Figures 9.



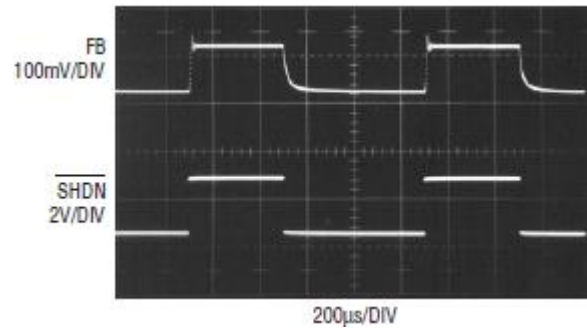


Figure 9. PWM Dimming Control Using the CE Pin ($f_{PWM}=1\text{KHz}$)

2. Using a DC Voltage

For some applications, the preferred method of brightness control is a variable DC voltage to adjust the LED current. The dimming control using a DC voltage is shown in Figure 10.

As the DC voltage increases, the voltage drop on R2 increases and the voltage drop on R_{SET} decreases. Thus, the LED current decreases. When the DC control voltage is at the maximum DC control voltage V_{MAX}, the LED current decreases to the minimum value of I_{LED}, I_{LED(MIN)}. While the maximum value of I_{LED}, I_{LED(MAX)} is the current programmed by R_{SET}.

The selection of R2 and R_{ADJ} will make the current from the variable DC source much smaller than the LED current and much larger than the FB pin bias current. For V_{DC} range from 0V to 2V, the selection of resistors in Figure 10 gives dimming control of LED current from 0mA to 350mA.

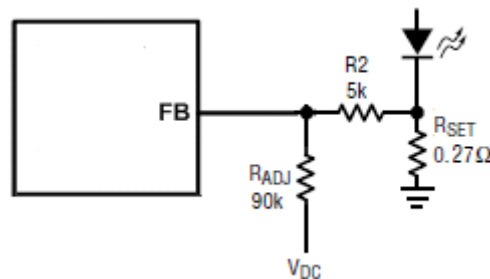


Figure 10. Dimming Control Using a DC Voltage

3. Using a Filtered PWM Signal

While the direct PWM method provides the widest dimming range and the purest white light output, it causes the CE9401 to enter into PFM Mode operation. This operation may be undesirable for some systems, as it may reflect some noise to the input source at the PWM dimming frequency. The solution is to filter the control signal by adding a 10k resistor and a 0.1µF capacitor as shown in Figure 11, converting the PWM to a DC level before it reaches the R_{SET} pin. The 10k resistor minimizes the capacitance seen by the R_{SET} pin.

The filtered PWM signal can be considered as an adjustable DC voltage. It can be used to replace the variable DC voltage source in dimming control. The circuit is shown in Figure 11.

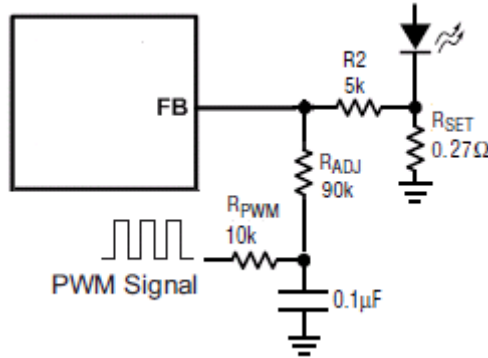


Figure 11. Dimming Control Using a Filtered PWM Signal

4. Using a Logic Signal

For applications that need to adjust the LED current in discrete steps, a logic signal can be used as shown in Figure 12. R_{MIN} sets the minimum LED current (when the NMOS is off). R_{INC} sets how much the LED current increases when the NMOS is turned on. The selection of R_{SET} and R_{INC} follows formula (1) and Table 1.

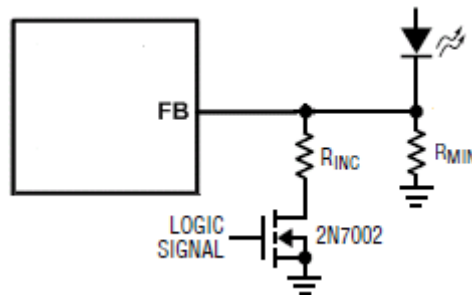


Figure 12. Dimming Control Using a Logic Signal

Start-up and Inrush Current

To achieve minimum start-up delay, no internal soft-start circuit is included in CE9401. When first turned on without an external soft-start circuit, inrush current is about 200mA as shown in Figure 13. If soft-start is desired, the recommended circuit and the waveforms are shown in Figure 14. If both soft-start and dimming are used, a 1kHz PWM signal on CE pin is not recommended. Use a lower frequency or implement dimming through the FB pin as shown in Figures 10, 11 or 12.

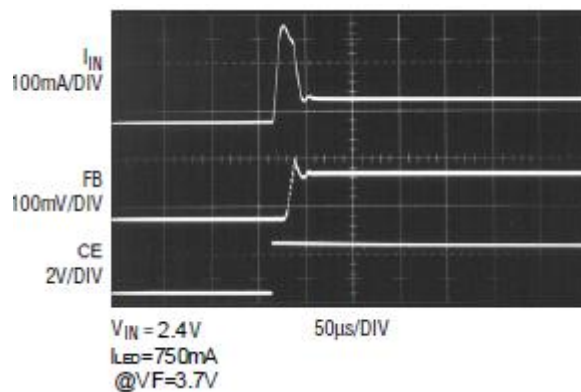
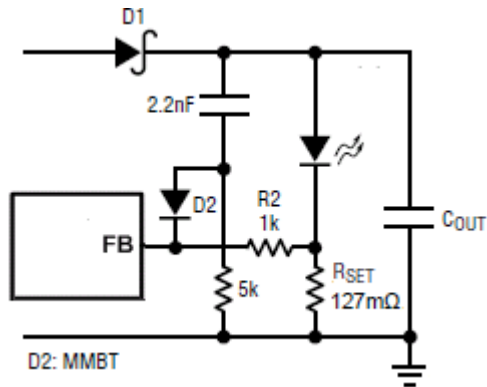
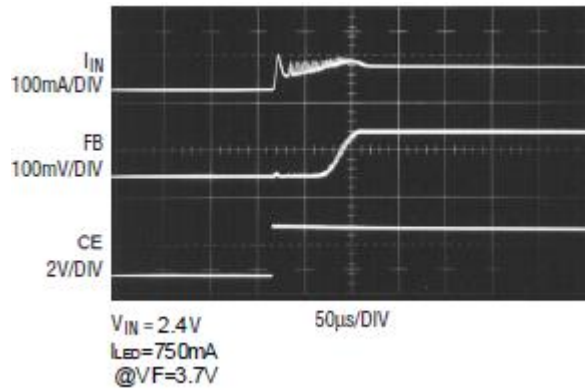


Figure 13. Start-Up Waveforms Without Soft-Startup Circuit



(14a) Recommended Soft-Startup Circuit



(14b) Soft-Startup Waveforms

Figure 14. Recommended Soft-Startup Circuit and Waveforms

Open-Circuit Protection

Since this is a boost converter attempting to drive a current into the load, an open or high impedance load will cause the regulator loop to increase the output voltage in an effort to achieve regulation. To protect the device, output voltage is limited to 5.1V under all conditions.

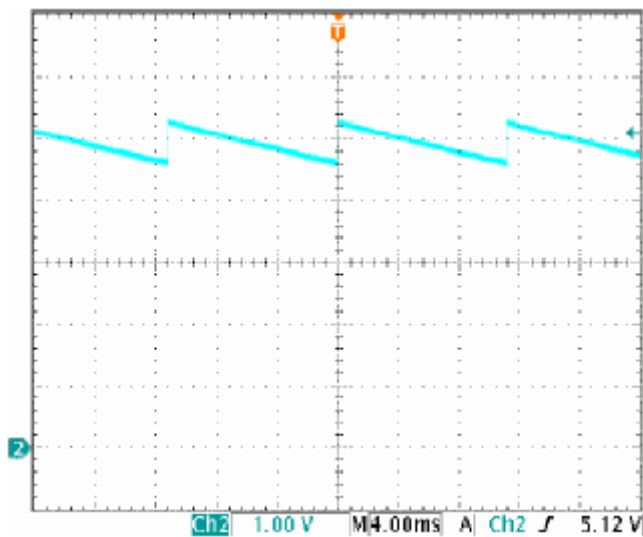


Figure 15. Overvoltage Protection

■ APPLICATION INFORMATION

The CE9401 requires only five external components to operate: an inductor, an output rectifier diode, an output capacitor, a input capacitor and a LED current setting resistor. The inductor is nominally set at 3.3μH and the capacitor at 10μF. Optional components include an input bypass capacitor and dimming resistors.

COMPONENT SELECTION

Inductor Selection

The high frequency operation of the CE9401 allows the use of small surface mount inductors. The minimum inductance value is proportional to the operating frequency and is limited by the following constraints:

$$L \geq \frac{3}{f_{osc}} H$$

$$L \geq \frac{V_{IN(MIN)} * [V_{OUT(MAX)} - V_{IN(MIN)}]}{f_{osc} * \Delta I_{L(peak-peak)} * V_{OUT(MAX)}} H$$

where:

f_{OSC} = Operating Frequency (Hz)

$\Delta I_{L(peak-peak)}$ = Inductor Peak To Peak Current Ripple (A)

$V_{IN(MIN)}$ = Minimum Input Voltage (V)

$V_{OUT(MAX)}$ = Maximum Output Voltage (V)

The inductor peak to peak current ripple is typically set to 20% to 40% of the average inductor current.

The peak inductor current is given by:

$$I_{L,peak} = I_{L,AVG} + \frac{\Delta I_{L(peak-peak)}}{2} = I_{OUT} * \frac{(V_{OUT} + V_{forward} - R_N * I_{IN})}{V_{IN} - R_N * I_{IN}} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2 * L * f_{osc} * V_{OUT}}$$

where:

V_{IN} = Input Voltage (V)

V_{OUT} = Output Voltage (V)

$V_{forward}$ = Output Rectifier Diode Forward Voltage (V)

I_{OUT} = LED Drive Current (A)

I_{IN} = Input Current = $V_{OUT}/V_{IN} \cdot I_{OUT}$ (A)

R_N = $R_{DS(ON)}$ of the NMOSFET Switch (Ω)

For high efficiency, choose an inductor with a high frequency core material, such as ferrite, to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses and must be able to handle the peak inductor current at full load without saturating. In single cell applications, the inductor ESR must be below 25m Ω to keep the efficiency up and maintain output current regulation. Dual cell applications can tolerate significantly higher ESR (up to 75m Ω) with minimal efficiency degradation. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 1A to 2A region. If radiated noise is an issue, use a toroid, pot core or shielded bobbin inductor to minimize radiated noise. See Table 2 for a list of suggested inductors. Look closely at the manufacturers data sheets; they specify saturation current differently.

■ APPLICATION INFORMATION

Table 2. Inductor Information

INDUCTOR PART NUMBER	ESR (mΩ)	SATURATION CURRENT(A)
TOKO A918CY-3R3M	47	1.97
TYCO DN4835-3R3M	58	2.15
TDK SLF7045T-3R3M2R5	20	2.5

Output Rectifier Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The peak diode current can be calculated using the formula:

$$I_{D_peak} = I_{OUT}/(1-D) + \Delta I_{L(peak-peak)}/2$$

In the above equation, I_{OUT} is the LED drive current and $\Delta I_{L(peak-peak)}$ is the inductor peak to peak current ripple .

The output rectifier diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The diode D average rectified forward current I_{D_AVG} rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode must be rated to handle 2A, the switch current limit of the CE9401. The diode must be rated for a reverse breakdown voltage higher than the maximum output voltage used of the converter.

Do not use ordinary rectifier diodes, since the slow recovery time will compromise efficiency.

Schottky diode is a good choice for the rectifier diode to decrease power dissipation and achieve high power LED efficiency, because of its low forward voltage drop and fast reverse recovery time.

It's indispensable to use a Schottky diode rated at 2A with the CE9401.

The Schottky rectifier diode selected has to be able to dissipate the power. The dissipated power, P_{diode_loss} , is the average rectified forward current times the diode forward voltage, $V_{forward}$.

$$P_{diode_loss} = I_{D_AVG} * V_{forward}$$

Table 3. Schottky Rectifier Diode Selection

Rectified Forward Current Rating I_{D_AVG}	Vr	$V_{forward(Max.)}/I_{D_AVG}$	SUPPLIER	COMPONENT CODE
2A	10V	0.35V/2A	ON Semiconductor	MBRA210LT3G
2A	10V	0.46V/2A	NXP	PMEG1020EH
2A	20V	0.44V/2A	Vishay General Semiconductor	SL22
2A	20V	0.5V/2A	Fairchild Semiconductor	SS22
2A	25V	0.44V/2A	ST	STPS2L25

■ APPLICATION INFORMATION

Output Capacitor Selection

The output capacitor value and equivalent series resistance (ESR) are the primary factors in the output ripple. The output ripple is not a direct concern for LED drive as the LED will operate at the average current value. However the peak pulsed forward current rating of the LED must not be exceeded to avoid damaging the LED.

The output ripple voltage has two primary components.

The first is due to the value of the capacitor and is given by:

$$VR_{CAP} = \frac{I_{L_peak} * V_{IN}}{C_{OUT} * V_{OUT} * f_{osc}}$$

The second is due to the capacitor ESR:

$$VR_{CAP_ESR} = I_{L_peak} * R_{CAP_ESR}$$

The LED current ripple and peak pulsed current are calculated by:

$$IR_{LED} = \frac{VR_{CAP} * VR_{CAP_ESR}}{R_{SET} + R_{LED}}$$

$$I_{PPFC} = I_{OUT} + \frac{IR_{LED}}{2}$$

where:

R_{SET} = LED Current Setting Resistor

R_{LED} = Dynamic Impedance of the LED

A reasonable value of the output capacitor depends on the LED current. A minimum output capacitor value of 6.8uF is recommended under normal operating conditions, while a 10uF-22uF capacitor may be required for higher power LED current.

The ESR of the output capacitor is the important parameter to determine the output voltage ripple of the converter, so Low ESR capacitors should be used to minimize output ripple. Ceramic X5R or X7R type capacitors are recommended, because they maintain capacitance over wide voltage and temperature ranges. See Table 4 for a list of component suppliers.

Table 4. Capacitor Information

CAPACITOR PART NUMBER	DESCRIPTION
TDK C2012X5R0J106K	10μF, 6.3V, X5R in 0805
AVX 1210ZC106MAT	10μF, 10V, X7R in 1210
Taiyo Yuden CELMK316BJ106ML	10μF, 10V, X7R in 1206

Input Capacitor Selection

An input capacitor is required to reduce the input ripple and switching noise for proper operation of the CE9401. For good input decoupling, Low ESR (equivalent series resistance) capacitors should be used at the input. At least 3.3uF input capacitor is recommended for most applications.

■ APPLICATION INFORMATION

Design Example

The example will use a Lumileds DS25 white LED. The key specifications are:

$$V_F \text{ (at } I_F = 350\text{mA)} = 3.4 \pm 0.6\text{V}$$

$$R_{LED} = 1\Omega$$

$$\text{Peak Pulsed Forward Current} = 0.5\text{A}$$

Component values will be calculated for 1 or 2 NiMH cells and assumes the end-of-charge voltage to be 0.9V per cell. The operating frequency is assumed to be 1MHz, the typical frequency. The allowed inductor ripple current is 0.31A. Table 5 shows a summary of the key parameters.

Table 5. Summary of Key Parameters

PARAMETER	1-CELL	2-CELL	UNITS
L_{MIN}	2.2	3.2	μH
Choose L	3.3	3.3	μH
I_{IN}	1.56	0.78	A
I_{L_peak}	1.93	0.96	A
Choose C_{OUT}	4.7	4.7	μF
Cap ESR	5	5	m Ω
VR_{CAP}	0.09	0.09	V
VR_{CAP_ESR}	0.01	0.005	V
IR_{LED}	0.10	0.09	A
I_{PPFC}	0.40	0.39	A

where:

I_{L_peak} is the peak inductor current

VR_{CAP} is the ripple voltage due to the output capacitor value

VR_{CAP_ESR} is the ripple voltage due to the output capacitor ESR

IR_{LED} is the LED current ripple

I_{PPFC} is the LED peak pulsed forward current

PCB Layout Checklist

Keep resistance in the battery connections as low as possible. In single cell applications, only 0.1 Ω in the battery connections will have a dramatic effect in efficiency and battery life. I^2R losses can exceed 100mW and the converter operates lower on the efficiency curve.

As for all switching power supplies, the layout and components placement of the CE9401 is an important step in the design; especially at high peak currents and high switching frequencies. The high speed operation of the CE9401 demands careful attention to board layout. You will not get advertised performance with careless layout. Figure 16 shows the recommended component placement. A large ground pin copper area will help to lower the chip temperature.

The input capacitor and output capacitor should be placed respectively as close as possible to the input pin and output pin of the IC; Make traces as short and wide as is feasible. Parasitic resistance and inductance reduce efficiency and increase ripple.

■ APPLICATION INFORMATION

the inductor and schottky diode should be placed as close as possible to the switch pin by using wide and short traces for the main current path; the current sense resistor should be placed as close as possible between the ground pin and feedback pin.

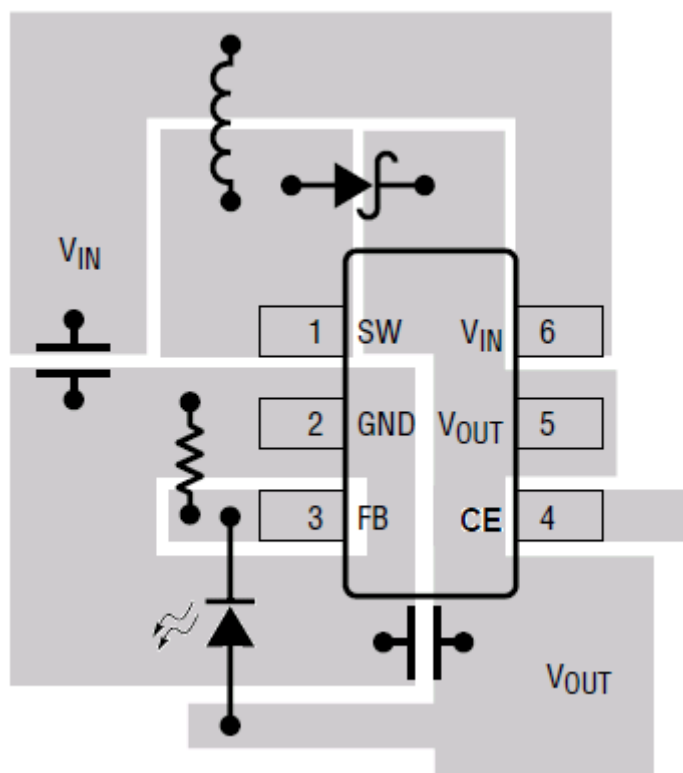


Figure 16. Recommended Component Placement for Single Layer Board

Red Luxeon LEDs

The red, red-orange and amber Luxeon LEDs have a lower forward voltage than the white, blue and green LEDs. Since the CE9401 internal circuitry is powered from the output, it requires a minimum LED voltage of 2.5V for reliable operation. The minimum forward voltage on the red LEDs is only 2.31V. The CE9401 requires an additional 190mV for proper operation. In non-dimming applications, this can be accomplished with a 0.6Ω resistor in series with the LED. The resistor voltage drops too low in dimming applications, so a Schottky diode is recommended to keep sufficient voltage at the output at lower currents.

■ TYPICAL APPLICATIONS

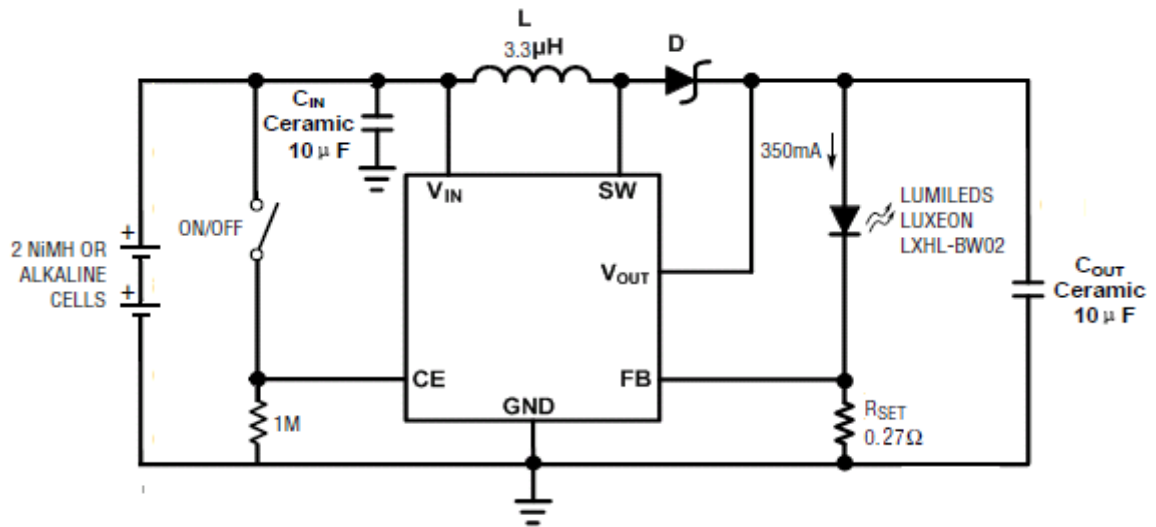


Figure 17. 2-Cell LED Driver

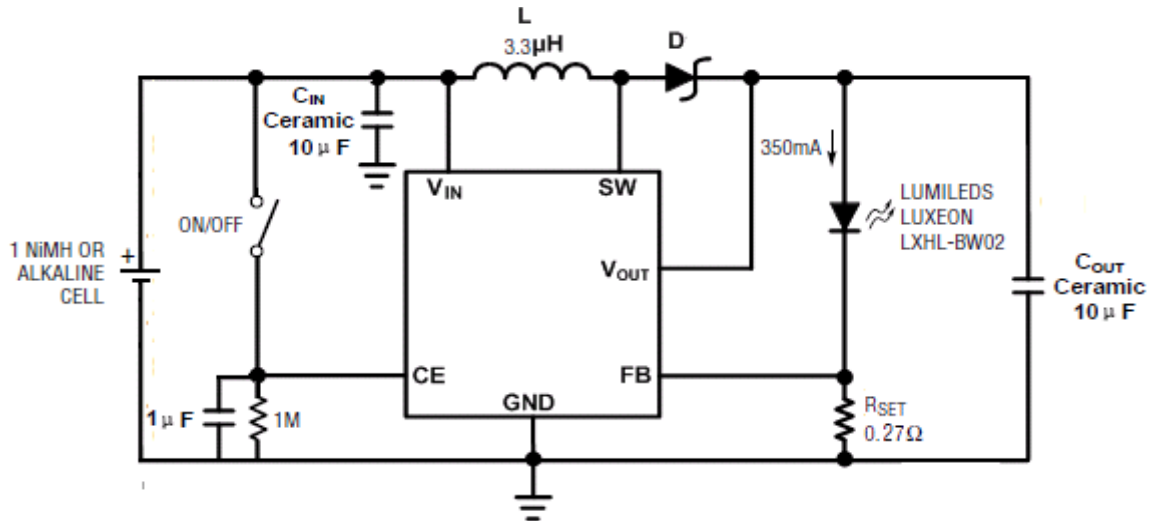


Figure 18. Soft Turn-Off LED Driver

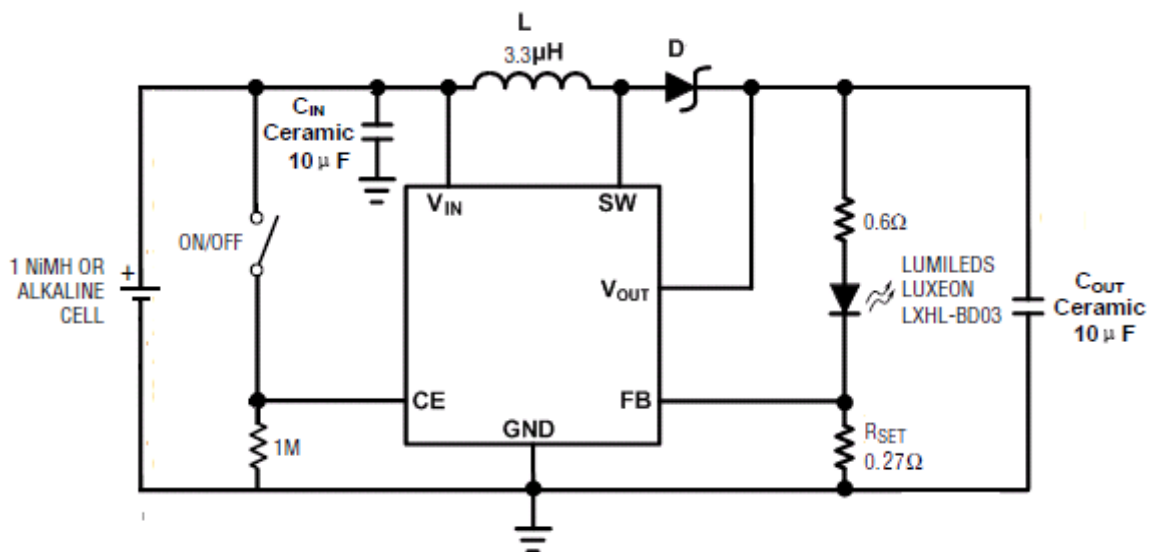


Figure 19. Luxeon Red LED Driver Without Dimming

■ TYPICAL APPLICATIONS

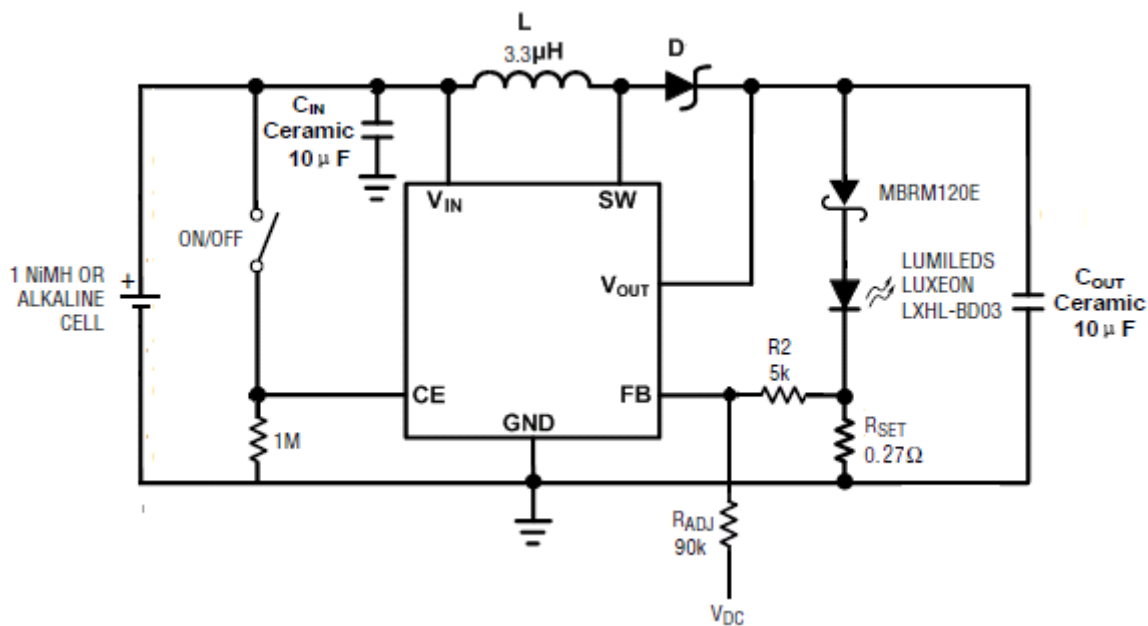


Figure 20. Luxeon Red LED Driver With Dimming

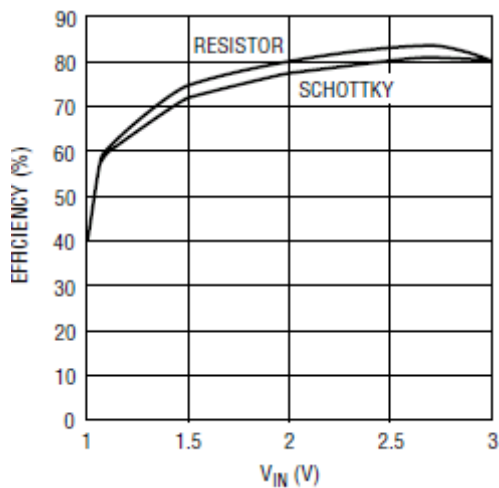
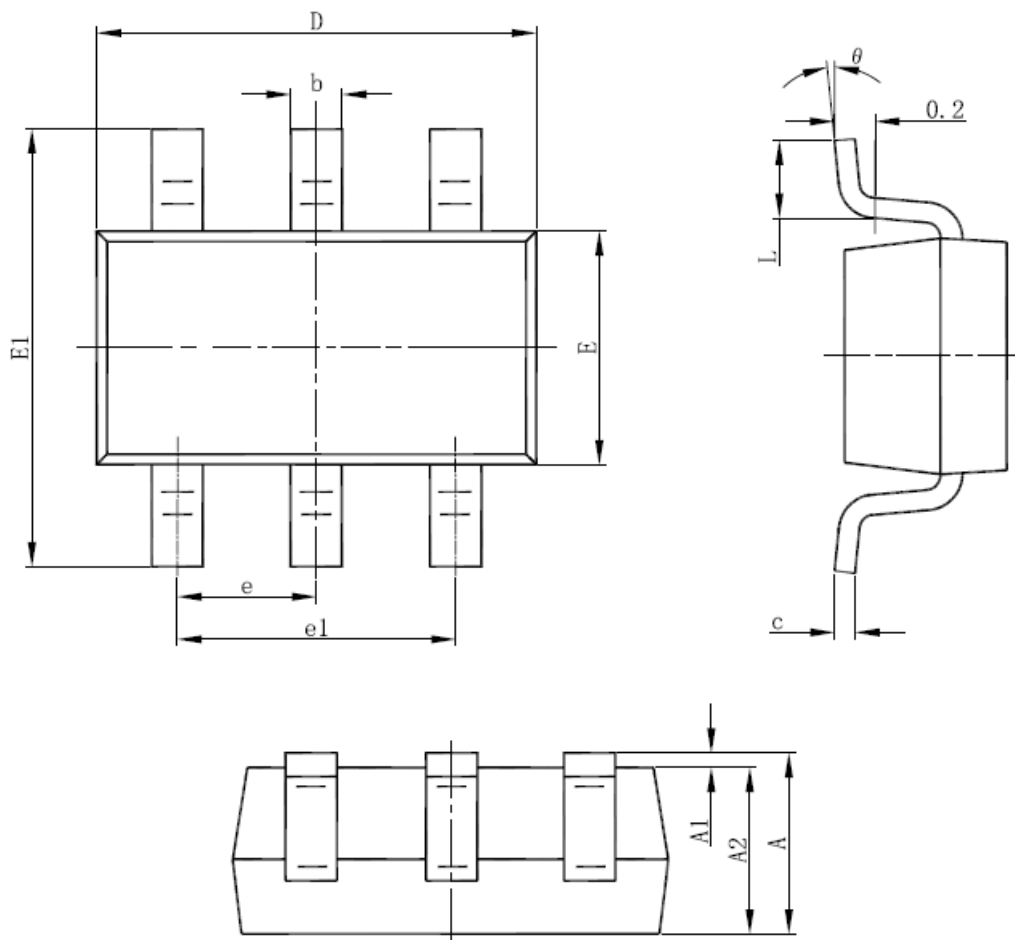


Figure 21. Efficiency vs V_{IN} with Red LED

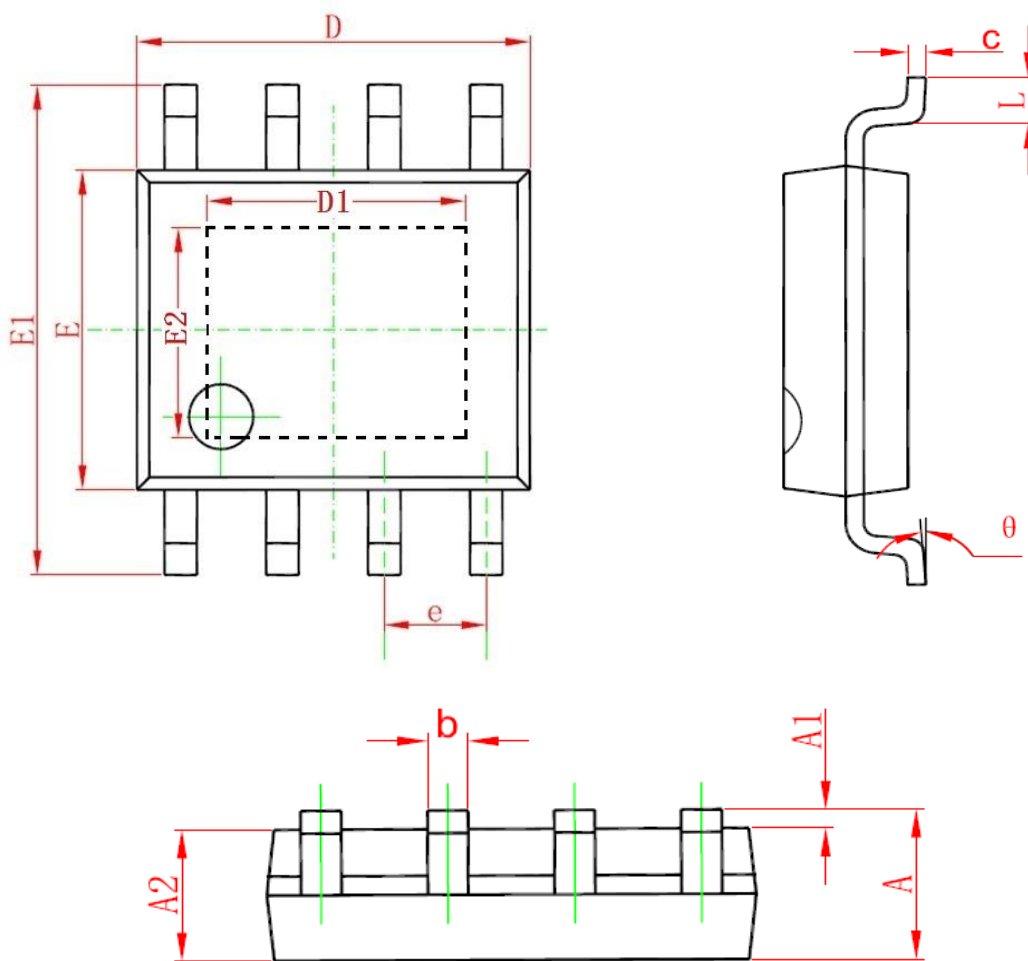
■ PACKAGING INFORMATION

● SOT-23-6 Package Outline Dimensions



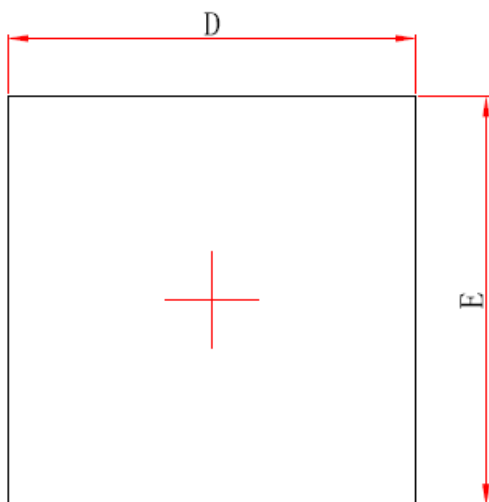
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

● SOP8-PP Package Outline Dimensions

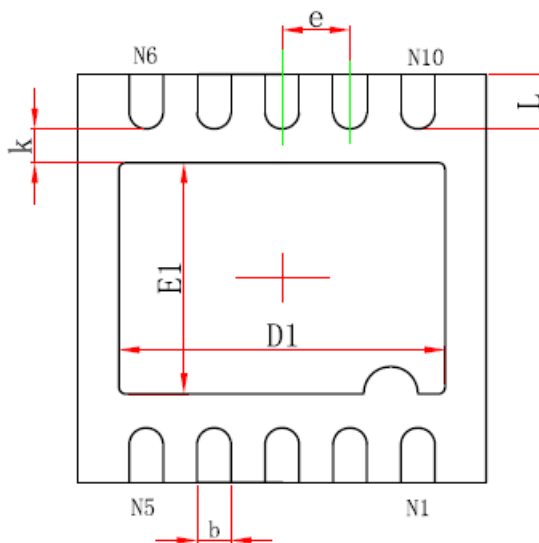


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.100	3.500	0.122	0.137
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.200	2.600	0.086	0.102
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

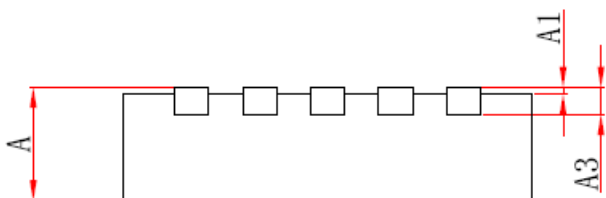
● DFN3x3-10 Package Outline Dimensions



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	2.300	2.500	0.091	0.098
E1	1.600	1.800	0.063	0.071
k	0.200MIN		0.008MIN	
b	0.180	0.300	0.007	0.012
e	0.500TYP		0.020TYP	
L	0.300	0.500	0.012	0.020

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