



CEP02N6/CEB02N6

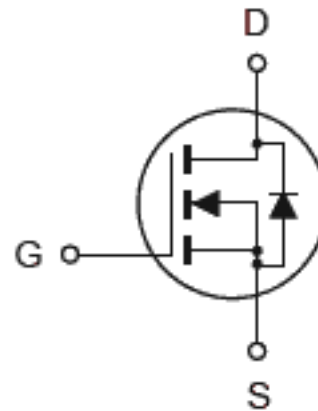
Sep. 2002

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N-Channel Logic Level Enhancement Mode Field Effect Transistor

FEATURES

- 600V, 2A, $R_{DS(ON)}=5\Omega$ @ $V_{GS}=10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current-Continuous -Pulsed	I_D	2	A
	I_{DM}	6	A
Drain-Source Diode Forward Current	I_S	6	A
Maximum Power Dissipation @Tc=25°C Derate above 25°C	P_D	60	W
		0.48	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.1	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

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ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE AVALANCHE RATING²						
Single Pulse Avalanche Energy ^c	E _{AS}			125		mJ
Avalanche Current	I _{AR}			2		A
Repetitive Avalanche Energy	E _{AR}			5.4		mJ
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	600			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 600V, V _{GS} = 0V			25	μA
Gate-Body Leakage	I _{GSS}	V _{GS} = ± 30V, V _{DS} = 0V			± 100	nA
ON CHARACTERISTICS²						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2		4	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 1A		3.8	5.0	Ω
On-State Drain Current	I _{D(on)}	V _{GS} = 10V, V _{DS} = 10V	2			A
Forward Transconductance	g _{FS}	V _{DS} = 50V, I _D = 1A		1.2		S
SWITCHING CHARACTERISTICS^b						
Turn-On Delay Time	t _{D(on)}	V _{DD} = 300V, I _D = 2A, V _{GS} = 10V R _{GEN} = 18Ω		18	35	ns
Rise Time	t _r			18	35	ns
Turn-Off Delay Time	t _{D(off)}			50	90	ns
Fall Time	t _f			16	40	ns
Total Gate Charge	Q _g	V _{DS} = 480V, I _D = 2A, V _{GS} = 10V		20	25	nC
Gate-Source Charge	Q _{gs}			2		nC
Gate-Drain Charge	Q _{gd}			12		nC

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ELECTRICAL CHARACTERISTICS ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS^b						
Input Capacitance	C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0\text{V}$ $f=1.0\text{MHz}$		250		pF
Output Capacitance	C_{oss}			50		pF
Reverse Transfer Capacitance	C_{rss}			30		pF
DRAIN-SOURCE DIODE CHARACTERISTICS^a						
Diode Forward Voltage	V_{SD}	$V_{GS}=0\text{V}, I_S=2\text{A}$			1.5	V

Notes

- a. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.
- c. $L=60\text{mH}$, $I_{AS}=2.0\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

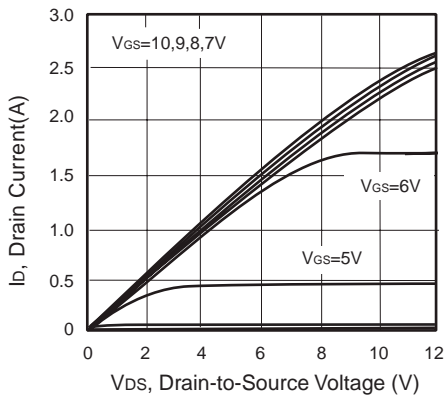


Figure 1. Output Characteristics

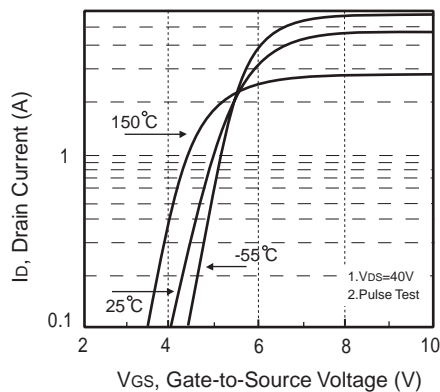


Figure 2. Transfer Characteristics

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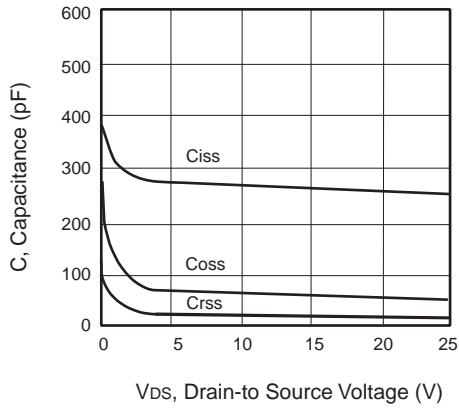


Figure 3. Capacitance

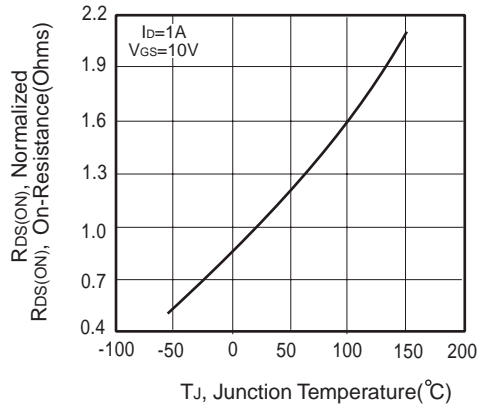


Figure 4. On-Resistance Variation with Temperature

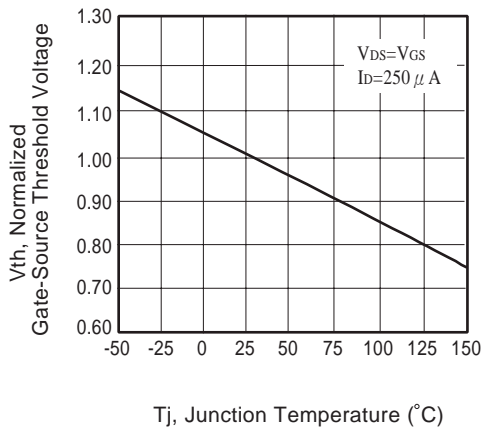


Figure 5. Gate Threshold Variation with Temperature

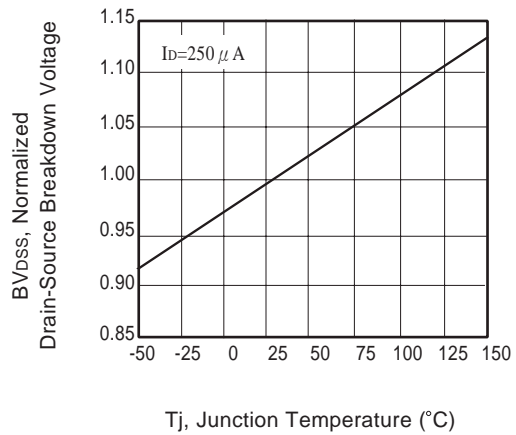


Figure 6. Breakdown Voltage Variation with Temperature

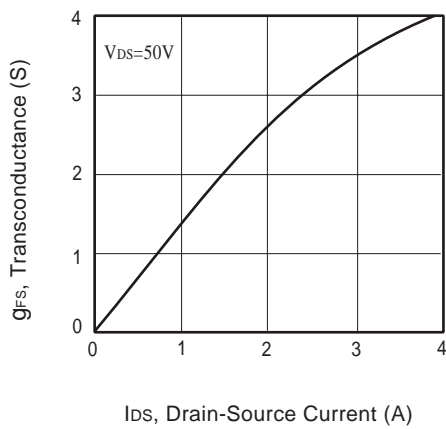


Figure 7. Transconductance Variation with Drain Current

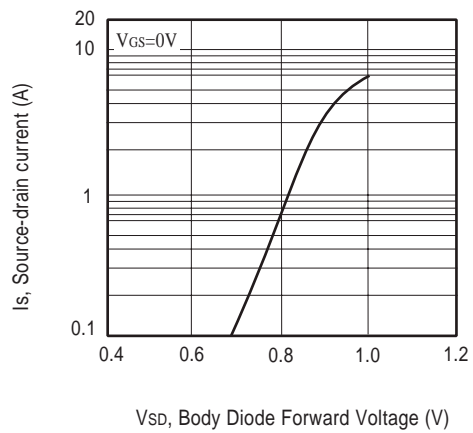


Figure 8. Body Diode Forward Voltage Variation with Source Current

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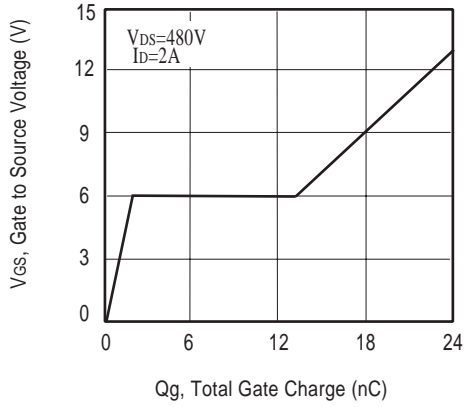


Figure 9. Gate Charge

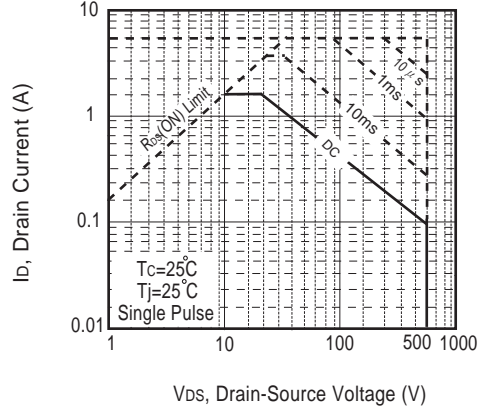


Figure 10. Maximum Safe Operating Area

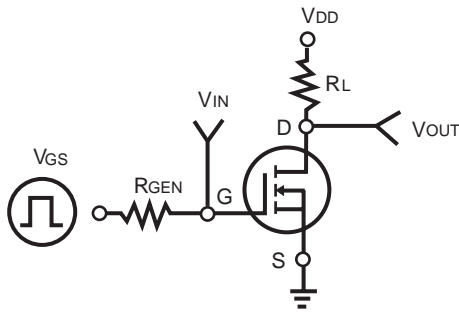


Figure 11. Switching Test Circuit

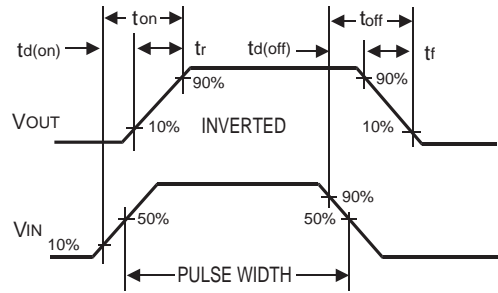


Figure 12. Switching Waveforms

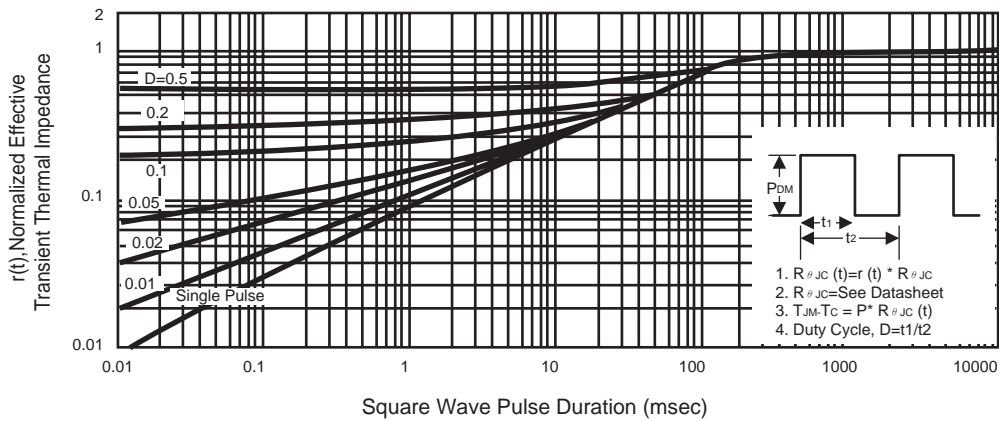


Figure 13. Normalized Thermal Transient Impedance Curve