



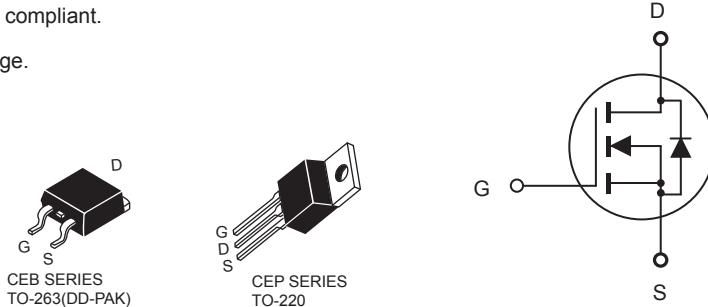
CEP60N10V/CEB60N10V

N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

- 100V, 57A, $R_{DS(ON)} = 24m\Omega$ @ $V_{GS} = 10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead-free plating ; RoHS compliant.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current-Continuous	I_D	57	A
Drain Current-Pulsed ^a	I_{DM}	228	A
Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$	P_D	200 1.3	W W/ $^\circ C$
Single Pulsed Avalanche Energy ^d	E_{AS}	560	mJ
Single Pulsed Avalanche Current ^d	I_{AS}	40	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.75	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$

This is preliminary information on a new product in development now .
Details are subject to change without notice .

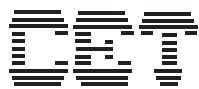
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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 100\text{V}, V_{\text{GS}} = 0\text{V}$		1		μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{\text{GS}} = 30\text{V}, V_{\text{DS}} = 0\text{V}$		100		nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{\text{GS}} = -30\text{V}, V_{\text{DS}} = 0\text{V}$		-100		nA
On Characteristics^b						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250\mu\text{A}$	3		5	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10\text{V}, I_D = 30\text{A}$		20	24	$\text{m}\Omega$
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 25\text{V}, V_{\text{GS}} = 0\text{V}, f = 1.0 \text{ MHz}$		2520		pF
Output Capacitance	C_{oss}			400		pF
Reverse Transfer Capacitance	C_{rss}			30		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}} = 50\text{V}, I_D = 30\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 2.5\Omega$		26		ns
Turn-On Rise Time	t_r			4		ns
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			43		ns
Turn-Off Fall Time	t_f			7		ns
Total Gate Charge	Q_g	$V_{\text{DS}} = 80\text{V}, I_D = 30\text{A}, V_{\text{GS}} = 10\text{V}$		53		nC
Gate-Source Charge	Q_{gs}			16		nC
Gate-Drain Charge	Q_{gd}			22		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S			57		A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{\text{GS}} = 0\text{V}, I_S = 57\text{A}$		1.3		V
Notes :						
a.Repetitive Rating : Pulse width limited by maximum junction temperature.□						
b.Pulse Test : Pulse Width $\leq 300\mu\text{s}$. Duty Cycle $\leq 2\%$.						
c.Guaranteed by design, not subject to production testing. d.L = $700\mu\text{H}$, $I_{\text{AS}} = 40\text{A}$, $V_{\text{DD}} = 25\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$						



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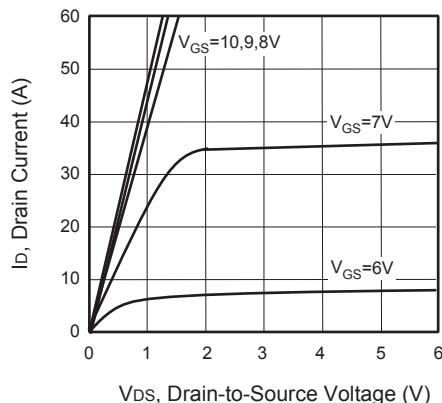


Figure 1. Output Characteristics

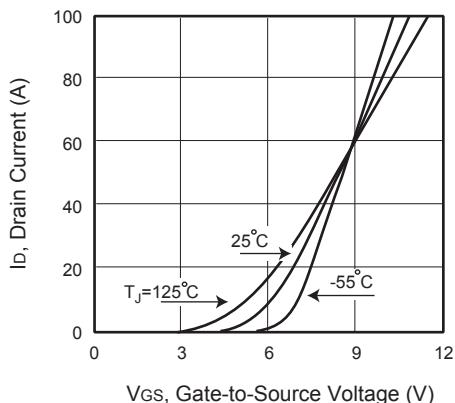


Figure 2. Transfer Characteristics

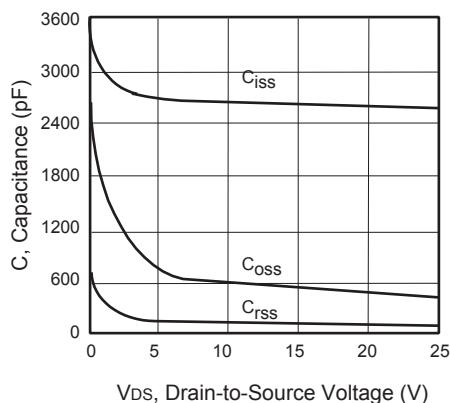


Figure 3. Capacitance

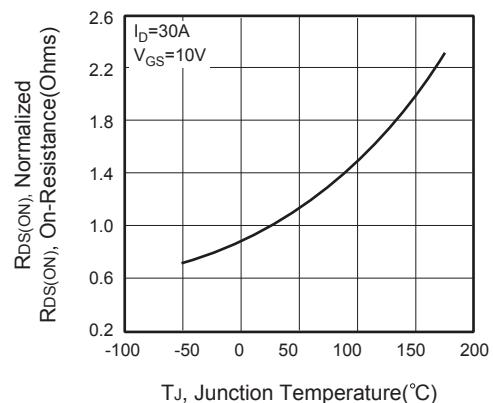


Figure 4. On-Resistance Variation with Temperature

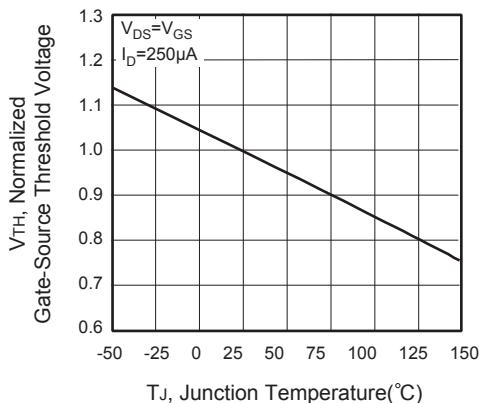


Figure 5. Gate Threshold Variation with Temperature

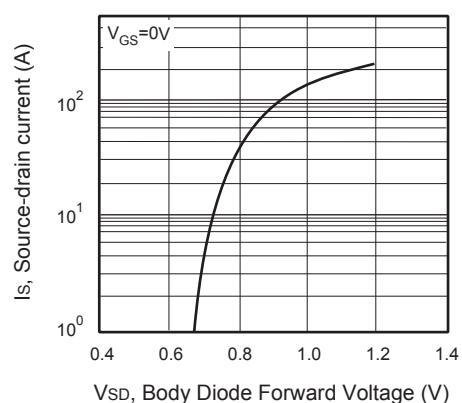


Figure 6. Body Diode Forward Voltage Variation with Source Current



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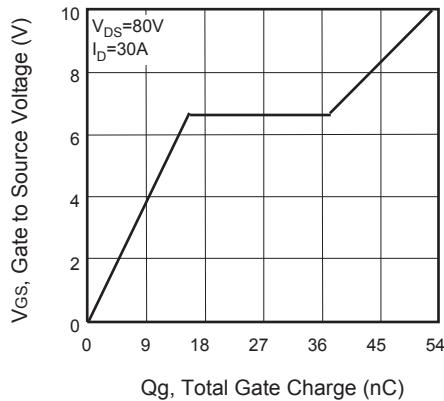


Figure 7. Gate Charge

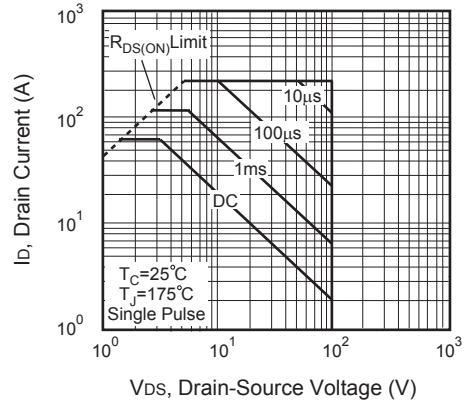


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

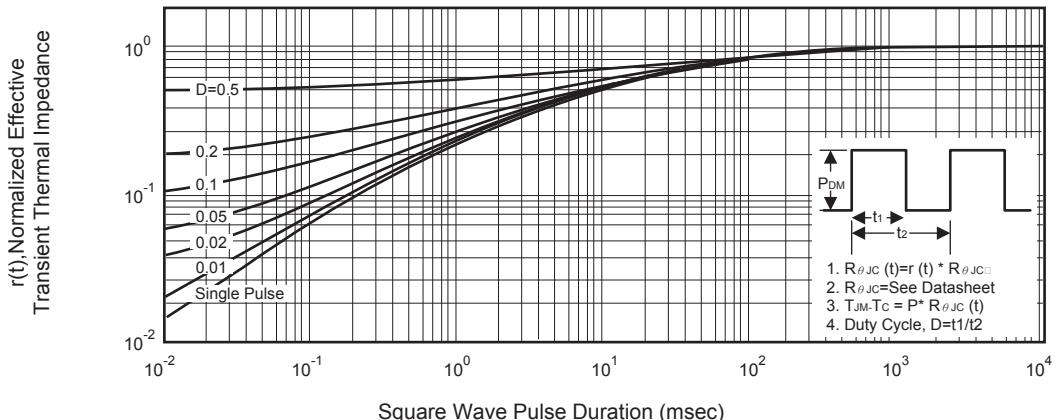


Figure 11. Normalized Thermal Transient Impedance Curve