

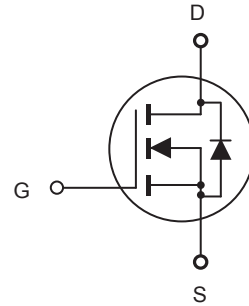


CED02N7G-1/CEU02N7G-1

N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- 720V, 1.6A, $R_{DS(ON)} = 6.75\Omega$ @ $V_{GS} = 10V$,
750V@ $T_C=150^\circ C$
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.
- TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	720 ($T_C=25^\circ C$)	V
		750 ($T_C=150^\circ C$)	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current-Continuous @ $T_C = 25^\circ C$ @ $T_C = 100^\circ C$	I_D	1.6	A
		1.1	A
Drain Current-Pulsed ^a	I_{DM}	6.4	A
Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$	P_D	48	W
		0.38	W/ $^\circ C$
Single Pulsed Avalanche Energy ^d	E_{AS}	11.25	mJ
Single Pulsed Avalanche Current ^d	I_{AS}	1.5	A
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.6	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ C/W$



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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$T_C=25^\circ\text{C}, V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	720			V
		$T_C=150^\circ\text{C}, V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	750			
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 700\text{V}, V_{GS} = 0\text{V}$			25	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30\text{V}, V_{DS} = 0\text{V}$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30\text{V}, V_{DS} = 0\text{V}$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{V}, I_D = 1\text{A}$		5.4	6.75	Ω
Dynamic Characteristics^c						
Forward Transconductance	g_{FS}	$V_{DS} = 50\text{V}, I_D = 1\text{A}$		1.5		S
Input Capacitance	C_{iss}	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$		315		pF
Output Capacitance	C_{oss}			55		pF
Reverse Transfer Capacitance	C_{rss}			20		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{V}, I_D = 1.9\text{A}, V_{GS} = 10\text{V}, R_{GEN} = 18\Omega$		14		ns
Turn-On Rise Time	t_r			12.5		ns
Turn-Off Delay Time	$t_{d(off)}$			23		ns
Turn-Off Fall Time	t_f			10		ns
Total Gate Charge	Q_g	$V_{DS} = 480\text{V}, I_D = 1.9\text{A}, V_{GS} = 10\text{V}$		9		nC
Gate-Source Charge	Q_{gs}			1.5		nC
Gate-Drain Charge	Q_{gd}			5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S				1.6	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0\text{V}, I_S = 1\text{A}$			1.5	V
Notes : □ a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$. □ c.Guaranteed by design, not subject to production testing. □ d.L =10mH, $I_{AS} = 1.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$						



CED02N7G-1/CEU02N7G-1

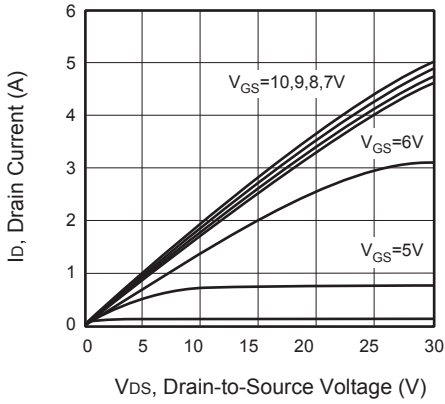


Figure 1. Output Characteristics

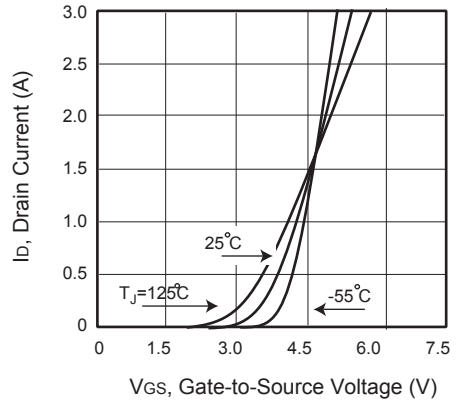


Figure 2. Transfer Characteristics

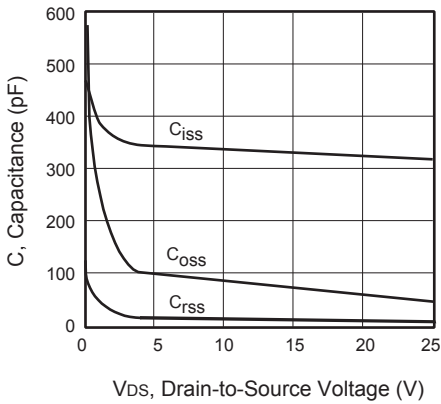


Figure 3. Capacitance

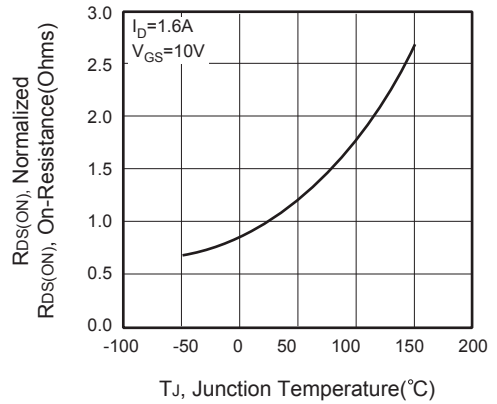


Figure 4. On-Resistance Variation with Temperature

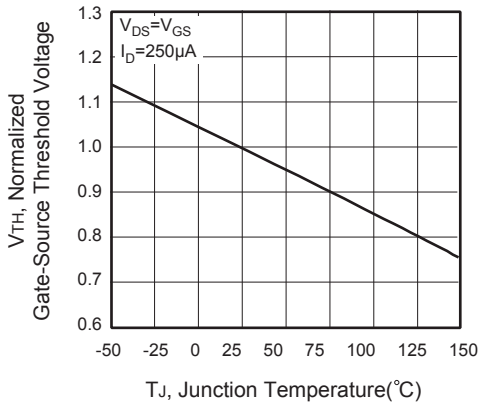


Figure 5. Gate Threshold Variation with Temperature

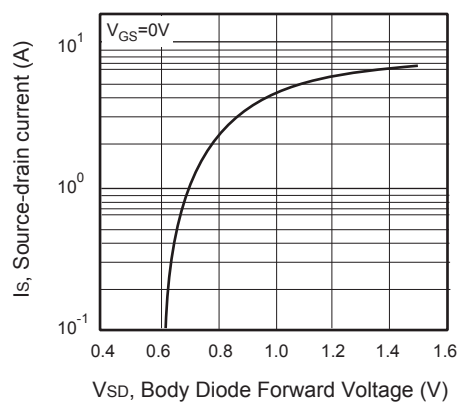


Figure 6. Body Diode Forward Voltage Variation with Source Current



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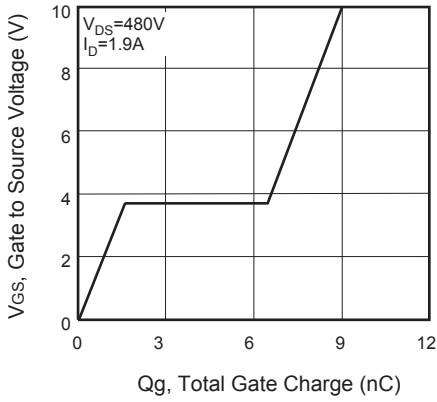


Figure 7. Gate Charge

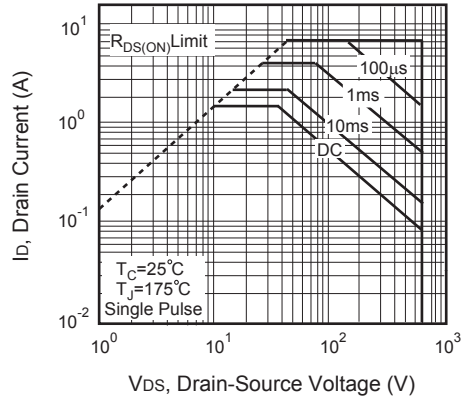


Figure 8. Maximum Safe Operating Area

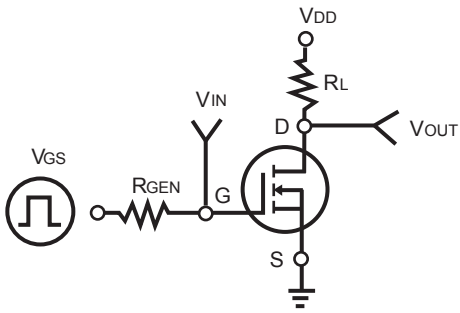


Figure 9. Switching Test Circuit

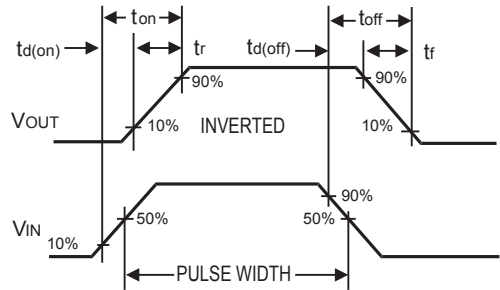


Figure 10. Switching Waveforms

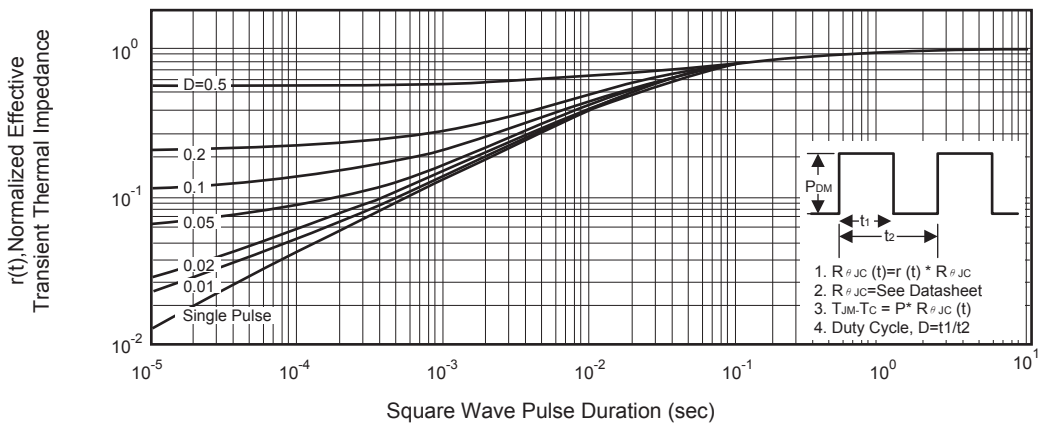


Figure 11. Normalized Thermal Transient Impedance Curve