

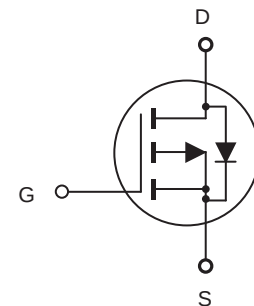


CED12P10/CEU12P10

P-Channel Enhancement Mode Field Effect Transistor

FEATURES

- -100V, -9A, $R_{DS(ON)} = 315m\Omega$ @ $V_{GS} = -10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead free product is acquired.
- TO-251 & TO-252 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	± 30	V
Drain Current-Continuous	I_D	-9	A
Drain Current-Pulsed ^a	I_{DM}	-36	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above 25°C	P_D	50	W
		0.4	W/ $^\circ\text{C}$
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$



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Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100V, V_{GS} = 0V$			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics ^c						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-2		-4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -4.7A$		260	315	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = -40V, I_D = -4.7A$		3.5		S
Dynamic Characteristics ^d						
Input Capacitance	C_{iss}	$V_{DS} = -25V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$		625		pF
Output Capacitance	C_{oss}			140		pF
Reverse Transfer Capacitance	C_{rss}			45		pF
Switching Characteristics ^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -50V, I_D = -11A,$ $V_{GS} = -10V, R_{GEN} = 25\Omega$		15	30	ns
Turn-On Rise Time	t_r			12	25	ns
Turn-Off Delay Time	$t_{d(off)}$			31	60	ns
Turn-Off Fall Time	t_f			31	60	ns
Total Gate Charge	Q_g	$V_{DS} = -80V, I_D = -11A,$ $V_{GS} = -10V$		15.6	20	nC
Gate-Source Charge	Q_{gs}			3.6		nC
Gate-Drain Charge	Q_{gd}			6.0		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				-9	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = -9A$			-1.5	V
Notes : a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10 \text{ sec}$. c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. d.Guaranteed by design, not subject to production testing.						



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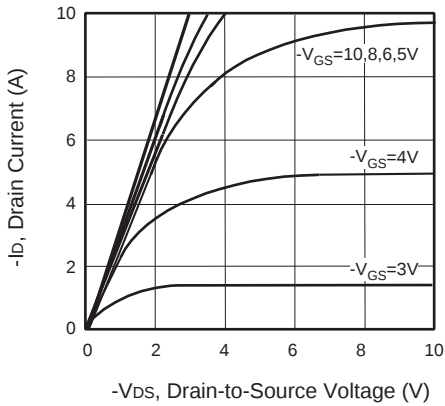


Figure 1. Output Characteristics

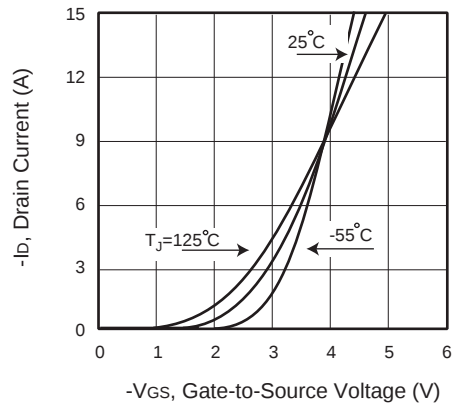


Figure 2. Transfer Characteristics

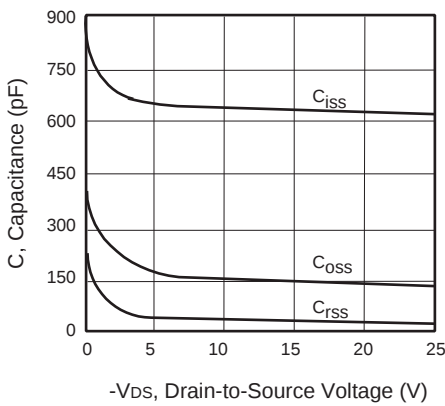


Figure 3. Capacitance

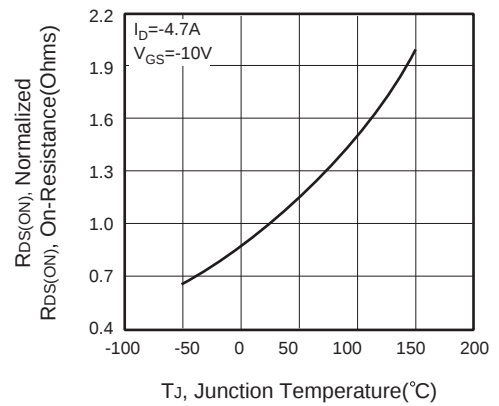


Figure 4. On-Resistance Variation with Temperature

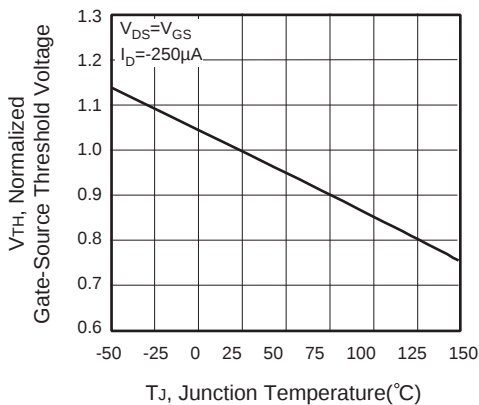


Figure 5. Gate Threshold Variation with Temperature

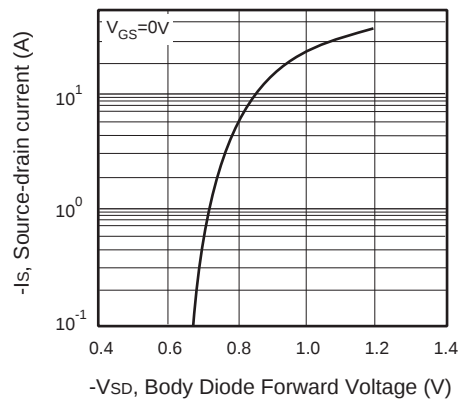


Figure 6. Body Diode Forward Voltage Variation with Source Current



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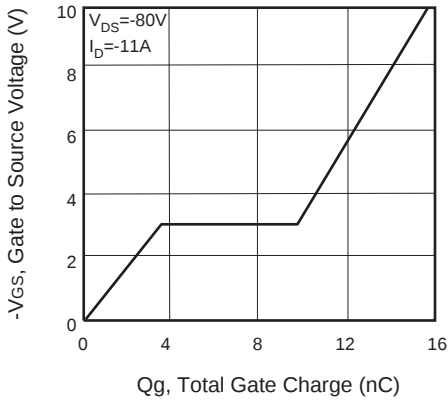


Figure 7. Gate Charge

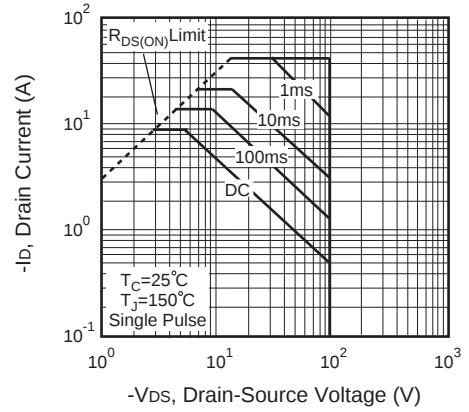


Figure 8. Maximum Safe Operating Area

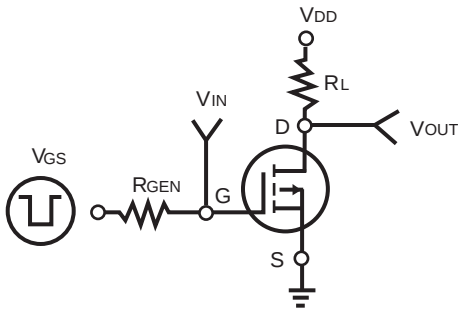


Figure 9. Switching Test Circuit

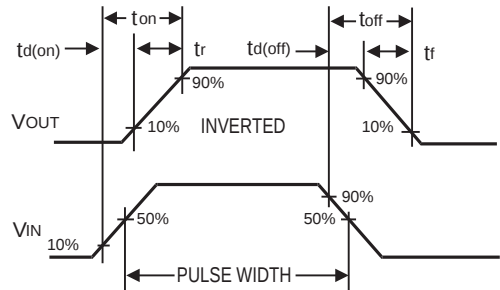


Figure 10. Switching Waveforms

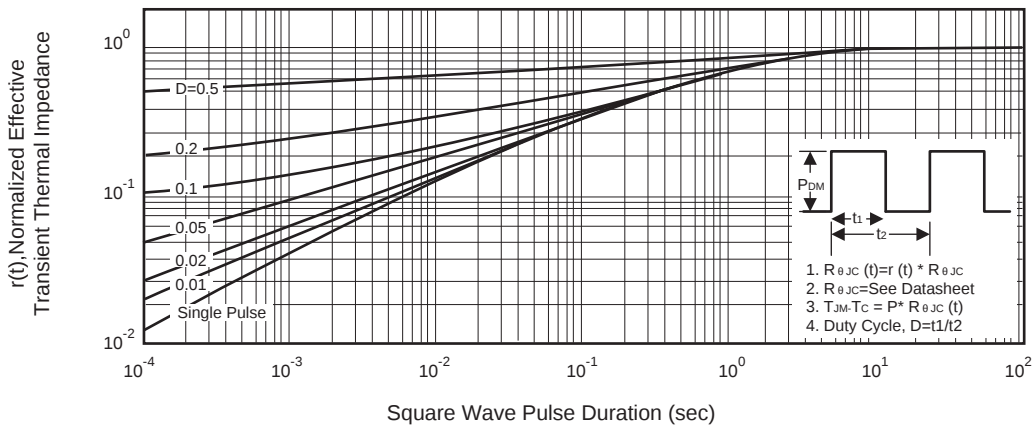


Figure 11. Normalized Thermal Transient Impedance Curve