CED61A3/CEU61A3

Jan. 2003

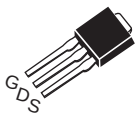
N-Channel Logic Level Enhancement Mode Field Effect Transistor

6

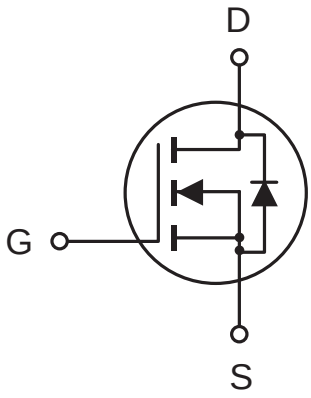
FEATURES

- 30V , 40A , $R_{DS(ON)}$=13.5mΩ @V_{GS}=10V.
  $R_{DS(ON)}$=20mΩ @V_{GS}=4.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- TO-251 & TO-252 package.

CEU SERIES
TO-252AA(D-PAK)



CED SERIES
TO-251(I-PAK)



ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	40	A
-Pulsed	I_{DM}	120	A
Drain-Source Diode Forward Current	I_S	40	A
Maximum Power Dissipation @Tc=25°C	P_D	50	W
Derate above 25°C		0.4	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	μA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
ON CHARACTERISTICS[a]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D 250μA	1		3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 20A		11	13.5	mΩ
		V_{GS} = 4.5V, I_D = 18A		16.5	20	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	40			A
Forward Transconductance	g_{FS}	V_{DS} = 10V, I_D = 26A		34		S
DYNAMIC CHARACTERISTICS[b]						
Input Capacitance	C_{ISS}	V_{DS} =15V, V_{GS} = 0V f =1.0MHz		1200		pF
Output Capacitance	C_{OSS}			480		pF
Reverse Transfer Capacitance	C_{RSS}			130		pF
SWITCHING CHARACTERISTICS[b]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 15V, I_D = 40A, V_{GS} = 10V R_{GEN} =24Ω		18	30	ns
Rise Time	t_r			25	50	ns
Turn-Off Delay Time	$t_{D(OFF)}$			45	90	ns
Fall Time	t_f			75	130	ns
Total Gate Charge	Q_g	V_{DS} = 15V,I_D = 40A V_{GS} = 5V		19	23	nC
Gate-Source Charge	Q_{gs}			5		nC
Gate-Drain Charge	Q_{gd}			9		nC

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ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS [a]						
Diode Forward Voltage	V_{SD}	V_{GS} = 0V, Is = 26A		0.9	1.3	V

6

Notes

a.Pulse Test:Pulse Width≤300 μs, Duty Cycle≤ 2%.

b.Guaranteed by design, not subject to production testing.

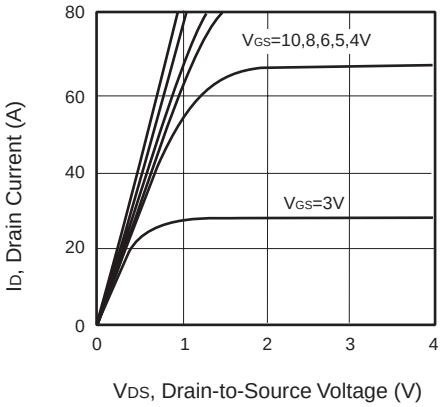

Figure 1. Output Characteristics

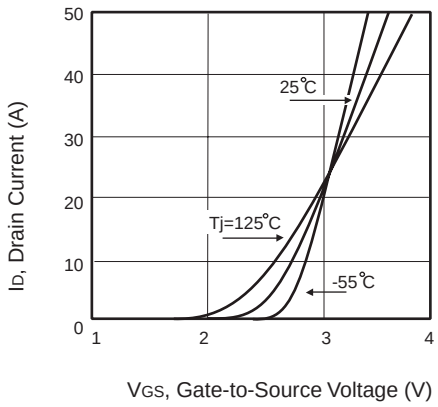

Figure 2. Transfer Characteristics

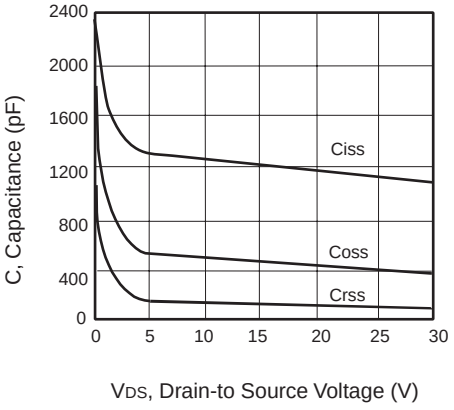

Figure 3. Capacitance

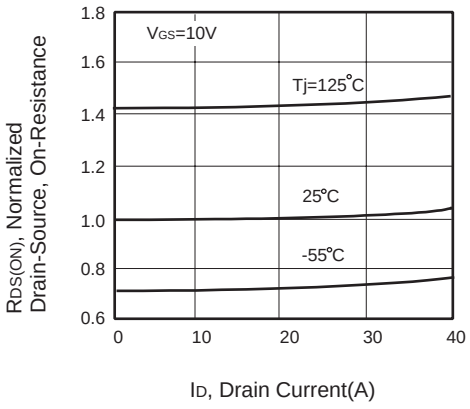

Figure 4. On-Resistance Variation with Drain Current and Temperature

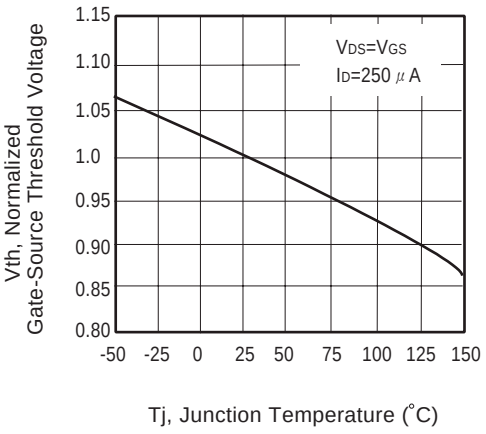

Figure 5. Gate Threshold Variation with Temperature

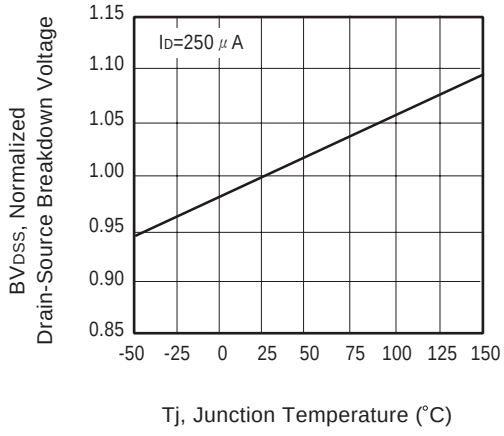

Figure 6. Breakdown Voltage Variation with Temperature

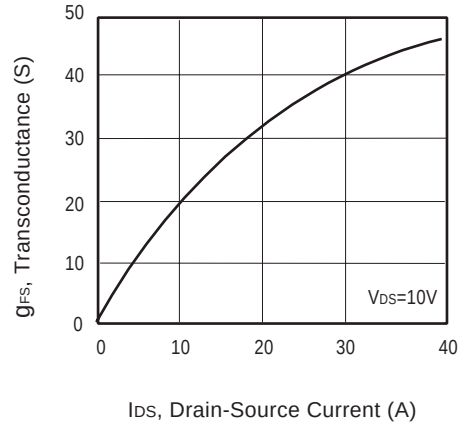

Figure 7. Transconductance Variation with Drain Current

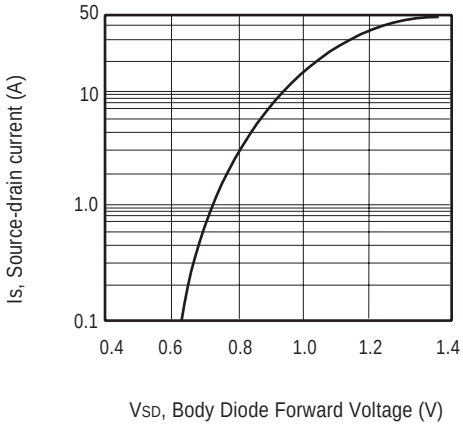

Figure 8. Body Diode Forward Voltage Variation with Source Current

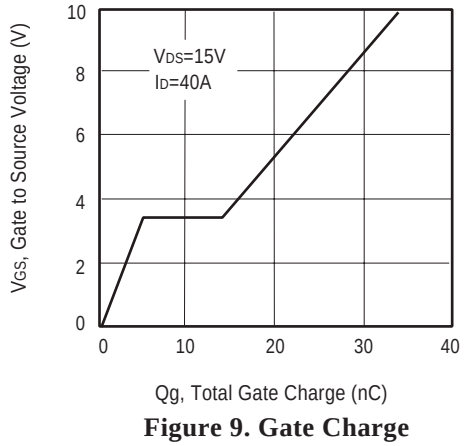

Figure 9. Gate Charge

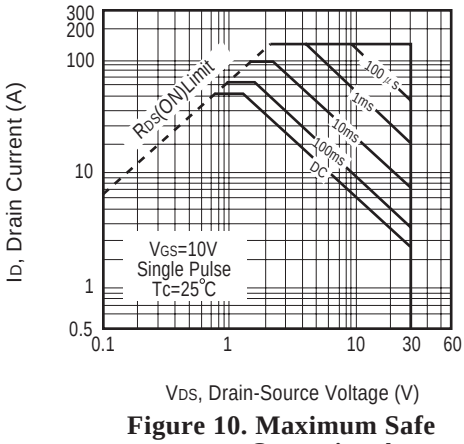

Figure 10. Maximum Safe Operating Area

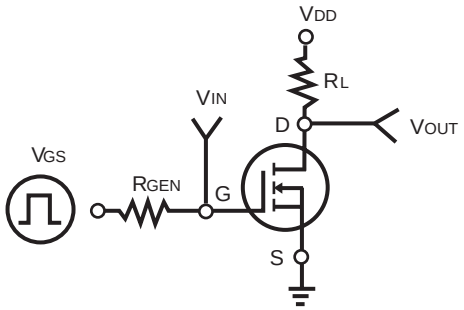

Figure 11. Switching Test Circuit

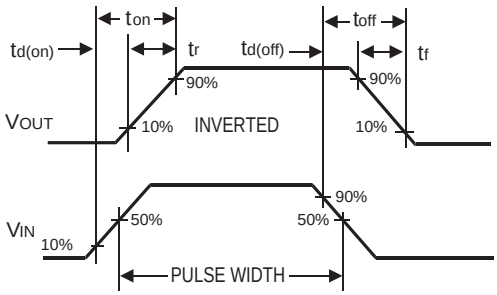

Figure 12. Switching Waveforms

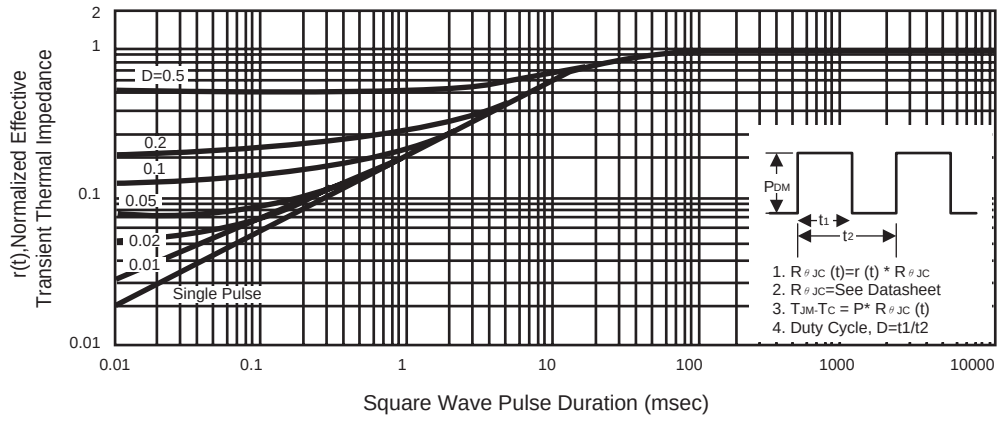

Figure 13. Normalized Thermal Transient Impedance Curve