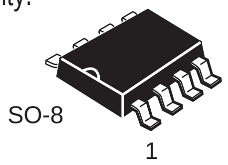
CEM11C2

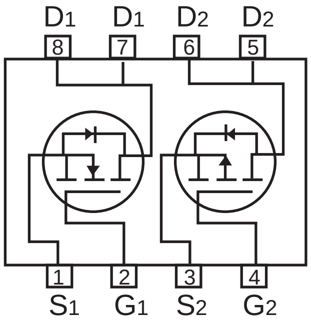
Jul. 2002

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

FEATURES

- 30V ,7A , $R_{DS(ON)}$=30mΩ @V_{GS}=10V.
  $R_{DS(ON)}$=42mΩ @V_{GS}=4.5V.
  -20V , -4.3A , $R_{DS(ON)}$=90mΩ @V_{GS}=-4.5V.
  $R_{DS(ON)}$=120mΩ @V_{GS}=-2.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Surface Mount Package.





ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	30	-20	V
Gate-Source Voltage	V_{GS}	±20	±8	V
Drain Current-Continuous[a] @T_J=125°C	I_D	±7	±4.3	A
-Pulsed[b]	I_{DM}	±30	±17	A
Drain-Source Diode Forward Current[a]	I_S	2.3	-4.3	A
Maximum Power Dissipation[a]	P_D	2.0		W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient[a]	$R_{\theta JA}$	62.5	°C/W

N-Channel ELECTRICAL CHARACTERISTICS (T$_A$=25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V,I_D = 250µA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	µA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
ON CHARACTERISTICS^b						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	1		3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 7A		24	30	mΩ
		V_{GS} = 4.5V, I_D = 3.5A		32	42	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	30			A
Forward Transconductance	g_{FS}	V_{DS} = 15V, I_D =7A		8		S
DYNAMIC CHARACTERISTICS^c						
Input Capacitance	C_{ISS}	V_{DS} =15V, V_{GS} = 0V f =1.0MHz		804		pF
Output Capacitance	C_{OSS}			328		pF
Reverse Transfer Capacitance	C_{RSS}			79		pF
SWITCHING CHARACTERISTICS^c						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 25V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6Ω		16	24	ns
Rise Time	t_r			7	14	ns
Turn-Off Delay Time	$t_{D(OFF)}$			47	60	ns
Fall Time	t_f			10	15	ns
Total Gate Charge	Q_g	V_{DS} =15V, I_D = 2A, V_{GS} =10V		20	24	nC
Gate-Source Charge	Q_{gs}			3		nC
Gate-Drain Charge	Q_{gd}			6		nC

P-Channel ELECTRICAL CHARACTERISTICS (T$_A$=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250µA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16V, V_{GS} = 0V			-1	µA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±8V, V_{DS} = 0V			±100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250µA	-0.6		-1.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = -4.5V,I_D = -2.2A		50	90	mΩ
		V_{GS} = -2.5V,I_D = -1.8A		80	120	mΩ
On-State Drain Current	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -4.5V	-20			A
Forward Transconductance	g_{FS}	V_{DS} = -16V,I_D = -2.2A	4	6		S
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS} =-15V, V_{GS} = 0V f =1.0MHz		1430		pF
Output Capacitance	C_{OSS}			800		pF
Reverse Transfer Capacitance	C_{RSS}			325		pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 10V, I_D = -2.2A, V_{GEN} = - 4.5V, R_{GEN} = 6 Ω		20	28	ns
Rise Time	t_r			21	30	ns
Turn-Off Delay Time	$t_{D(OFF)}$			76	106	ns
Fall Time	t_f			56	78	ns
Total Gate Charge	Q_g	V_{DS} =-6V, I_D = -2.2A, V_{GS} =-4.5V		19.4	25	nC
Gate-Source Charge	Q_{gs}			3		nC
Gate-Drain Charge	Q_{gd}			5		nC

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ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition		Min	Typ[c]	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS [b]							
Diode Forward Voltage	V_{SD}	V_{GS} = 0V, Is = 2A	N-Ch		0.76	1.1	V
		V_{GS} = 0V, Is =-1.8A	P-Ch		-0.80	-1.0	

Notes

a.Surface Mounted on FR4 Board, t ≤10sec.

b.Pulse Test:Pulse Width ≤300 μs, Duty Cycle ≤ 2%.

c.Guaranteed by design, not subject to production testing.

N-Channel

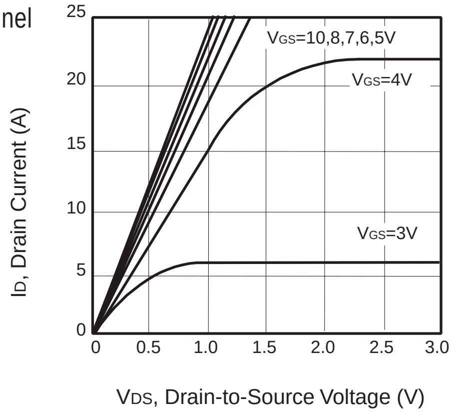


Figure 1. Output Characteristics

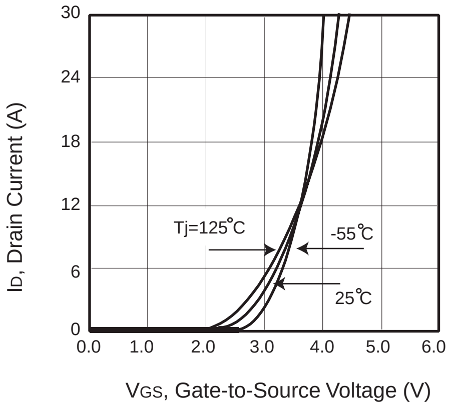


Figure 2. Transfer Characteristics

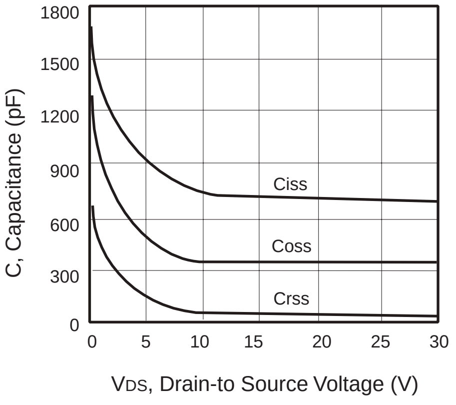


Figure 3. Capacitance

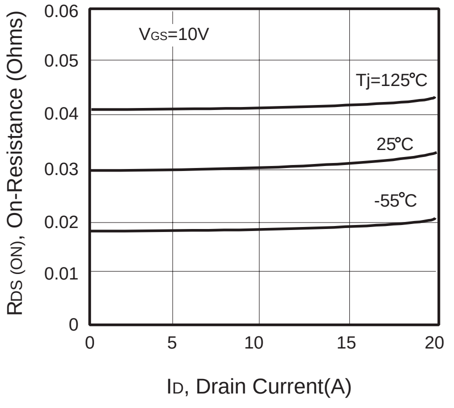


Figure 4. On-Resistance Variation with Drain Current and Temperature

N-Channel

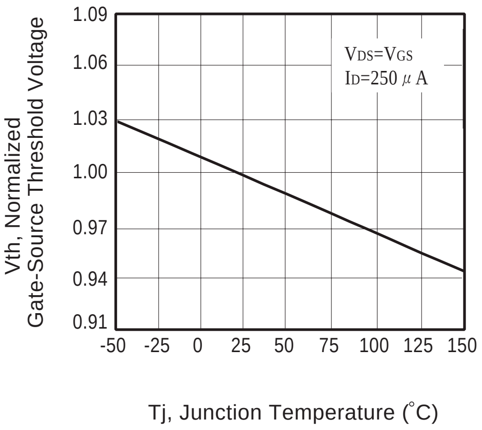


Figure 5. Gate Threshold Variation with Temperature

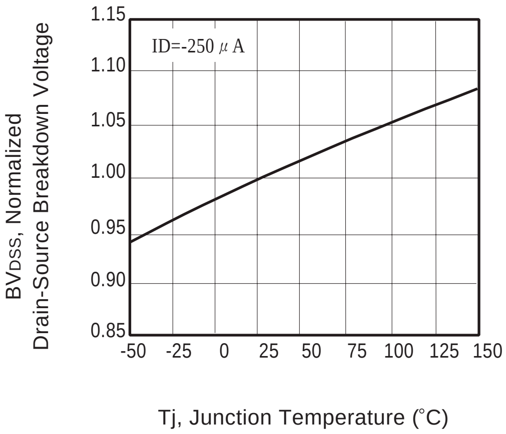


Figure 6. Breakdown Voltage Variation with Temperature

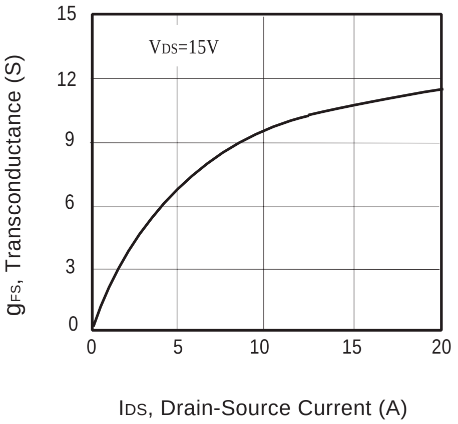


Figure 7. Transconductance Variation with Drain Current

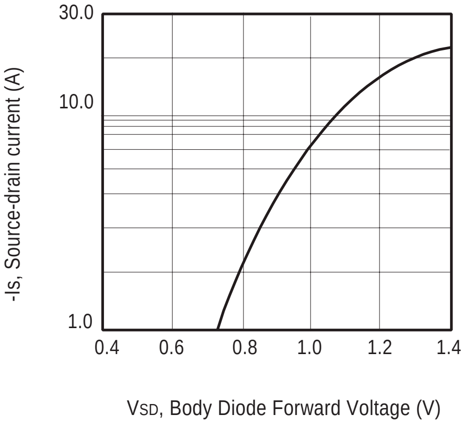


Figure 8. Body Diode Forward Voltage Variation with Source Current

P-Channel

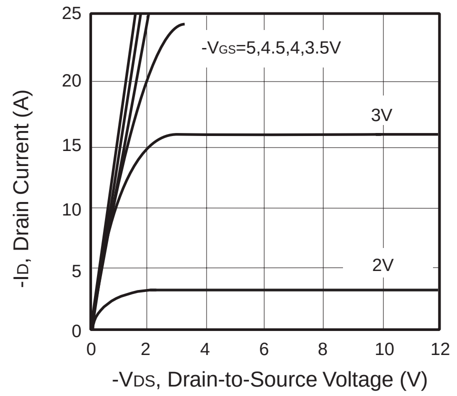


Figure 1. Output Characteristics

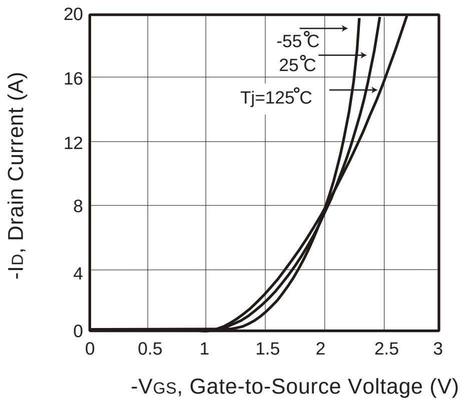


Figure 2. Transfer Characteristics

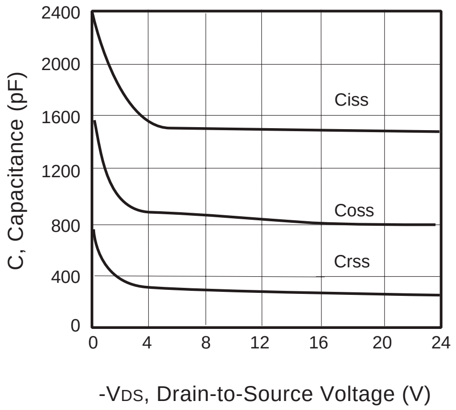


Figure 3. Capacitance

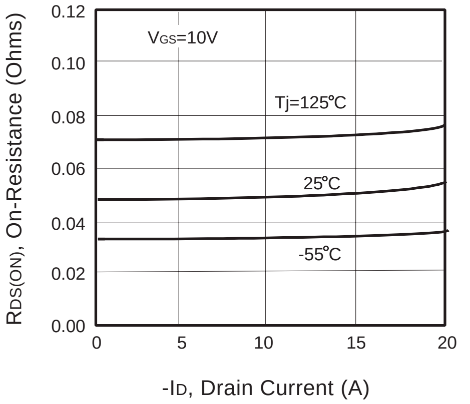


Figure 4. On-Resistance Variation withDrain Current and Temperature

P-Channel

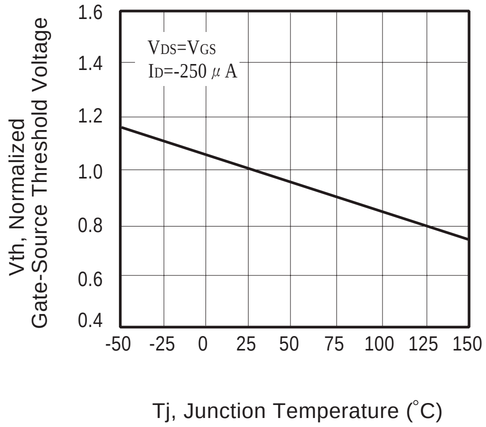


Figure 5. Gate Threshold Variation with Temperature

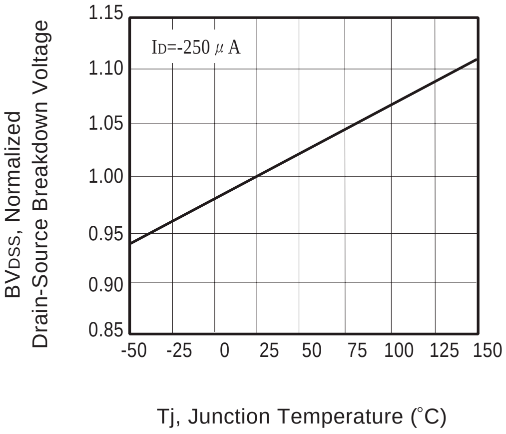


Figure 6. Breakdown Voltage Variation with Temperature

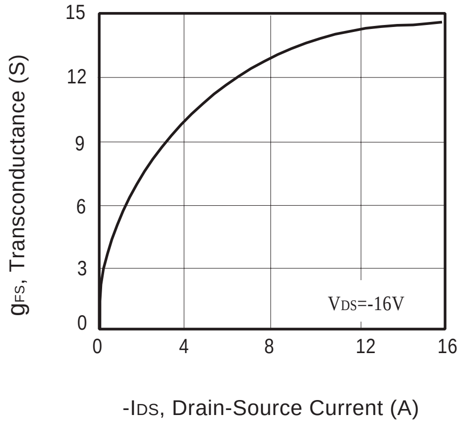


Figure 7. Transconductance Variation with Drain Current

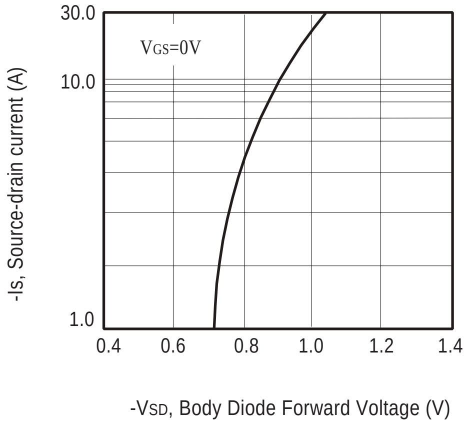


Figure 8. Body Diode Forward Voltage Variation with Source Current

N-Channel

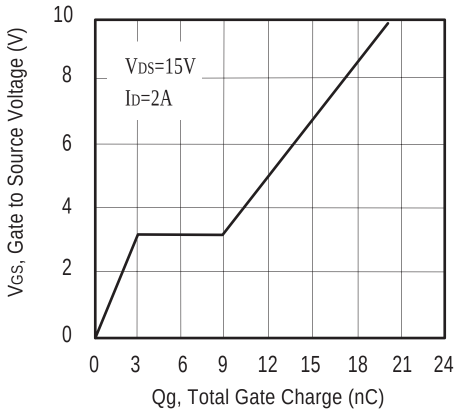


Figure 9. Gate Charge

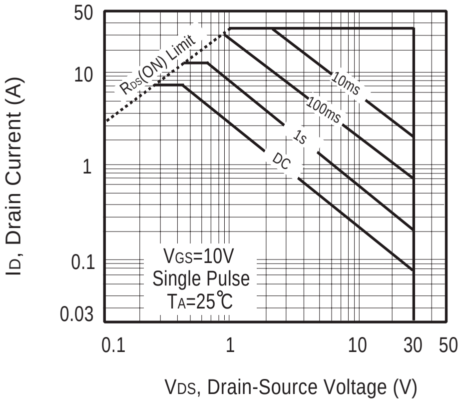
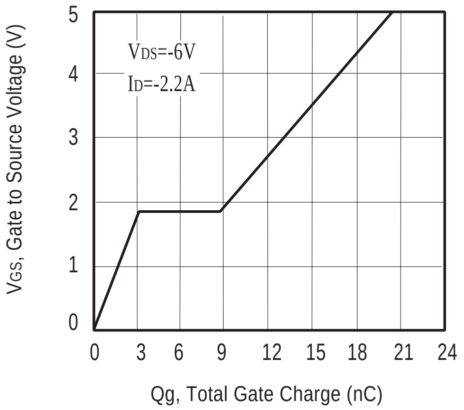


Figure 10. Maximum Safe Operating Area

P-Channel



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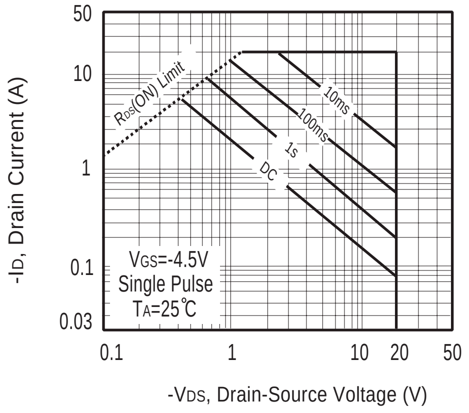

Figure 10. Maximum Safe Operating Area 50

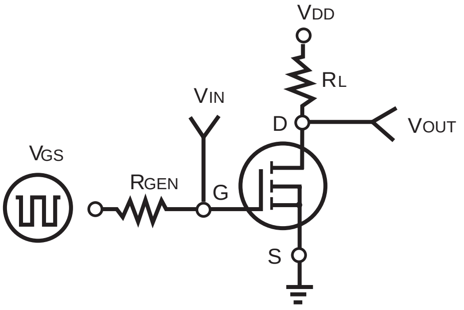

Figure 11. Switching Test Circuit

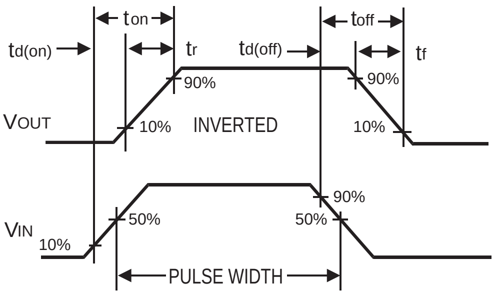

Figure 12. Switching Waveforms

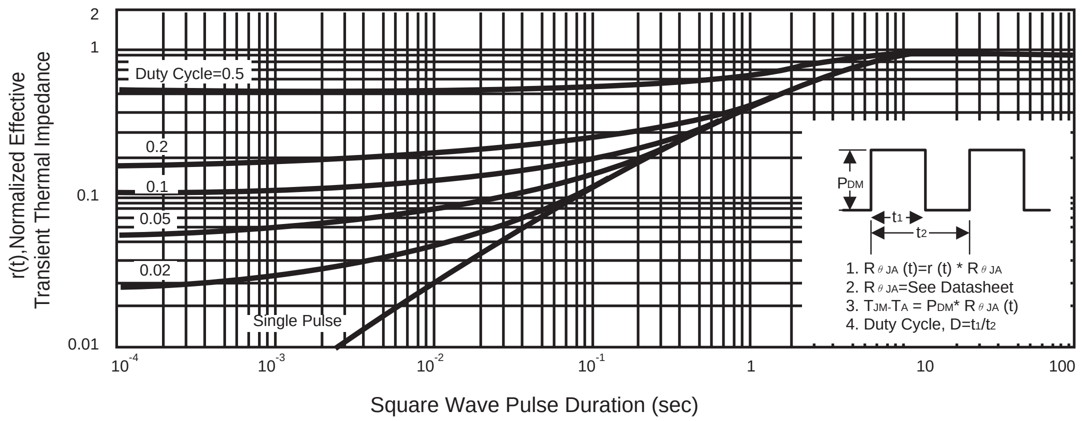

Figure 13. Normalized Thermal Transient Impedance Curve