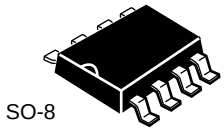
CEM3317

P-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

- -30V, -6.2A, $R_{DS(ON)}$ = 33mΩ @V_{GS} = -10V.
  $R_{DS(ON)}$ = 52mΩ @V_{GS} = -4.5V.
- -30V, -4.9A, $R_{DS(ON)}$ = 52mΩ @V_{GS} = -10V.
  $R_{DS(ON)}$ = 85mΩ @V_{GS} = -4.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.
- Surface mount Package.



SO-8

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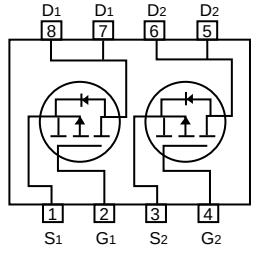

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	Channel 1	Channel 2	Units
Drain-Source Voltage	V_{DS}	-30	-30	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current-Continuous	I_D	-6.2	-4.9	A
Drain Current-Pulsed [a]	I_{DM}	-25	-20	A
Maximum Power Dissipation	P_D	2.0		W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	62.5	°C/W

P-Channel(Q1) Electrical Characteristics T_A = 25 C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -6.2A		27	33	mΩ
		V_{GS} = -4.5V, I_D = -4A		40	52	mΩ
Dynamic Characteristics [c]						
Forward Transconductance	g_{FS}	V_{DS} = -10V, I_D = -6.2A		5		S
Input Capacitance	C_{iss}	V_{DS} = -15V, V_{GS} = 0V, f = 1.0 MHz		1150		pF
Output Capacitance	C_{oss}			250		pF
Reverse Transfer Capacitance	C_{rss}			150		pF
Switching Characteristics [c]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15V, I_D = -1A, V_{GS} = -10V, R_{GEN} = 6Ω		13	25	ns
Turn-On Rise Time	t_r			6	15	ns
Turn-Off Delay Time	$t_{d(off)}$			58	115	ns
Turn-Off Fall Time	t_f			22	45	ns
Total Gate Charge	Q_g	V_{DS} = -15V, I_D = -6.2A, V_{GS} = -10V		19	25	nC
Gate-Source Charge	Q_{gs}			4.0		nC
Gate-Drain Charge	Q_{gd}			2.5		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current	I_S				-6.2	A
Drain-Source Diode Forward Voltage [b]	V_{SD}	V_{GS} = 0V, I_S = -1A			-1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
c.Guaranteed by design, not subject to production testing.

P-Channel(Q2) Electrical Characteristics T_A = 25 C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -4.9A		42	52	mΩ
		V_{GS} = -4.5V, I_D = -3.6A		65	85	mΩ
Forward Transconductance	g_{FS}	V_{DS} = -15V, I_D = -4.9A	5	8		S
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = -15V, V_{GS} = 0V, f = 1.0 MHz		845		pF
Output Capacitance	C_{oss}			155		pF
Reverse Transfer Capacitance	C_{rss}			95		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15V, I_D = -1A, V_{GS} = -10V, R_{GEN} = 6Ω		11	22	ns
Turn-On Rise Time	t_r			4	8	ns
Turn-Off Delay Time	$t_{d(off)}$			59	118	ns
Turn-Off Fall Time	t_f			23	46	ns
Total Gate Charge	Q_g	V_{DS} = -15V, I_D = -4.9A, V_{GS} = -10V		13.8	18.3	nC
Gate-Source Charge	Q_{gs}			1.8		nC
Gate-Drain Charge	Q_{gd}			2.2		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				-4.9	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = -4.9A			-1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

CHANNEL 1

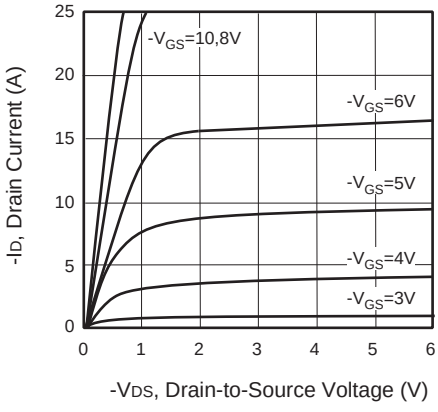

Figure 1. Output Characteristics

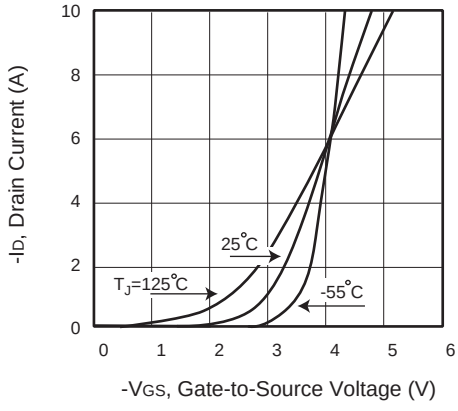

Figure 2. Transfer Characteristics

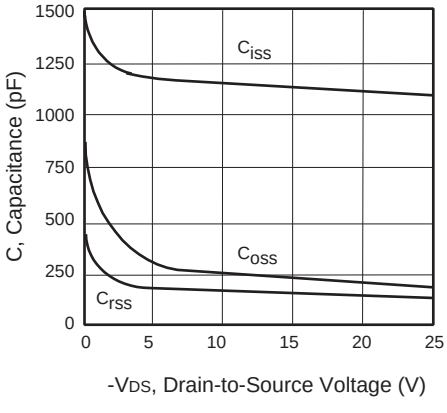

Figure 3. Capacitance

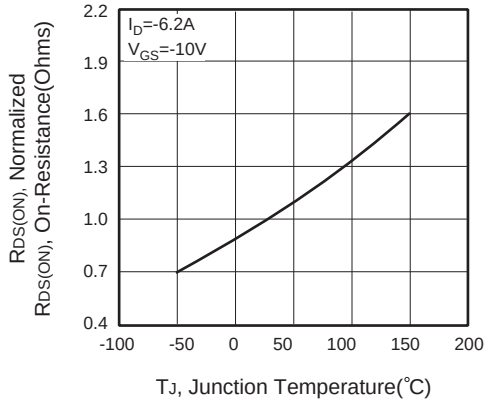

Figure 4. On-Resistance Variation with Temperature

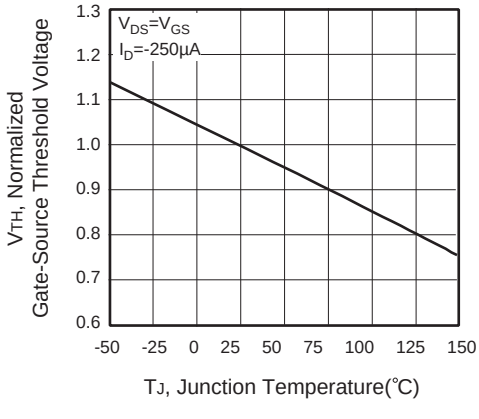

Figure 5. Gate Threshold Variation with Temperature

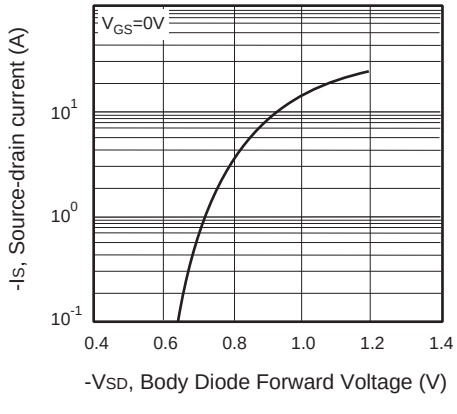

Figure 6. Body Diode Forward Voltage Variation with Source Current

CHANNEL 2

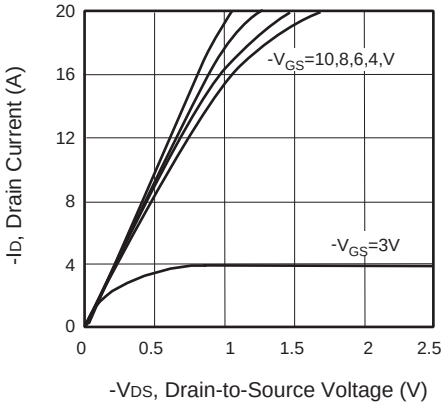

Figure 7. Output Characteristics

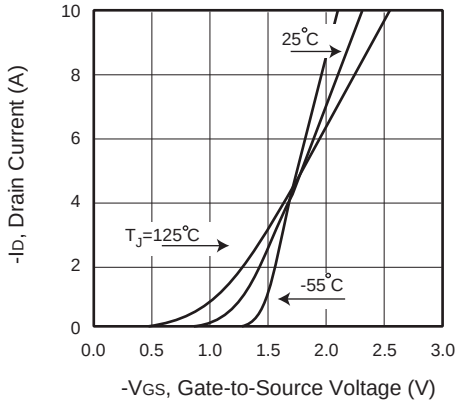

Figure 8. Transfer Characteristics

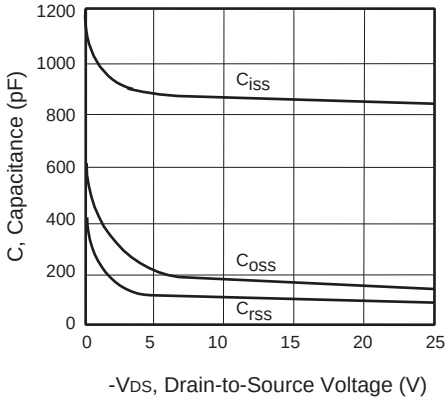

Figure 9. Capacitance

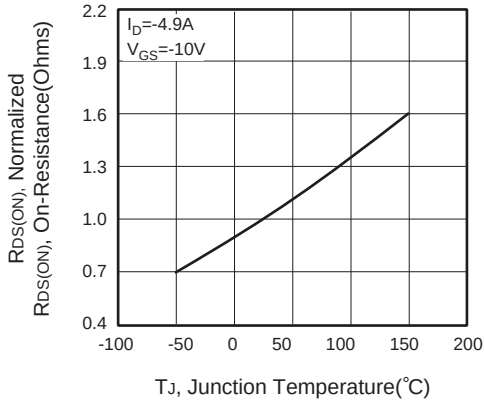

Figure 10. On-Resistance Variation with Temperature

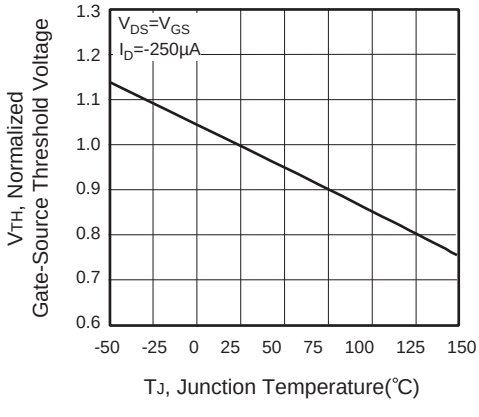

Figure 11. Gate Threshold Variation with Temperature

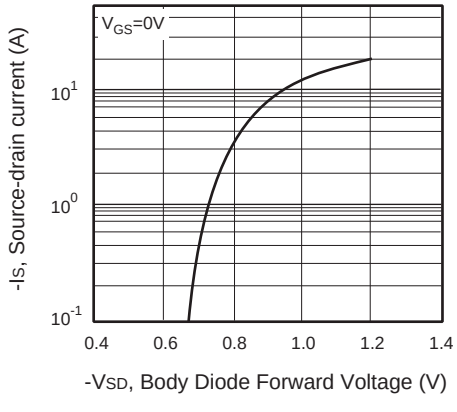

Figure 12. Body Diode Forward Voltage Variation with Source Current

CHANNEL 1

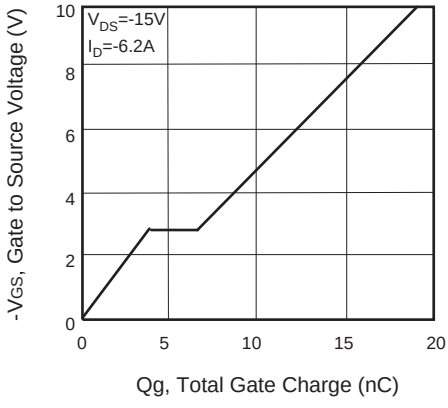

Figure 13. Gate Charge

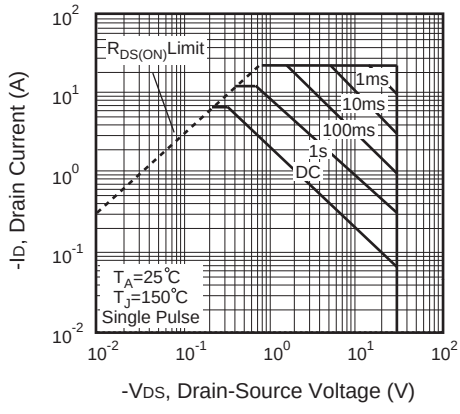

Figure 14. Maximum Safe Operating Area

CHANNEL 2

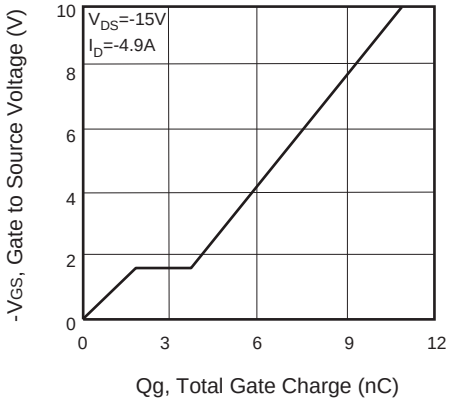

Figure 15. Gate Charge

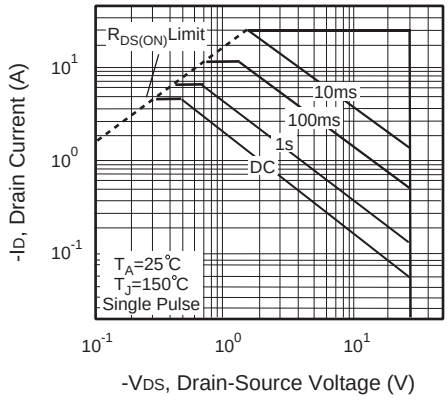

Figure 16. Maximum Safe Operating Area

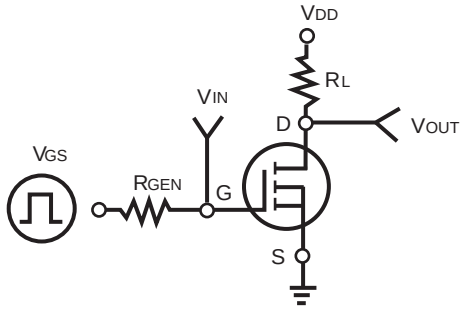

Figure 17. Switching Test Circuit

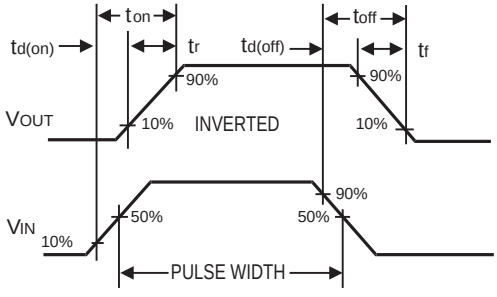

Figure 18. Switching Waveforms

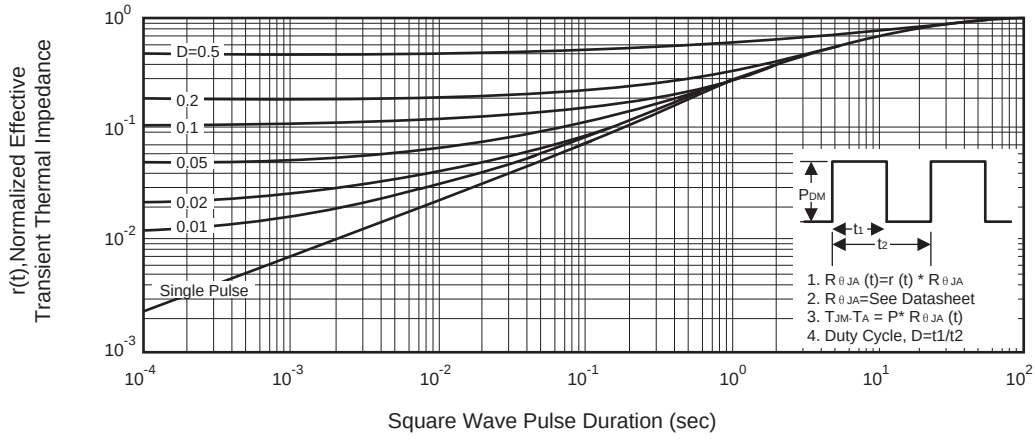

Figure 19. Normalized Thermal Transient Impedance Curve