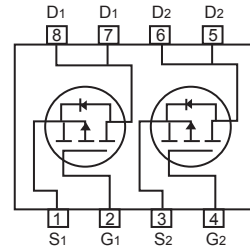
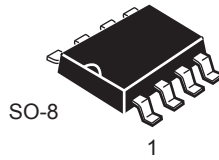


Dual P-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

- -40V, -5A, $R_{DS(ON)} = 44m\Omega$ @ $V_{GS} = -10V$.
 $R_{DS(ON)} = 65m\Omega$ @ $V_{GS} = -4.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead-free plating ; RoHS compliant.
- Surface mount Package.



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-5	A
Drain Current-Pulsed ^a	I_{DM}	-20	A
Maximum Power Dissipation	P_D	2.0	W
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient ^b	$R_{\theta JA}$	62.5	$^\circ C/W$



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Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-40			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40V, V_{GS} = 0V$			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics ^c						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -5.0A$		34	44	$m\Omega$
		$V_{GS} = -4.5V, I_D = -2.5A$		45	65	$m\Omega$
Dynamic Characteristics ^d						
Input Capacitance	C_{iss}	$V_{DS} = -20, V_{GS} = 0V, \square$ $f = 1.0 \text{ MHz}$		1125		pF
Output Capacitance	C_{oss}			150		pF
Reverse Transfer Capacitance	C_{rss}			100		pF
Switching Characteristics ^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -20, I_D = -5A,$ $V_{GS} = -10V, R_{GEN} = 3\Omega$		12	24	ns
Turn-On Rise Time	t_r			5	10	ns
Turn-Off Delay Time	$t_{d(off)}$			33	66	ns
Turn-Off Fall Time	t_f			4	8	ns
Total Gate Charge	Q_g	$V_{DS} = -20V, I_D = -5A,$ $V_{GS} = -10V$		20	26	nC
Gate-Source Charge	Q_{gs}			2.5		nC
Gate-Drain Charge	Q_{gd}			3.5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				-1.5	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = -1A$			-1.3	V
Notes : \square a.Repetitive Rating : Pulse width limited by maximum junction temperature. \square b.Surface Mounted on FR4 Board, $t \leq 10 \text{ sec.}$ \square c.Pulse Test : Pulse Width $\leq 300\mu s,$ Duty Cycle $\leq 2\%.$ \square d.Guaranteed by design, not subject to production testing. \square \square						



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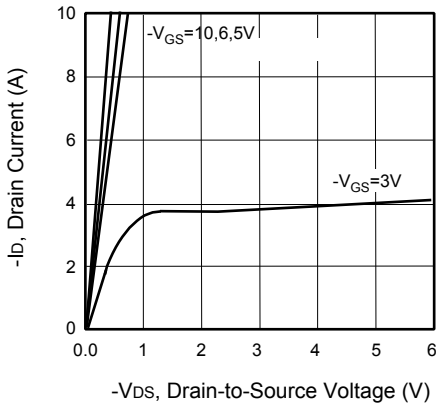


Figure 1. Output Characteristics

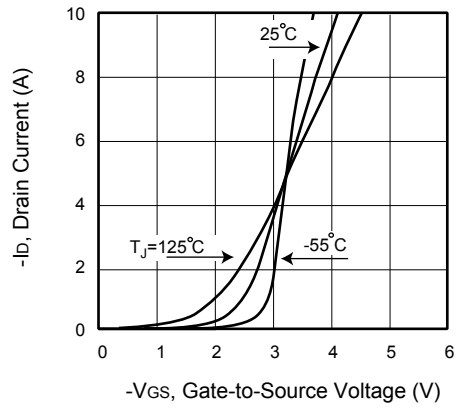


Figure 2. Transfer Characteristics

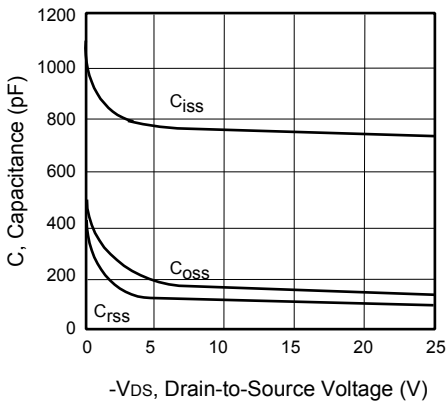


Figure 3. Capacitance

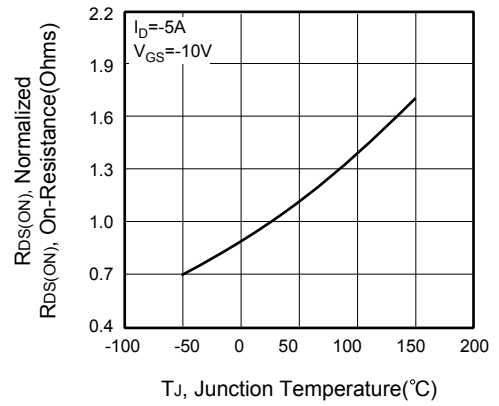


Figure 4. On-Resistance Variation with Temperature

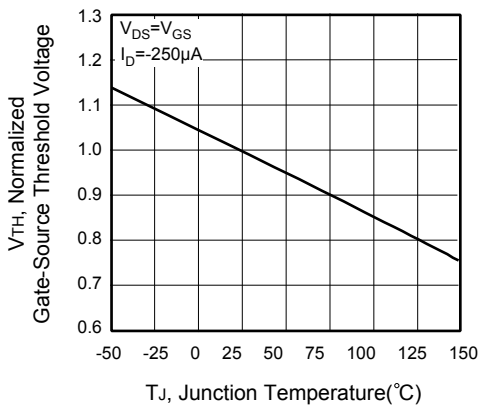


Figure 5. Gate Threshold Variation with Temperature

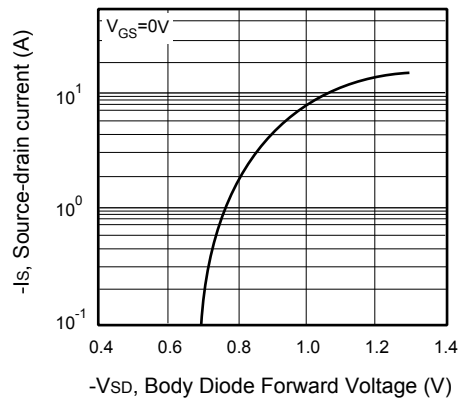


Figure 6. Body Diode Forward Voltage Variation with Source Current



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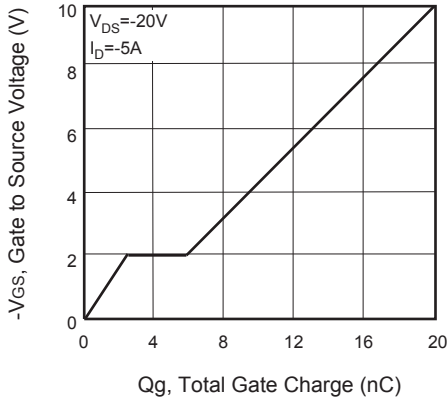


Figure 7. Gate Charge

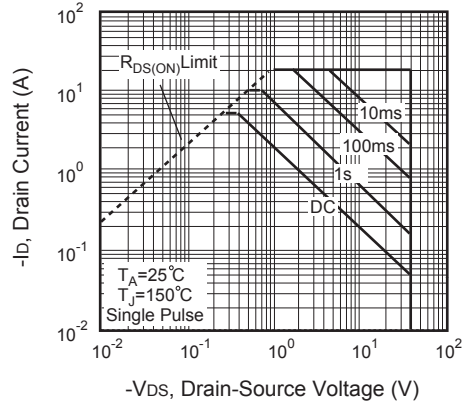


Figure 8. Maximum Safe Operating Area

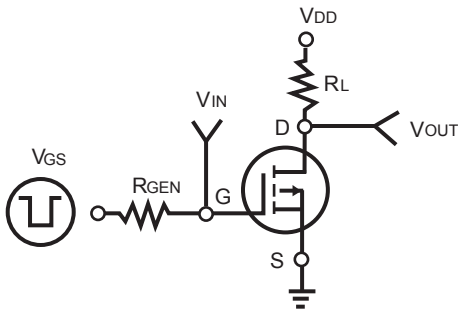


Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

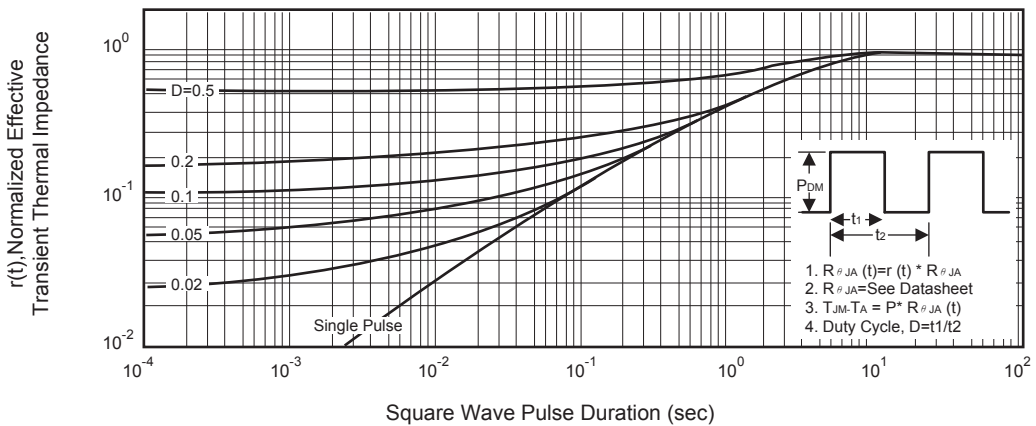


Figure 11. Normalized Thermal Transient Impedance Curve