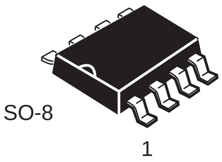
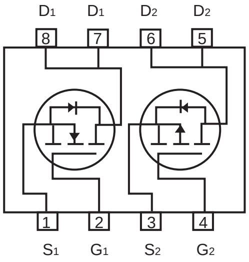
CEM4532

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

FEATURES

- 30V, 4.7A, $R_{DS(ON)}$ = 55mΩ @V_{GS} = 10V.
  $R_{DS(ON)}$ = 85mΩ @V_{GS} = 4.5V.
- -30V, -4.5A, $R_{DS(ON)}$ = 80mΩ @V_{GS} = -10V.
  $R_{DS(ON)}$ = 135mΩ @V_{GS} = -4.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.
- Surface mount Package.





ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current-Continuous	I_D	4.7	-4.5	A
Drain Current-Pulsed [a]	I_{DM}	20	-20	A
Maximum Power Dissipation	P_D	2.0		W
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	62.5	°C/W

N-Channel Electrical Characteristics $T_A = 25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V			1	µA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	IGSSR	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250µA	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 4.7A		40	55	mΩ
		V_{GS} = 4.5V, I_D = 3.7A		70	85	mΩ
Forwand Transconductance	g_{FS}	V_{DS} = 15V, I_D = 4.7A		5		S
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = 15V, V_{GS} = 0V, f = 1.0 MHz		357		pF
Output Capacitance	C_{oss}			190		pF
Reverse Transfer Capacitance	C_{rss}			60		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6Ω		15	30	ns
Turn-On Rise Time	t_r			18	40	ns
Turn-Off Delay Time	$t_{d(off)}$			30	60	ns
Turn-On Fall Time	t_f			5	15	ns
Total Gate Charge	Q_g	V_{DS} = 15V, I_D = 4.7A, V_{GS} = 10V		10.4	15	nC
Gate-Source Charge	Q_{gs}			2.3		nC
Gate-Drain Charge	Q_{gd}			2.8		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				1.7	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = 1.7A			1.2	V

Notes :

a.Repetitive Rating : Pulse width limited by maximum junction temperature.

b.Surface Mounted on FR4 Board, t ≤ 10 sec.

c.Pulse Test : Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.

d.Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics $T_A = 25℃$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250µA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V			-1	µA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	IGSSR	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250µA	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -4.5A		60	80	mΩ
		V_{GS} = -4.5V, I_D = -3.6A		105	135	mΩ
Forwand Transconductance	g_{FS}	V_{DS} = -15V, I_D = -4.5A		5.8		S
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = -15V, V_{GS} = 0V, f = 1.0 MHz		448		pF
Output Capacitance	C_{oss}			317		pF
Reverse Transfer Capacitance	C_{rss}			308		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15V, I_D = -1A, V_{GS} = -10V, R_{GEN} = 6Ω		19	45	ns
Turn-On Rise Time	t_r			19	45	ns
Turn-Off Delay Time	$t_{d(off)}$			38	75	ns
Turn-On Fall Time	t_f			48	95	ns
Total Gate Charge	Q_g	V_{DS} = -15V, I_D = -4.5A, V_{GS} = -10V		18	23	nC
Gate-Source Charge	Q_{gs}			3		nC
Gate-Drain Charge	Q_{gd}			4.5		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				-1.7	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = -1.7A			-1.2	V

Notes :

a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

N-CHANNEL

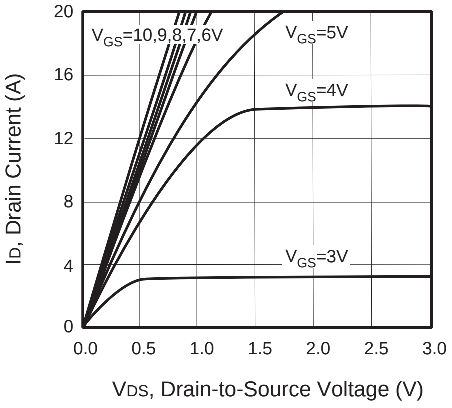


Figure 1. Output Characteristics

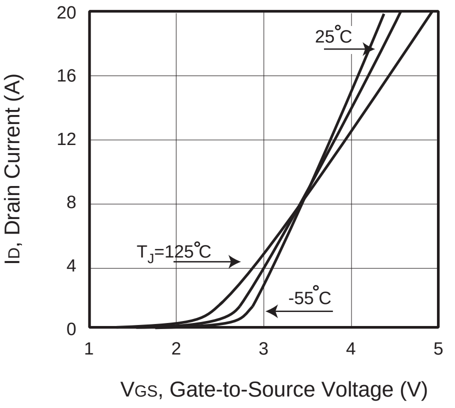


Figure 2. Transfer Characteristics

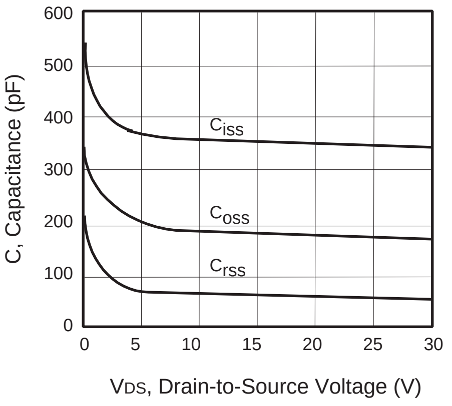


Figure 3. Capacitance

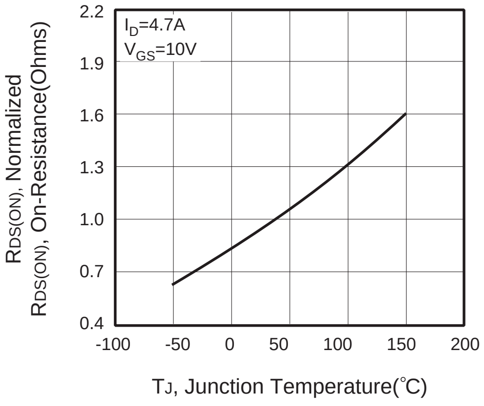


Figure 4. On-Resistance Variation with Temperature

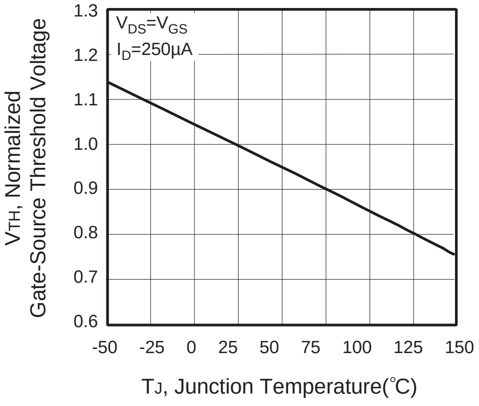


Figure 5. Gate Threshold Variation with Temperature

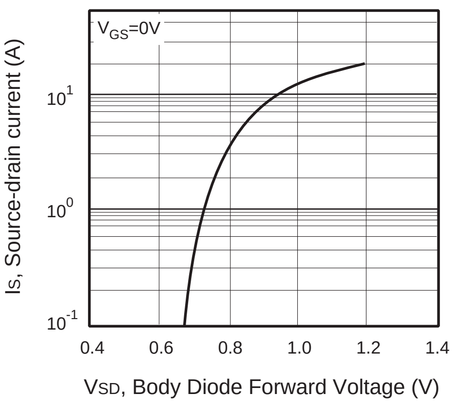


Figure 6. Body Diode Forward Voltage Variation with Source Current

P-CHANNEL

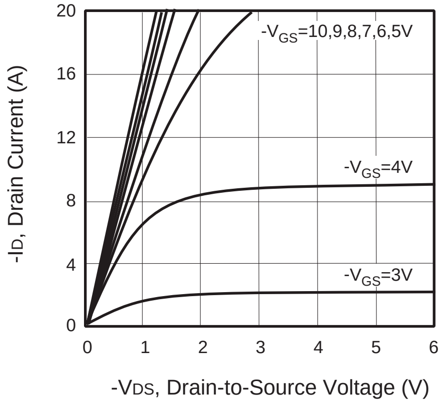


Figure 7. Output Characteristics

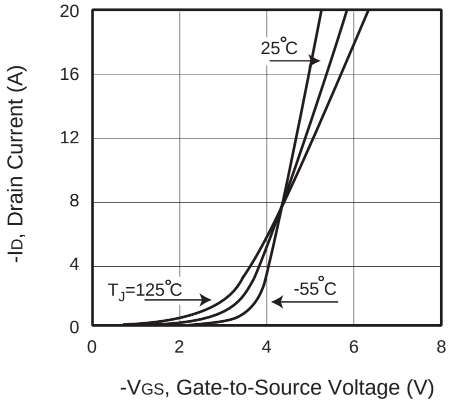


Figure 8. Transfer Characteristics

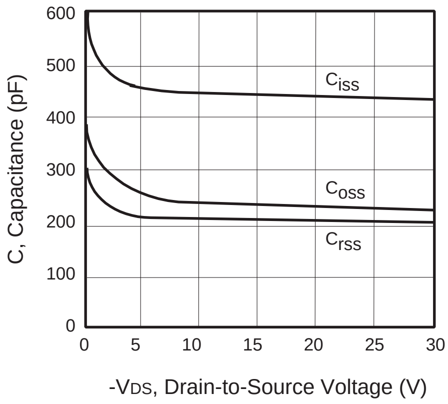


Figure 9. Capacitance

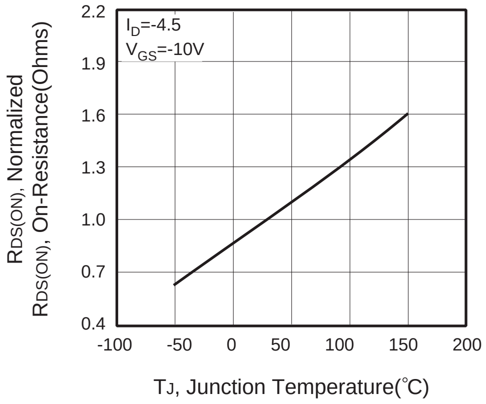


Figure 10. On-Resistance Variation with Temperature

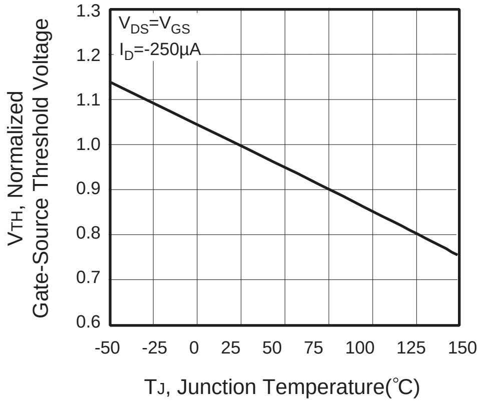


Figure 11. Gate Threshold Variation with Temperature

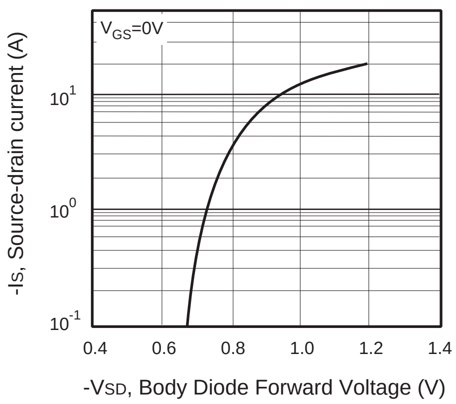


Figure 12. Body Diode Forward Voltage Variation with Source Current

N-CHANNEL

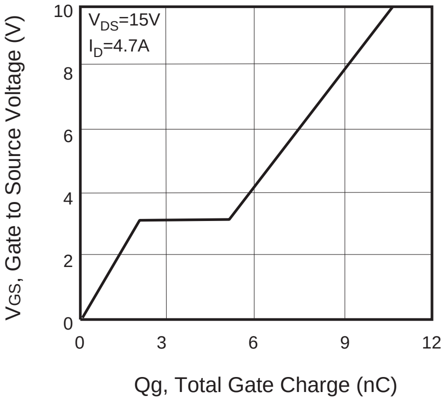


Figure 13. Gate Charge

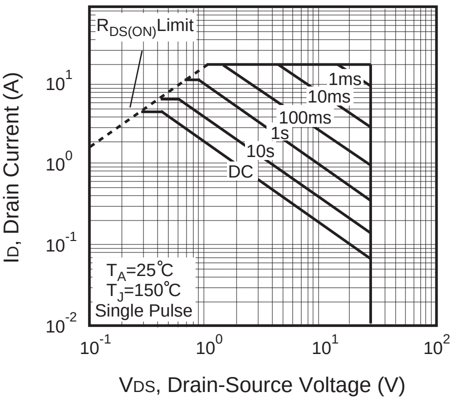


Figure 14. Maximum Safe Operating Area

P-CHANNEL

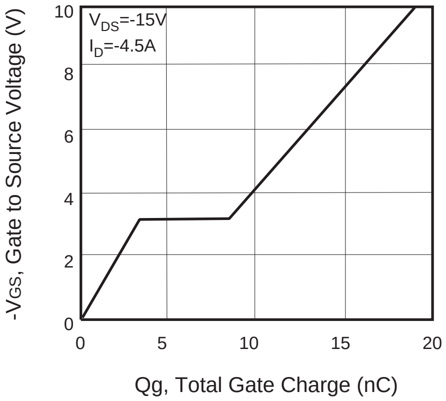


Figure 15. Gate Charge

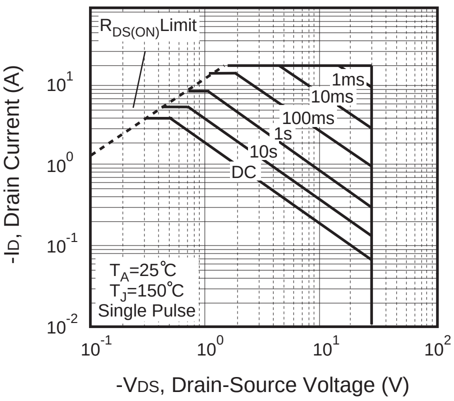


Figure 16. Maximum Safe Operating Area

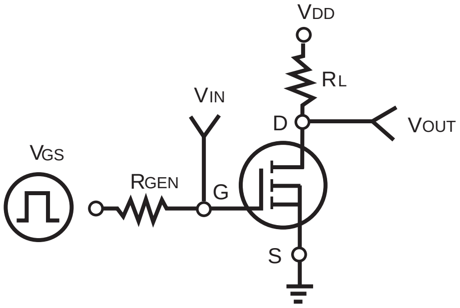


Figure 17. Switching Test Circuit

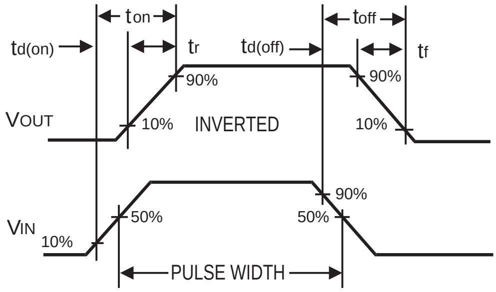


Figure 18. Switching Waveforms

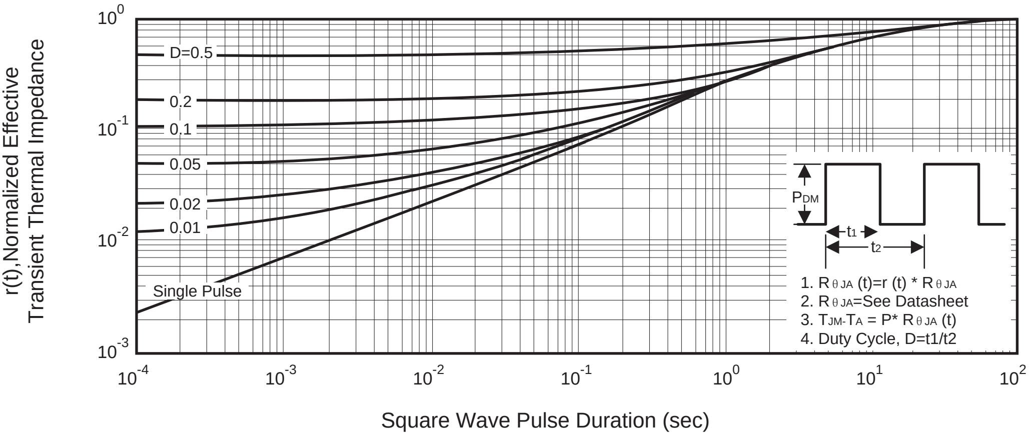


Figure 19. Normalized Thermal Transient Impedance Curve