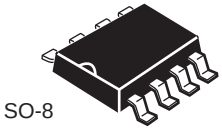
CEM4559

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

FEATURES

- 60V, 4.5A, $R_{DS(ON)}$ = 55mΩ @V_{GS} = 10V.
  $R_{DS(ON)}$ = 75mΩ @V_{GS} = 4.5V.
- -60V, -3.5A, $R_{DS(ON)}$ = 105mΩ @V_{GS} = -10V.
  $R_{DS(ON)}$ = 160mΩ @V_{GS} = -4.5V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead free product is acquired.
- Surface mount Package.



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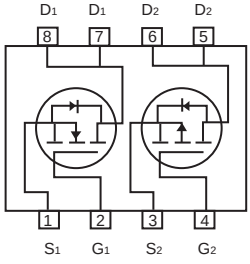

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	60	-60	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current-Continuous	I_D	4.5	-3.5	A
Drain Current-Pulsed [a]	I_{DM}	20	-20	A
Maximum Power Dissipation	P_D	2.0		W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	62.5	°C/W

N-Channel Electrical Characteristics T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 4.5A		42	55	mΩ
		V_{GS} = 4.5V, I_D = 4.0A		55	75	mΩ
Forwand Transconductance	g_{FS}	V_{DS} = 10V, I_D = 4.5A		8		S
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0 MHz		890		pF
Output Capacitance	C_{oss}			173		pF
Reverse Transfer Capacitance	C_{rss}			22		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6Ω		11	25	ns
Turn-On Rise Time	t_r			8	18	ns
Turn-Off Delay Time	$t_{d(off)}$			34	65	ns
Turn-On Fall Time	t_f			9	22	ns
Total Gate Charge	Q_g	V_{DS} = 30V, I_D = 4.5A, V_{GS} = 10V		19	24	nC
Gate-Source Charge	Q_{gs}			2.8		nC
Gate-Drain Charge	Q_{gd}			3.6		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				1.3	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = 1.3A			1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics $T_A = 25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -48V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -3.5A		88	105	mΩ
		V_{GS} = -4.5V, I_D = -3.1A		130	160	mΩ
Forwand Transconductance	g_{FS}	V_{DS} = -5V, I_D = -3.5A		7		S
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = -30V, V_{GS} = 0V, f = 1.0 MHz		780		pF
Output Capacitance	C_{oss}			170		pF
Reverse Transfer Capacitance	C_{rss}			49		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -30V, I_D = -1A, V_{GS} = -10V, R_{GEN} = 6Ω		13	45	ns
Turn-On Rise Time	t_r			9	30	ns
Turn-Off Delay Time	$t_{d(off)}$			48	150	ns
Turn-On Fall Time	t_f			22	75	ns
Total Gate Charge	Q_g	V_{DS} = -30V, I_D = -3.5A, V_{GS} = -10V		21	29	nC
Gate-Source Charge	Q_{gs}			3		nC
Gate-Drain Charge	Q_{gd}			4		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				-1.3	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = -1.3A			-1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

N-CHANNEL

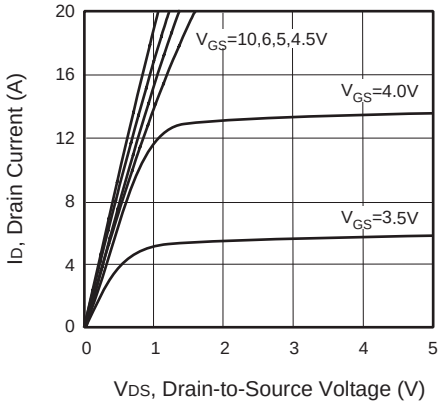

Figure 1. Output Characteristics

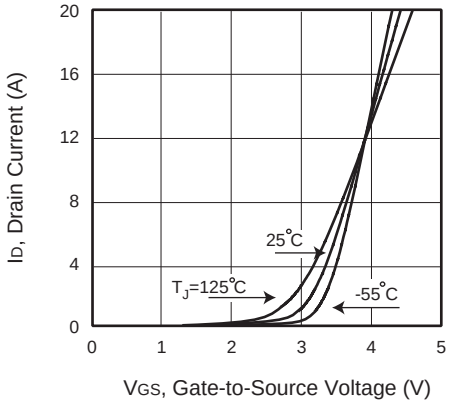

Figure 2. Transfer Characteristics

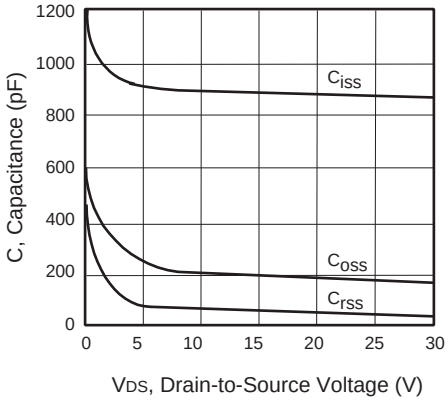

Figure 3. Capacitance

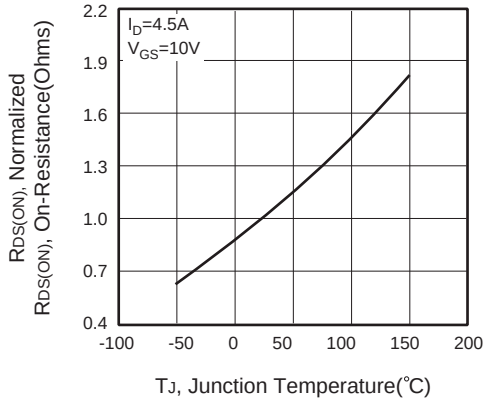

Figure 4. On-Resistance Variation with Temperature

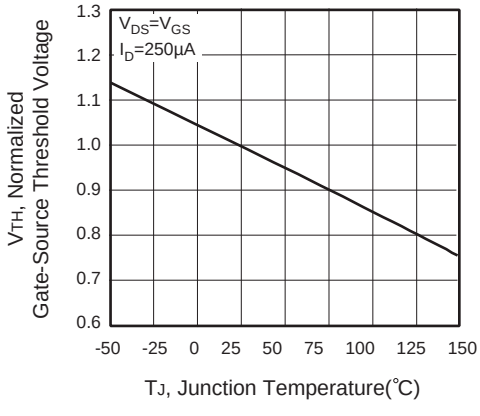

Figure 5. Gate Threshold Variation with Temperature

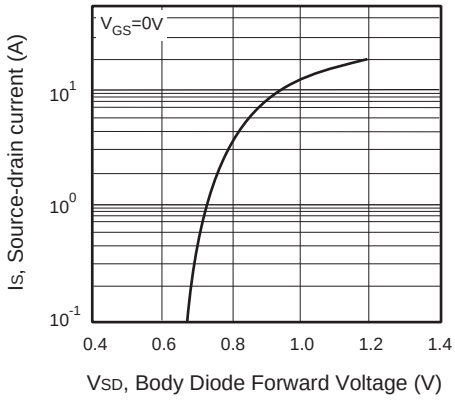

Figure 6. Body Diode Forward Voltage Variation with Source Current

P-CHANNEL

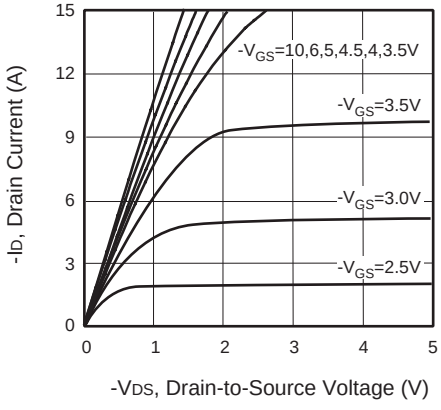

Figure 7. Output Characteristics

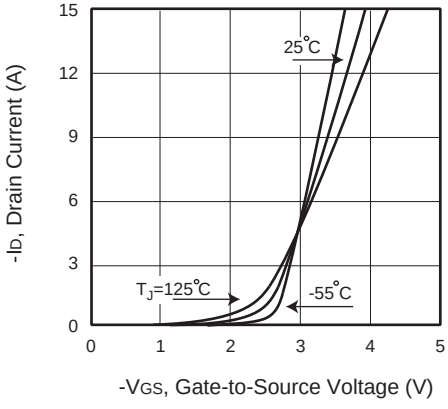

Figure 8. Transfer Characteristics

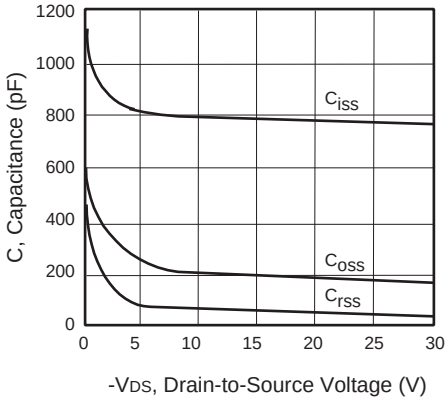

Figure 9. Capacitance

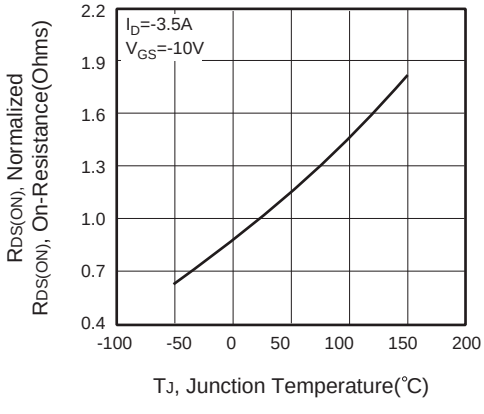

Figure 10. On-Resistance Variation with Temperature

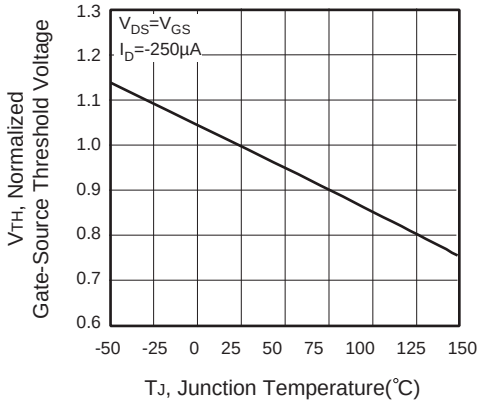

Figure 11. Gate Threshold Variation with Temperature

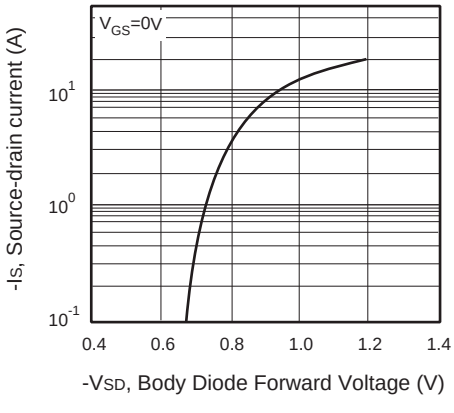

Figure 12. Body Diode Forward Voltage Variation with Source Current

N-CHANNEL

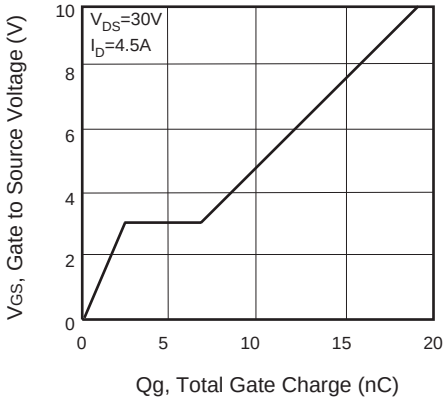

Figure 13. Gate Charge

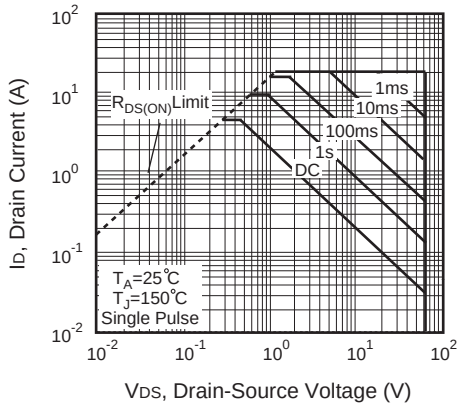

Figure 14. Maximum Safe Operating Area

P-CHANNEL

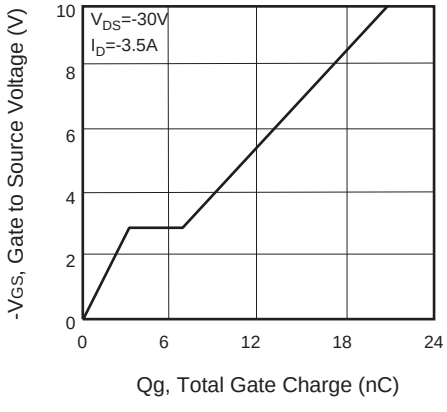

Figure 15. Gate Charge

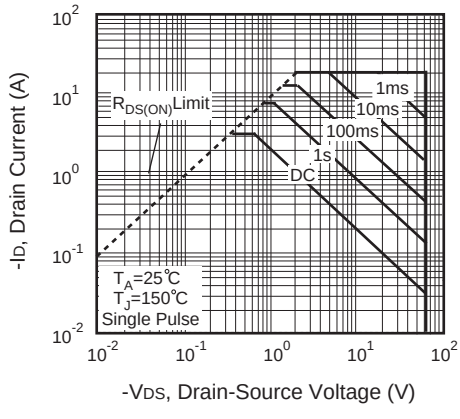

Figure 16. Maximum Safe Operating Area

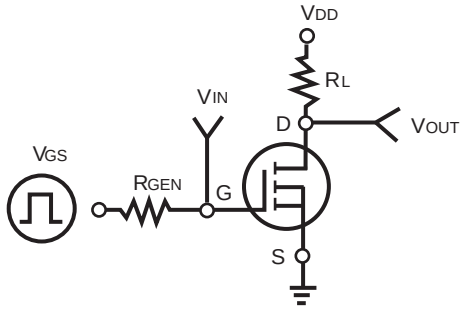

Figure 17. Switching Test Circuit

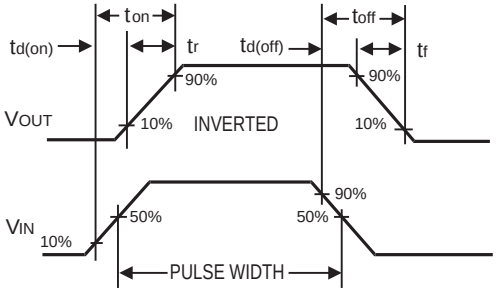

Figure 18. Switching Waveforms

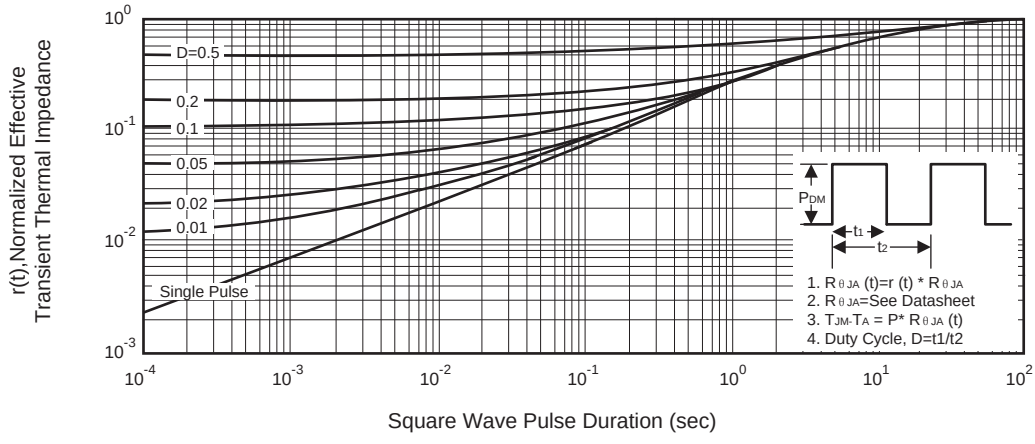

Figure 19. Normalized Thermal Transient Impedance Curve