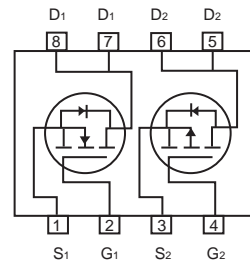
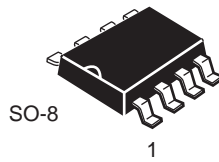


## Dual Enhancement Mode Field Effect Transistor (N and P Channel)

### FEATURES

- 30V, 7.3A,  $R_{DS(ON)} = 18m\Omega$  (typ) @  $V_{GS} = 10V$ .  
 $R_{DS(ON)} = 26m\Omega$  (typ) @  $V_{GS} = 4.5V$ .
- -30V, -4.6A,  $R_{DS(ON)} = 45m\Omega$  (typ) @  $V_{GS} = -10V$ .  
 $R_{DS(ON)} = 72m\Omega$  (typ) @  $V_{GS} = -4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- Surface mount Package.



### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	$V_{DS}$	30	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Drain Current-Continuous	$I_D$	7.3	-4.6	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	30	-20	A
Maximum Power Dissipation	$P_D$	2.0		W
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	62.5	$^\circ C/W$



# CEM4600

## N-Channel Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

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Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics <sup>c</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 7.3A$		18	22	$m\Omega$
		$V_{GS} = 4.5V, I_D = 6.3A$		26	32	$m\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 15V, I_D = 7.3A$		10		S
<b>Dynamic Characteristics <sup>d</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 15V, V_{GS} = 0V, f = 1.0\text{ MHz}$		750		pF
Output Capacitance	$C_{oss}$			360		pF
Reverse Transfer Capacitance	$C_{rss}$			110		pF
<b>Switching Characteristics <sup>d</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6\Omega$		22	45	ns
Turn-On Rise Time	$t_r$			34	70	ns
Turn-Off Delay Time	$t_{d(off)}$			43	90	ns
Turn-On Fall Time	$t_f$			18	35	ns
Total Gate Charge	$Q_g$	$V_{DS} = 15V, I_D = 7.3A, V_{GS} = 10V$		21	28	nC
Gate-Source Charge	$Q_{gs}$			2.6		nC
Gate-Drain Charge	$Q_{gd}$			4.4		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				2.3	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 2.3A$			1.3	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10$ sec. c.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . d.Guaranteed by design, not subject to production testing.						



# CEM4600

## P-Channel Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30V, V_{GS} = 0V$			-1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics <sup>c</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1		-3	V
Static Drain-Source	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -4.6A$		45	55	$m\Omega$
On-Resistance		$V_{GS} = -4.5V, I_D = -4A$		72	90	$m\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = -15V, I_D = -4.6A$		6.5		S
<b>Dynamic Characteristics <sup>d</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -15V, V_{GS} = 0V,$ $f = 1.0\text{ MHz}$		1040		pF
Output Capacitance	$C_{oss}$			420		pF
Reverse Transfer Capacitance	$C_{rss}$			150		pF
<b>Switching Characteristics <sup>d</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15V, I_D = -1A,$ $V_{GS} = -10V, R_{GEN} = 6\Omega$		19	48	ns
Turn-On Rise Time	$t_r$			10	30	ns
Turn-Off Delay Time	$t_{d(off)}$			74	135	ns
Turn-On Fall Time	$t_f$			36	75	ns
Total Gate Charge	$Q_g$	$V_{DS} = -15V, I_D = -4.6A,$ $V_{GS} = -10V$		23	29	nC
Gate-Source Charge	$Q_{gs}$			2		nC
Gate-Drain Charge	$Q_{gd}$			6		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				-2.3	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = -2.3A$			-1.3	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10$ sec. c.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . d.Guaranteed by design, not subject to production testing.						



# CEM4600

## N-CHANNEL

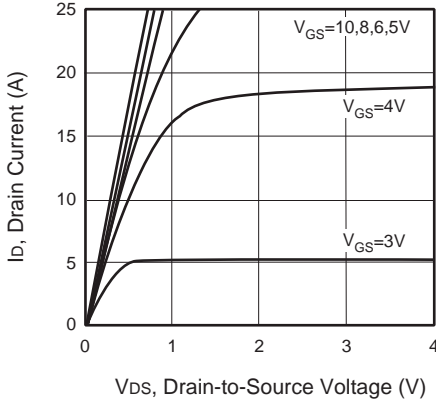


Figure 1. Output Characteristics

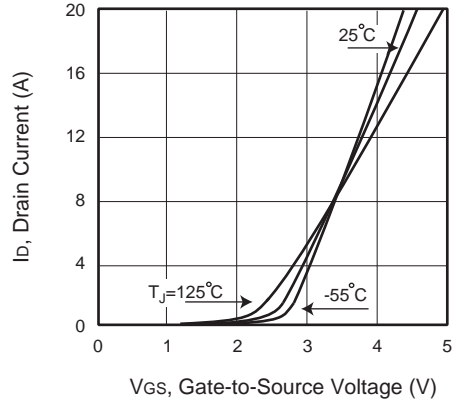


Figure 2. Transfer Characteristics

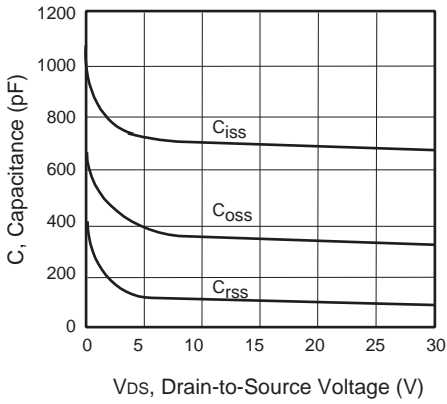


Figure 3. Capacitance

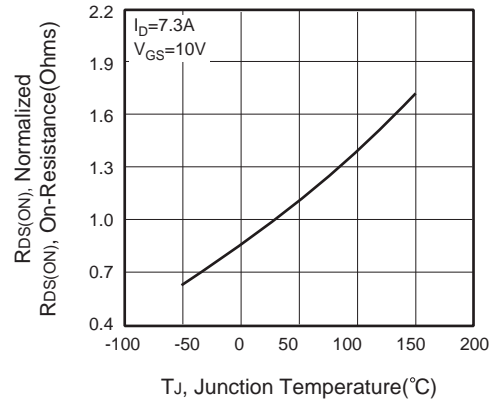


Figure 4. On-Resistance Variation with Temperature

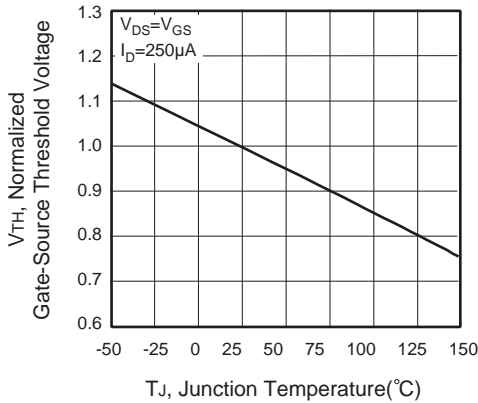


Figure 5. Gate Threshold Variation with Temperature

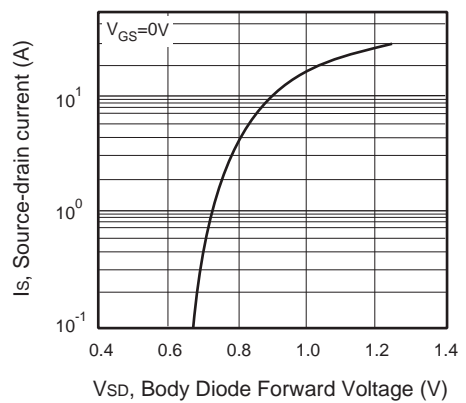


Figure 6. Body Diode Forward Voltage Variation with Source Current



# CEM4600

## P-CHANNEL

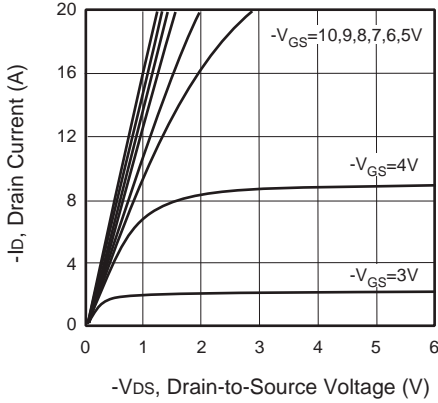


Figure 7. Output Characteristics

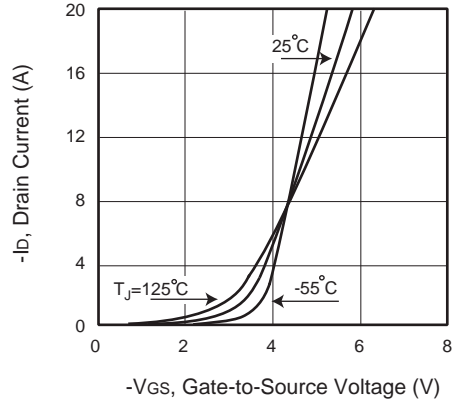


Figure 8. Transfer Characteristics

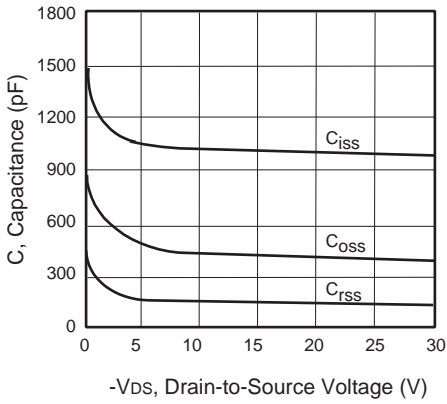


Figure 9. Capacitance

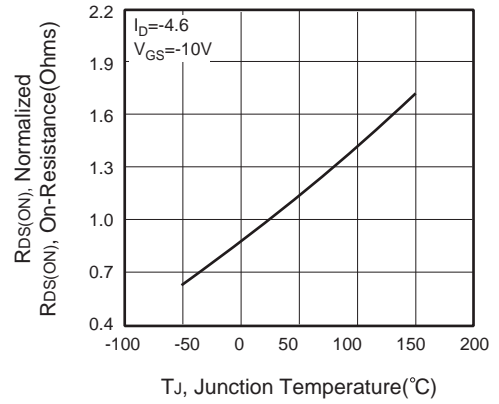


Figure 10. On-Resistance Variation with Temperature

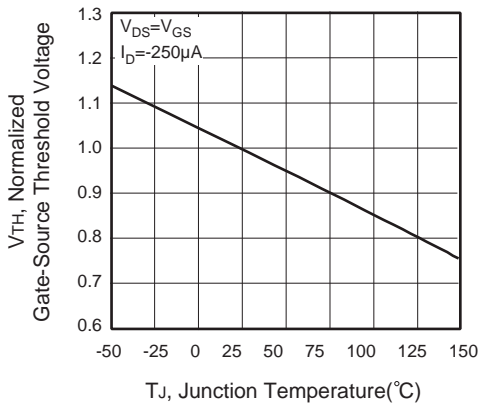


Figure 11. Gate Threshold Variation with Temperature

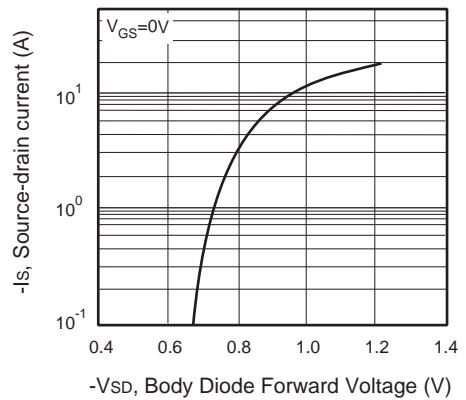


Figure 12. Body Diode Forward Voltage Variation with Source Current



# CEM4600

## N-CHANNEL

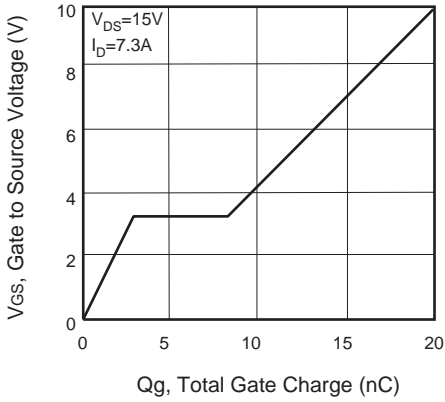


Figure 13. Gate Charge

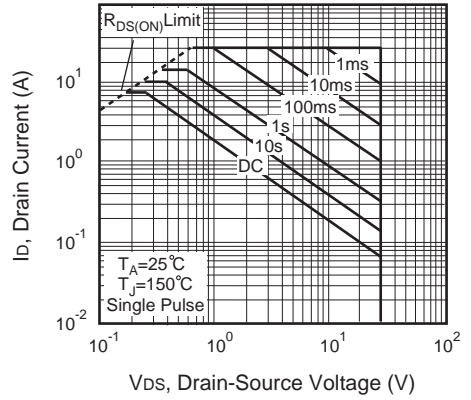


Figure 14. Maximum Safe Operating Area

## P-CHANNEL

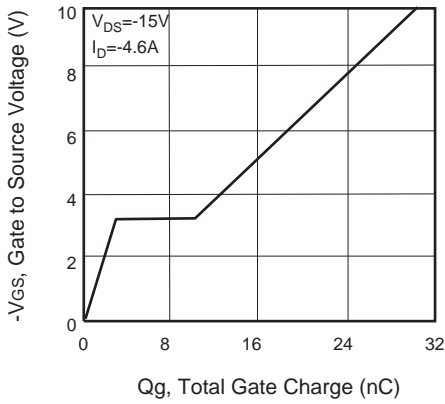


Figure 15. Gate Charge

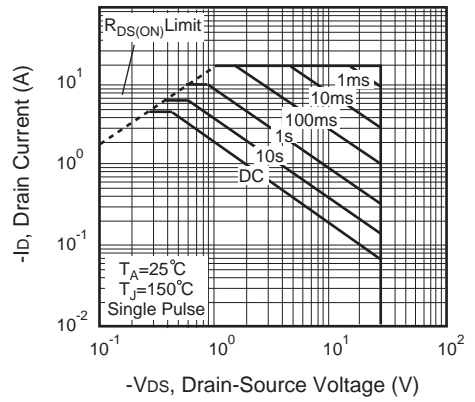


Figure 16. Maximum Safe Operating Area

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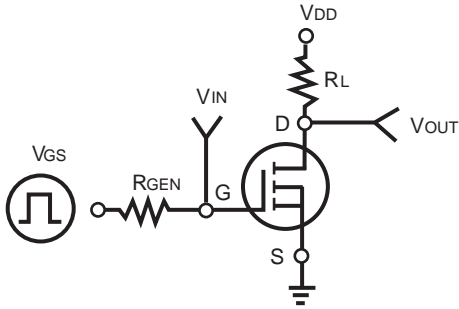


Figure 17. Switching Test Circuit

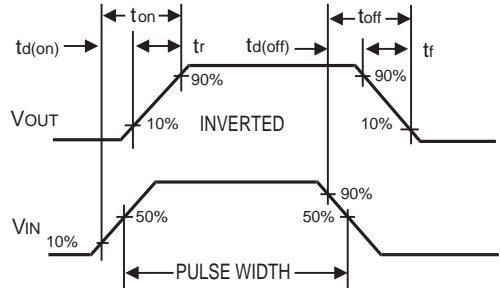


Figure 18. Switching Waveforms

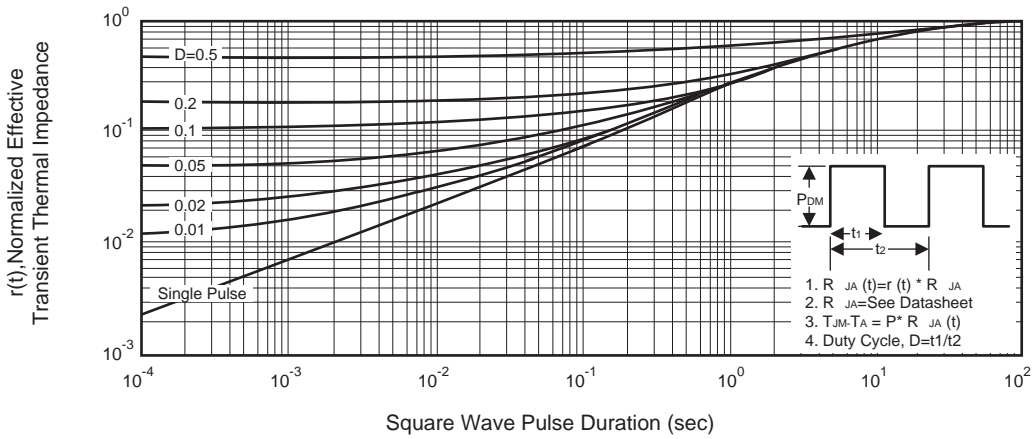


Figure 19. Normalized Thermal Transient Impedance Curve