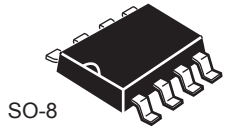
CEM7350L

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

FEATURES

- 100V, 2.6A, $R_{DS(ON)}$ = 190mΩ @V_{GS} = 5V.
  $R_{DS(ON)}$ = 180mΩ @V_{GS} = 10V.
- -100V, -2.0A, $R_{DS(ON)}$ = 320mΩ @V_{GS} = -10V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- Lead-free plating ; RoHS compliant.
- Surface mount Package.



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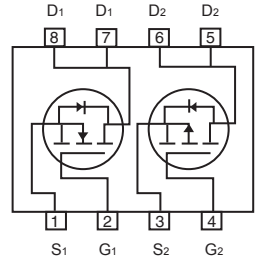

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	100	-100	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current-Continuous	I_D	2.6	-2.0	A
Drain Current-Pulsed [a]	I_{DM}	10.4	-8.0	A
Maximum Power Dissipation	P_D	2.0		W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	62.5	°C/W

N-Channel Electrical Characteristics T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 1.3A		140	180	mΩ
		V_{GS} = 5V , I_D = 1A		150	190	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0 MHz		465		pF
Output Capacitance	C_{oss}			85		pF
Reverse Transfer Capacitance	C_{rss}			25		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50V, I_D = 1.3A, V_{GS} = 10V, R_{GEN} = 22Ω		10	20	ns
Turn-On Rise Time	t_r			3	6	ns
Turn-Off Delay Time	$t_{d(off)}$			53	106	ns
Turn-Off Fall Time	t_f			8	16	ns
Total Gate Charge	Q_g	V_{DS} = 80V, I_D = 1.3A, V_{GS} = 10V		12.3	16	nC
Gate-Source Charge	Q_{gs}			0.8		nC
Gate-Drain Charge	Q_{gd}			2.7		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				1.6	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = 2.6A			1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-2		-4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -1.5A		250	320	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = -25V, V_{GS} = 0V, f = 1.0 MHz		575		pF
Output Capacitance	C_{oss}			115		pF
Reverse Transfer Capacitance	C_{rss}			30		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -50V, I_D = -1A, V_{GS} = -10V, R_{GEN} = 22Ω		15	30	ns
Turn-On Rise Time	t_r			11	22	ns
Turn-Off Delay Time	$t_{d(off)}$			57	114	ns
Turn-Off Fall Time	t_f			20	40	ns
Total Gate Charge	Q_g	V_{DS} = -80V, I_D = -1.5A, V_{GS} = -10V		14	18	nC
Gate-Source Charge	Q_{gs}			2.5		nC
Gate-Drain Charge	Q_{gd}			5.0		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				-1.6	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = -2A			-1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

N-CHANNEL

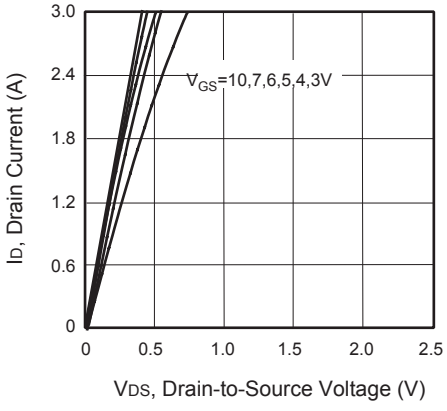

Figure 1. Output Characteristics

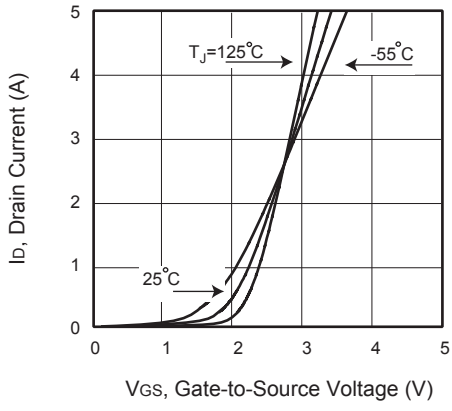

Figure 2. Transfer Characteristics

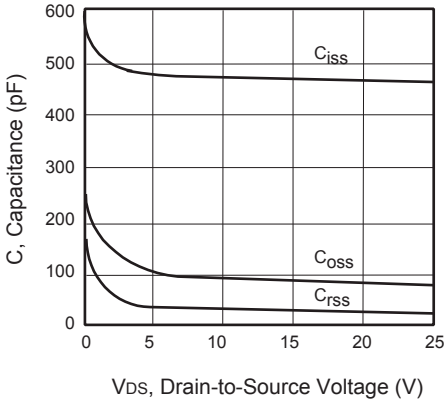

Figure 3. Capacitance

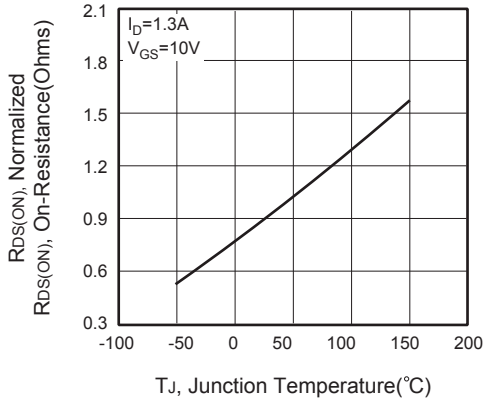

Figure 4. On-Resistance Variation with Temperature

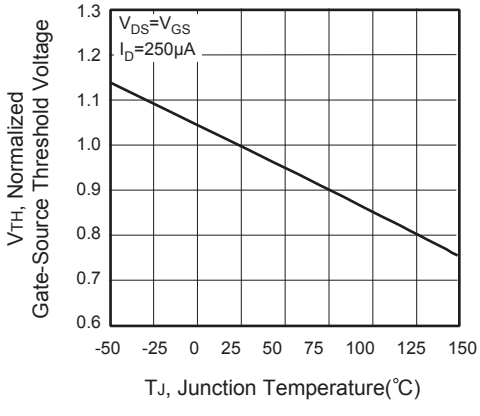

Figure 5. Gate Threshold Variation with Temperature

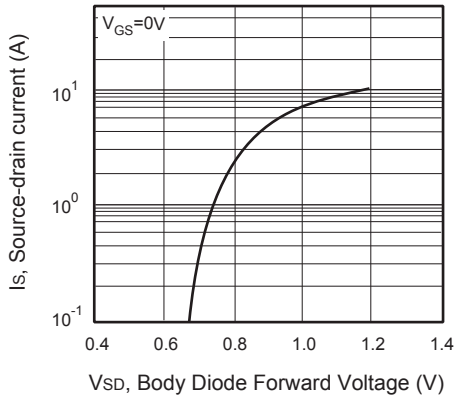

Figure 6. Body Diode Forward Voltage Variation with Source Current

P-CHANNEL

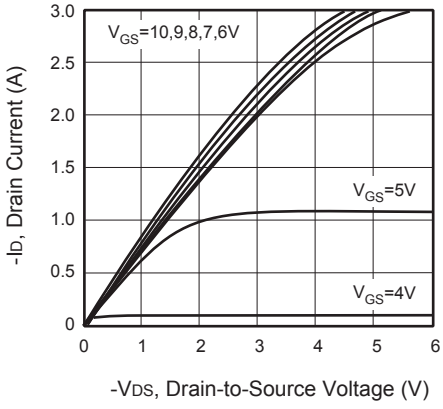

Figure 7. Output Characteristics

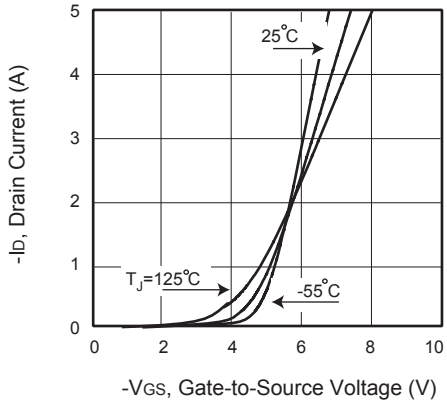

Figure 8. Transfer Characteristics

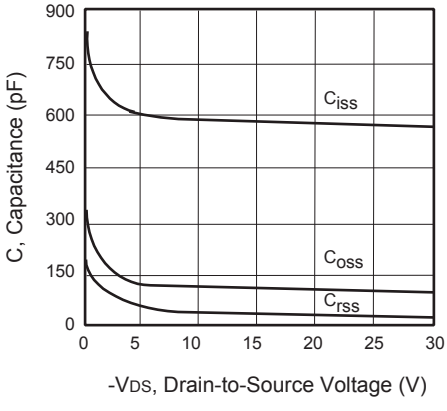

Figure 9. Capacitance

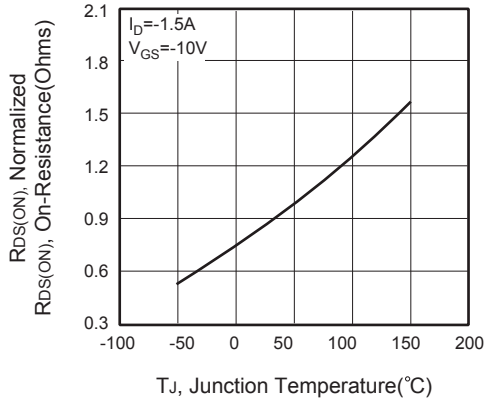

Figure 10. On-Resistance Variation with Temperature

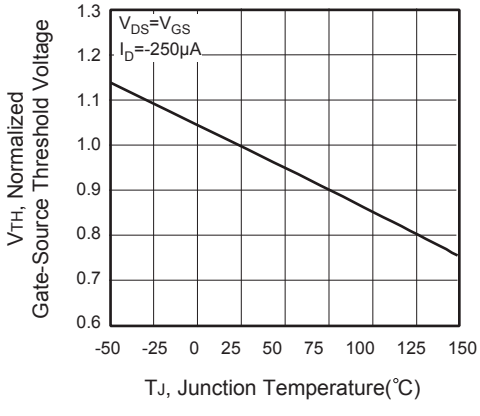

Figure 11. Gate Threshold Variation with Temperature

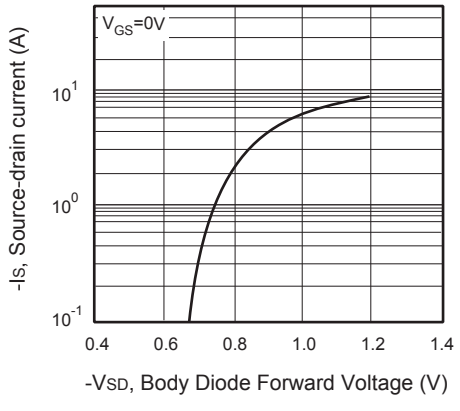

Figure 12. Body Diode Forward Voltage Variation with Source Current

N-CHANNEL

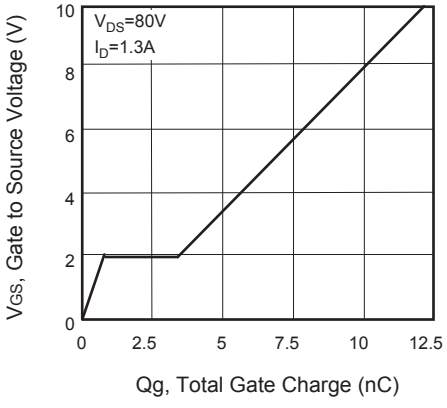

Figure 13. Gate Charge

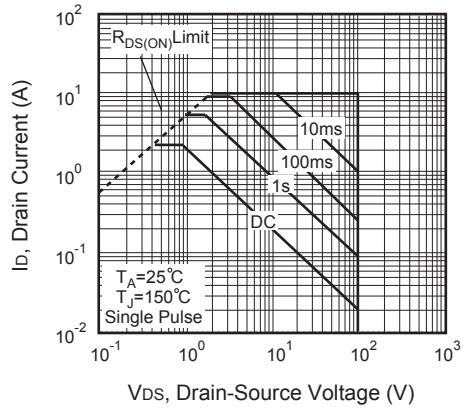

Figure 14. Maximum Safe Operating Area

P-CHANNEL

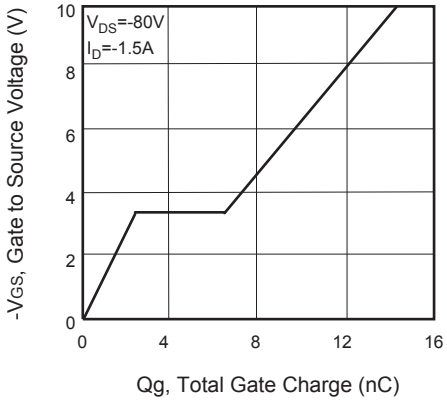

Figure 15. Gate Charge

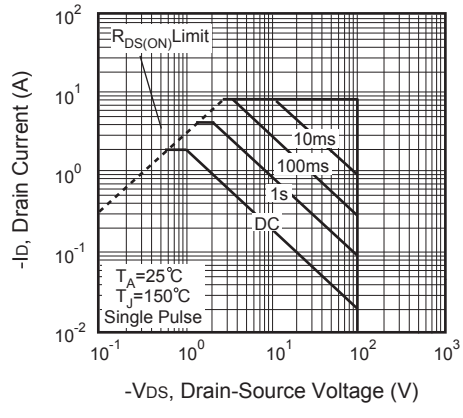

Figure 16. Maximum Safe Operating Area

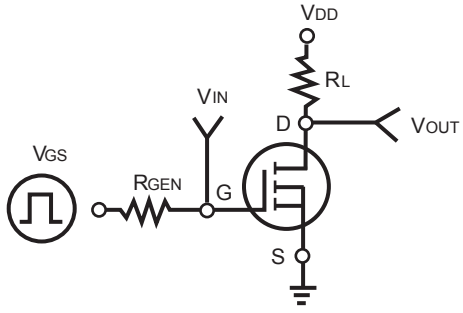

Figure 17. Switching Test Circuit

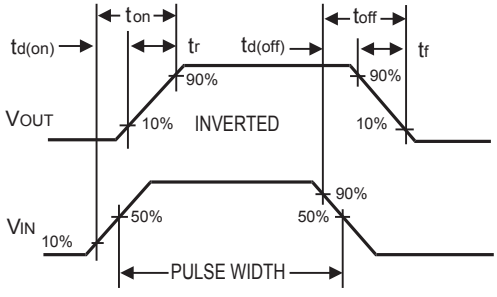

Figure 18. Switching Waveforms

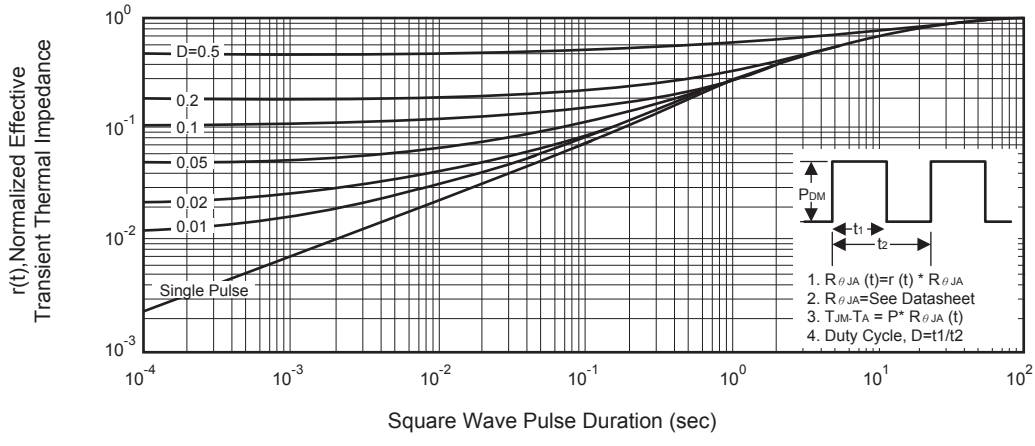

Figure 19. Normalized Thermal Transient Impedance Curve