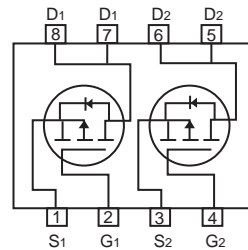
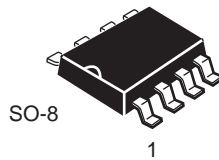


## Dual P-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- -30V, -5.9A,  $R_{DS(ON)} = 36m\Omega$  @  $V_{GS} = -10V$ .  
 $R_{DS(ON)} = 60m\Omega$  @  $V_{GS} = -4.5V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- Surface mount Package.



### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-5.9	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	-20	A
Maximum Power Dissipation	$P_D$	2.0	W
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient <sup>b</sup>	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

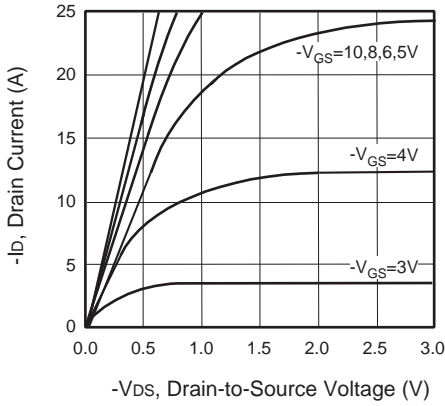


## Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

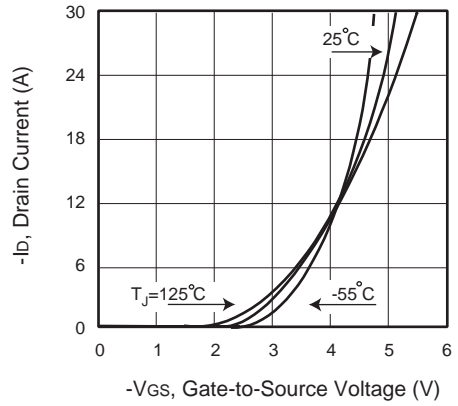
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -24V, V_{GS} = 0V$			-1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>c</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -5.3A$		30	36	$m\Omega$
		$V_{GS} = -4.5V, I_D = -2.0A$		45	60	$m\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = -15V, I_D = -5.3A$		8		S
<b>Dynamic Characteristics<sup>d</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = -15V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1300		pF
Output Capacitance	$C_{oss}$			300		pF
Reverse Transfer Capacitance	$C_{rss}$			150		pF
<b>Switching Characteristics<sup>d</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15V, I_D = -1A, V_{GS} = -10V, R_{GEN} = 6\Omega$		10	20	ns
Turn-On Rise Time	$t_r$			4	10	ns
Turn-Off Delay Time	$t_{d(off)}$			58	80	ns
Turn-On Fall Time	$t_f$			23	30	ns
Total Gate Charge	$Q_g$	$V_{DS} = -15V, I_D = -5.3A, V_{GS} = -10V$		20	25	nC
Gate-Source Charge	$Q_{gs}$			3		nC
Gate-Drain Charge	$Q_{gd}$			5		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current <sup>b</sup>	$I_S$				-2.3	A
Drain-Source Diode Forward Voltage <sup>c</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = -2.3A$			-1.2	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature. b.Surface Mounted on FR4 Board, $t \leq 10\text{ sec}$ . c.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . d.Guaranteed by design, not subject to production testing.						



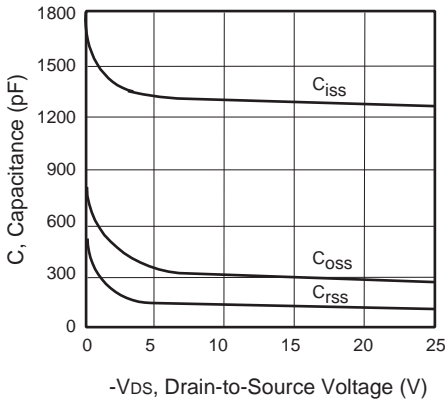
# CEM8531



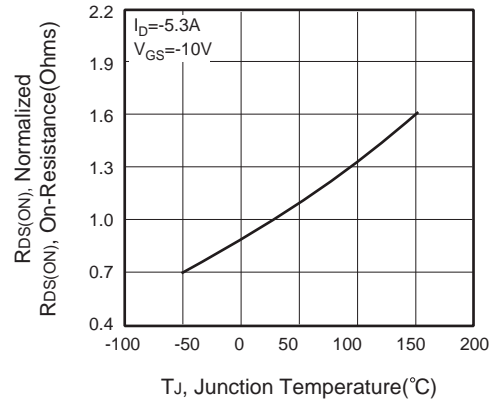
**Figure 1. Output Characteristics**



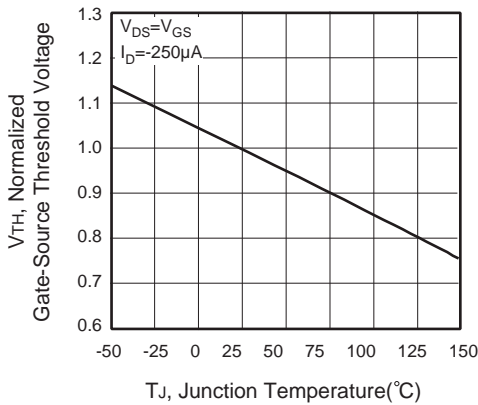
**Figure 2. Transfer Characteristics**



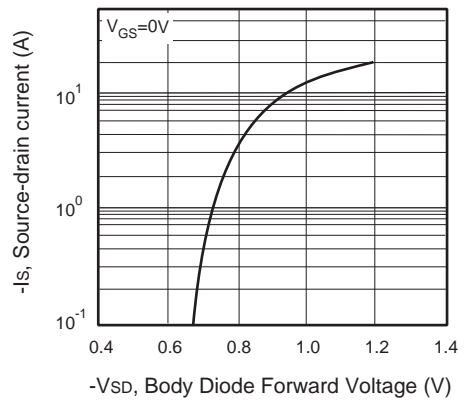
**Figure 3. Capacitance**



**Figure 4. On-Resistance Variation with Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Body Diode Forward Voltage Variation with Source Current**



# CEM8531

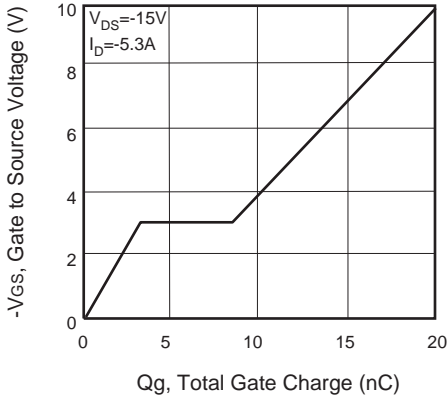


Figure 7. Gate Charge

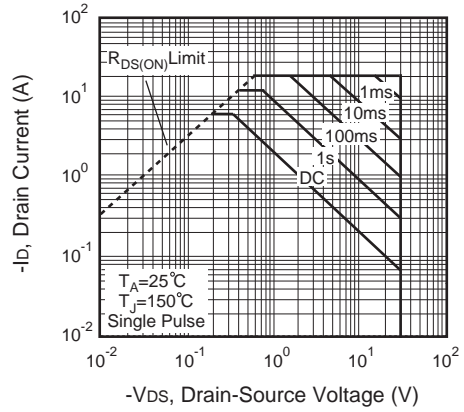


Figure 8. Maximum Safe Operating Area

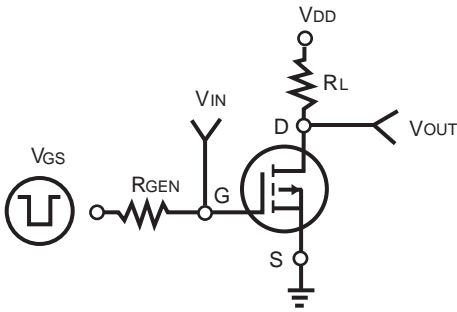


Figure 9. Switching Test Circuit

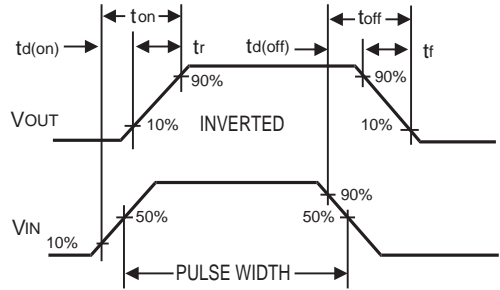


Figure 10. Switching Waveforms

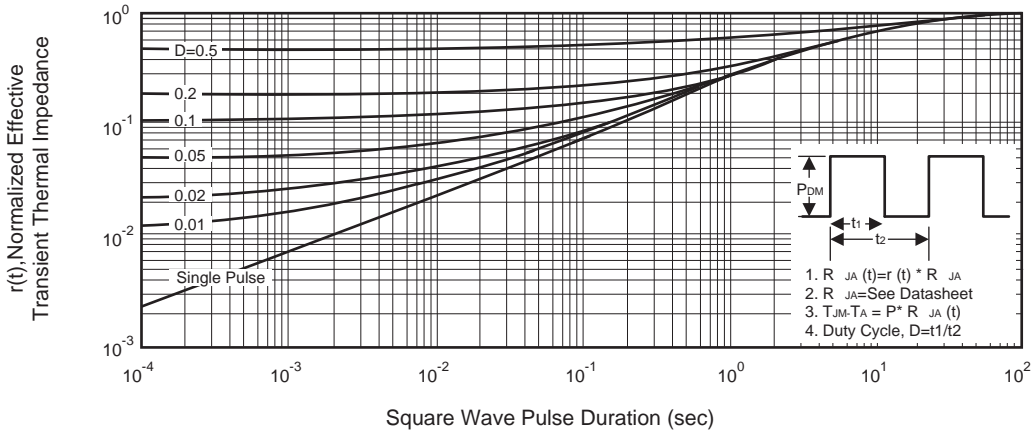


Figure 11. Normalized Thermal Transient Impedance Curve