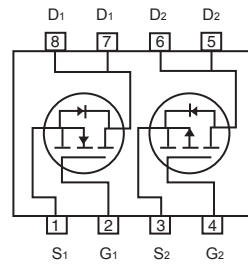
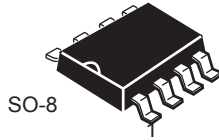


Dual Enhancement Mode Field Effect Transistor (N and P Channel)

PRELIMINARY

FEATURES

- 30V, 7A, $R_{DS(ON)} = 28m\Omega$ @ $V_{GS} = 10V$.
 $R_{DS(ON)} = 40m\Omega$ @ $V_{GS} = 4.5V$.
- -30V, -4.8A, $R_{DS(ON)} = 58m\Omega$ @ $V_{GS} = -10V$.
 $R_{DS(ON)} = 85m\Omega$ @ $V_{GS} = -4.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead free product is acquired.
- Surface mount Package.



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Drain Current-Continuous	I_D	7	-4.8	A
Drain Current-Pulsed ^a	I_{DM}	28	-19	A
Maximum Power Dissipation	P_D	2.0		W
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ C$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient ^b	$R_{\theta JA}$	62.5	$^\circ C/W$

This is preliminary information on a new product in development now .
 Details are subject to change without notice .

Rev 2. 2007.Sep.
<http://www.cetsemi.com>



CEM8958G

N-Channel Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 7A$		22	28	$m\Omega$
		$V_{GS} = 4.5V, I_D = 6A$		30	40	$m\Omega$
Dynamic Characteristics ^d						
Forward Transconductance	g_{FS}	$V_{DS} = 5V, I_D = 7A$		25		S
Input Capacitance	C_{iss}	$V_{DS} = 15V, V_{GS} = 0V, f = 1.0\text{ MHz}$		605		pF
Output Capacitance	C_{oss}			145		pF
Reverse Transfer Capacitance	C_{rss}			92		pF
Switching Characteristics ^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 2.7\Omega$		9	20	ns
Turn-On Rise Time	t_r			4	10	ns
Turn-Off Delay Time	$t_{d(off)}$			24	50	ns
Turn-Off Fall Time	t_f			4	10	ns
Total Gate Charge	Q_g	$V_{DS} = 15V, I_D = 5.8A, V_{GS} = 10V$		12.3	16	nC
Gate-Source Charge	Q_{gs}			1.5		nC
Gate-Drain Charge	Q_{gd}			2.5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				1.3	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = 1.3A$			1.2	V
Notes : <input type="checkbox"/> a.Repetitive Rating : Pulse width limited by maximum junction temperature. <input type="checkbox"/> b.Surface Mounted on FR4 Board, $t \leq 10\text{ sec.}$ <input type="checkbox"/> c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. <input type="checkbox"/> d.Guaranteed by design, not subject to production testing. <input type="checkbox"/> <input type="checkbox"/>						



CEM8958G

P-Channel Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30V, V_{GS} = 0V$			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-1		-3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -4.8A$		48	58	$m\Omega$
		$V_{GS} = -4.5V, I_D = -3.5A$		64	85	$m\Omega$
Dynamic Characteristics ^d						
Forward Transconductance	g_{FS}	$V_{DS} = -10V, I_D = -4.8A$		3		S
Input Capacitance	C_{iss}	$V_{DS} = -15V, V_{GS} = 0V, f = 1.0\text{ MHz}$		555		pF
Output Capacitance	C_{oss}			95		pF
Reverse Transfer Capacitance	C_{rss}			65		pF
Switching Characteristics ^d						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15V, I_D = -1A, V_{GS} = -10V, R_{GEN} = 6\Omega$		12	24	ns
Turn-On Rise Time	t_r			4	8	ns
Turn-Off Delay Time	$t_{d(off)}$			24	48	ns
Turn-Off Fall Time	t_f			5	10	ns
Total Gate Charge	Q_g	$V_{DS} = -15V, I_D = -4.8A, V_{GS} = -10V$		9.3	12.4	nC
Gate-Source Charge	Q_{gs}			3.2		nC
Gate-Drain Charge	Q_{gd}			1.5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current ^b	I_S				-4.5	A
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = -4.8A$			-1.3	V
Notes : <input type="checkbox"/> a.Repetitive Rating : Pulse width limited by maximum junction temperature. <input type="checkbox"/> b.Surface Mounted on FR4 Board, $t \leq 10\text{ sec.}$ <input type="checkbox"/> c.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. <input type="checkbox"/> d.Guaranteed by design, not subject to production testing. <input type="checkbox"/> <input type="checkbox"/>						



CEM8958G

N-CHANNEL

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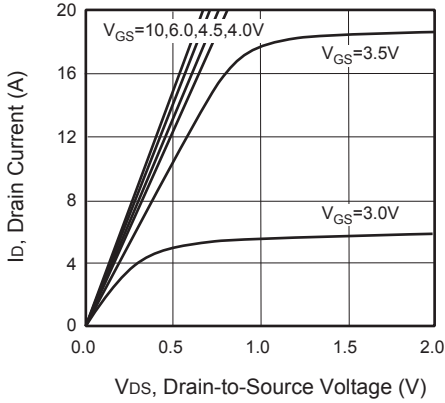


Figure 1. Output Characteristics

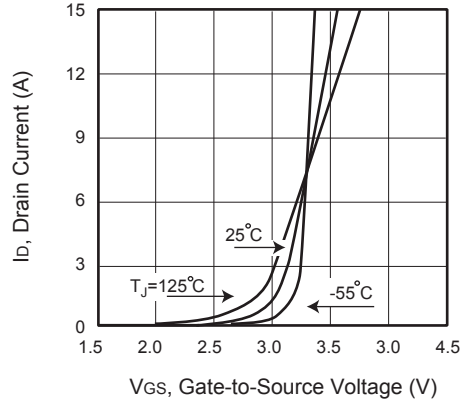


Figure 2. Transfer Characteristics

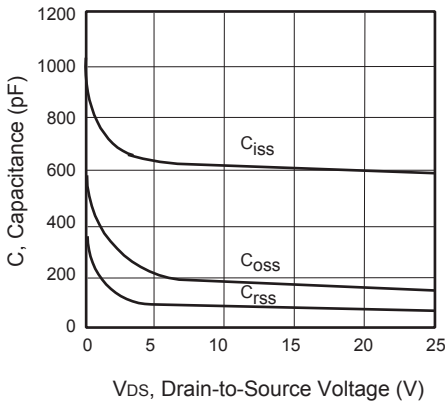


Figure 3. Capacitance

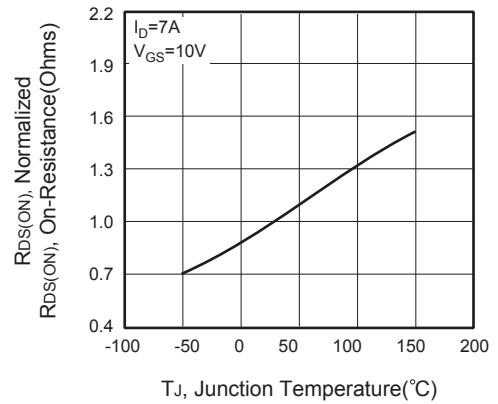


Figure 4. On-Resistance Variation with Temperature

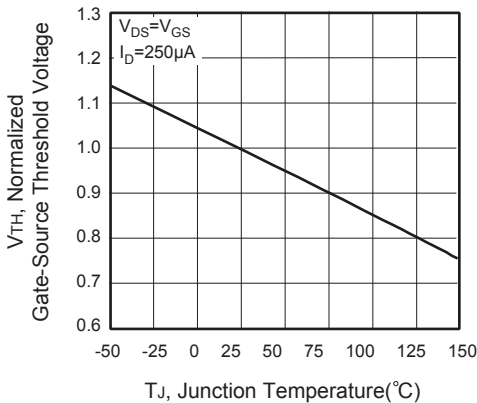


Figure 5. Gate Threshold Variation with Temperature

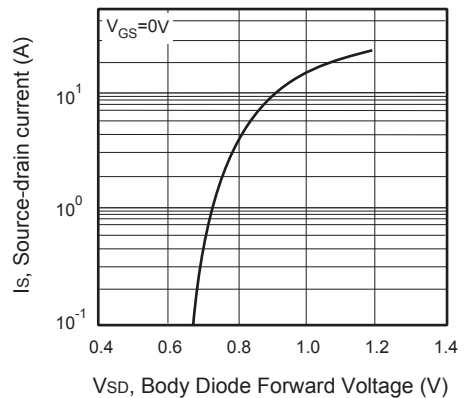


Figure 6. Body Diode Forward Voltage Variation with Source Current



CEM8958G

P-CHANNEL

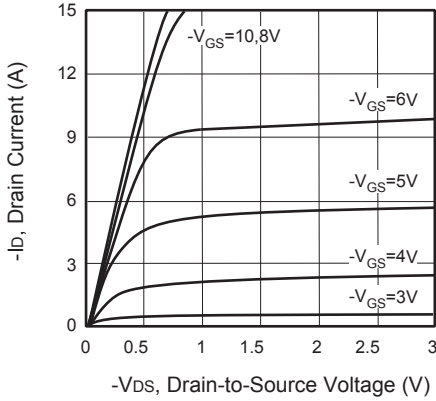


Figure 7. Output Characteristics

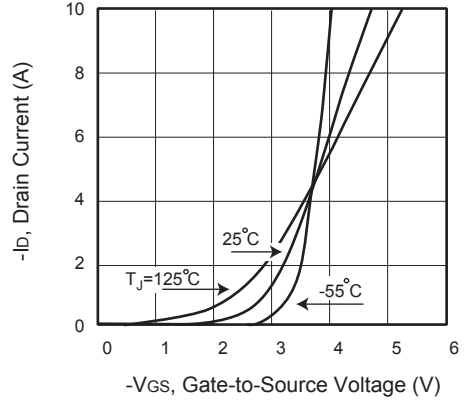


Figure 8. Transfer Characteristics

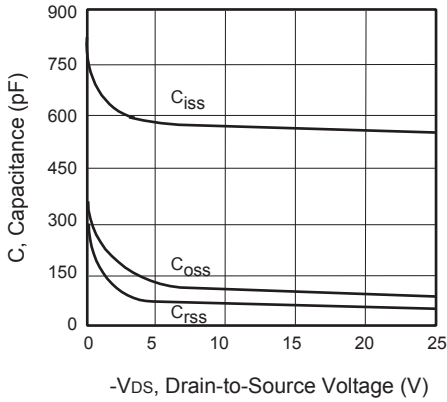


Figure 3. Capacitance

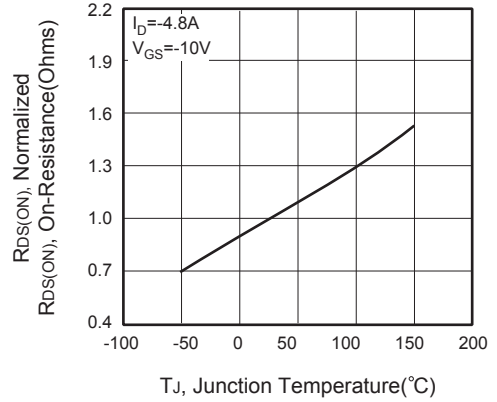


Figure 4. On-Resistance Variation with Temperature

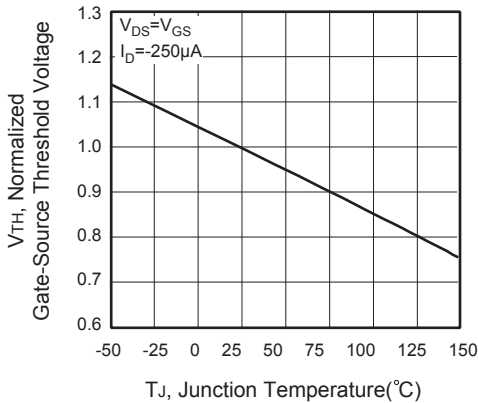


Figure 5. Gate Threshold Variation with Temperature

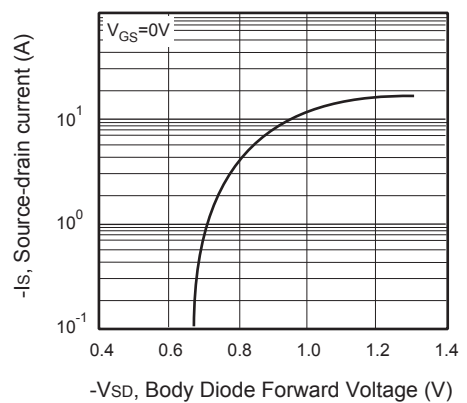


Figure 6. Body Diode Forward Voltage Variation with Source Current



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N-CHANNEL

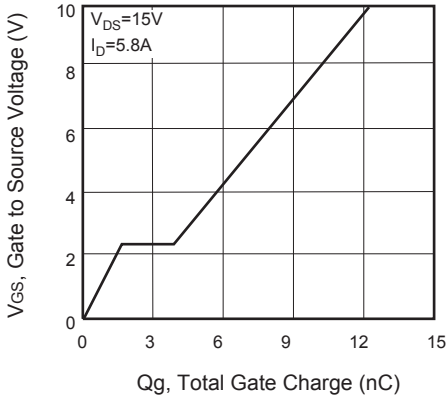


Figure 13. Gate Charge

P-CHANNEL

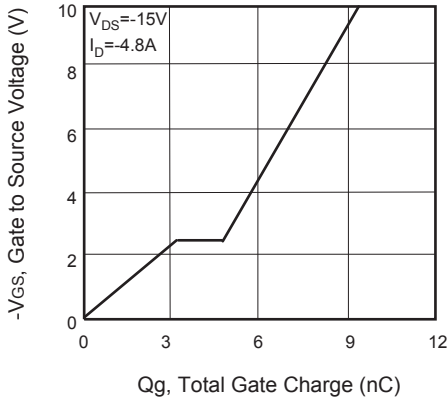


Figure 15. Gate Charge

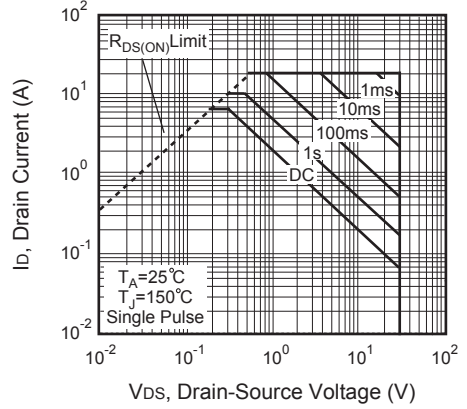


Figure 14. Maximum Safe Operating Area

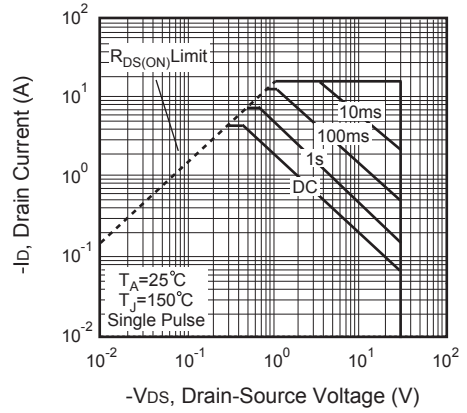


Figure 16. Maximum Safe Operating Area

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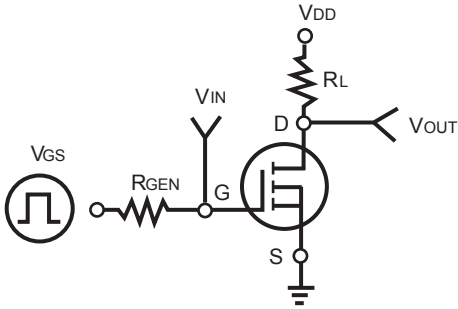


Figure 17. Switching Test Circuit

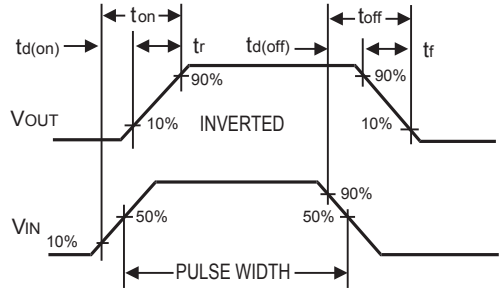


Figure 18. Switching Waveforms

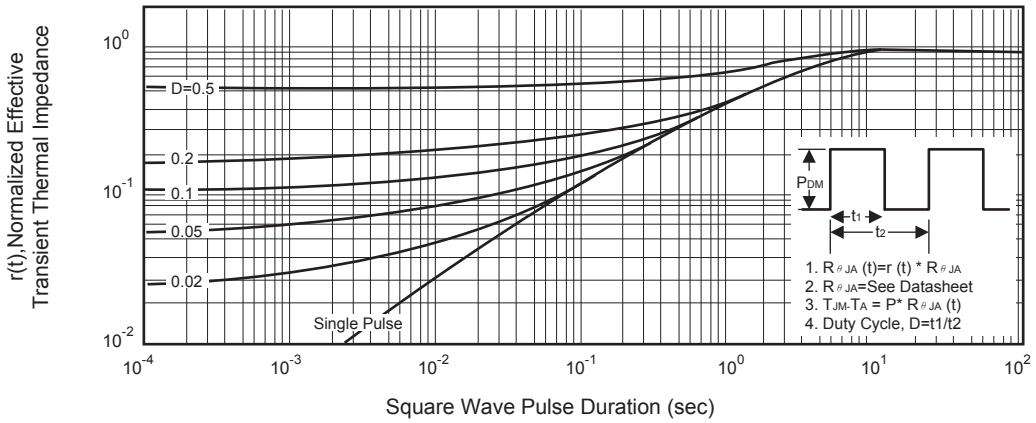


Figure 19. Normalized Thermal Transient Impedance Curve