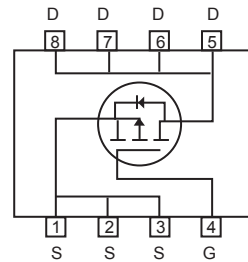


P-Channel Enhancement Mode Field Effect Transistor

FEATURES

- -20V, -7.7A, $R_{DS(ON)} = 25m\Omega$ @ $V_{GS} = -4.5V$.
 $R_{DS(ON)} = 35m\Omega$ @ $V_{GS} = -2.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead free product is acquired.
- Surface mount Package.



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	V
Drain Current-Continuous	I_D	-7.7	A
Drain Current-Pulsed ^a	I_{DM}	-30	A
Maximum Power Dissipation	P_D	2.5	W
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient ^b	$R_{\theta JA}$	50	$^\circ C/W$



CEM9424

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	
Off Characteristics							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-20			V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12V, V_{GS} = 0V$			-1	μA	
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 8V, V_{DS} = 0V$			100	nA	
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -8V, V_{DS} = 0V$			-100	nA	
On Characteristics ^c							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = -250\mu A$	-0.6		-1	V	
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5V, I_D = -7.7A$		20	25	$m\Omega$	
		$V_{GS} = -2.5V, I_D = -6.6A$		29	35	$m\Omega$	
Forward Transconductance	g_{FS}	$V_{DS} = -10V, I_D = -7.7A$		23		S	
Dynamic Characteristics ^d							
Input Capacitance	C_{iss}	$V_{DS} = -10V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$		2130		pF	
Output Capacitance	C_{oss}				760		pF
Reverse Transfer Capacitance	C_{rss}				127		pF
Switching Characteristics ^d							
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6V, I_D = -1A,$ $V_{GS} = -4.5V, R_{GEN} = 6\Omega$		60	80	ns	
Turn-On Rise Time	t_r			90	130	ns	
Turn-Off Delay Time	$t_{d(off)}$			310	400	ns	
Turn-Off Fall Time	t_f			190	250	ns	
Total Gate Charge	Q_g	$V_{DS} = -6V, I_D = -7.7A,$ $V_{GS} = -4.5V$		45	54	nC	
Gate-Source Charge	Q_{gs}			6		nC	
Gate-Drain Charge	Q_{gd}			14		nC	
Drain-Source Diode Characteristics and Maximum Ratings							
Drain-Source Diode Forward Current ^b	I_S				-2.3	A	
Drain-Source Diode Forward Voltage ^c	V_{SD}	$V_{GS} = 0V, I_S = -2.3A$			-1.2	V	
Notes : <input type="checkbox"/> a.Repetitive Rating : Pulse width limited by maximum junction temperature. <input type="checkbox"/> b.Surface Mounted on FR4 Board, $t \leq 10 \text{ sec.}$ <input type="checkbox"/> c.Pulse Test : Pulse Width $\leq 300\mu s,$ Duty Cycle $\leq 2\%.$ <input type="checkbox"/> d.Guaranteed by design, not subject to production testing. <input type="checkbox"/> <input type="checkbox"/>							



CEM9424

5

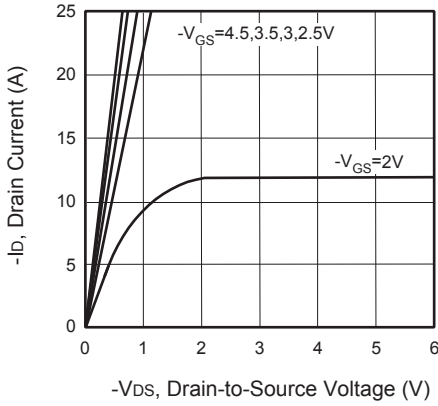


Figure 1. Output Characteristics

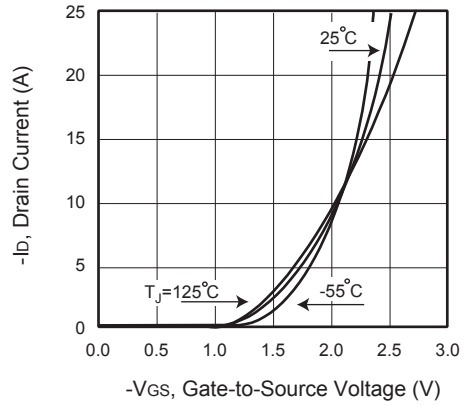


Figure 2. Transfer Characteristics

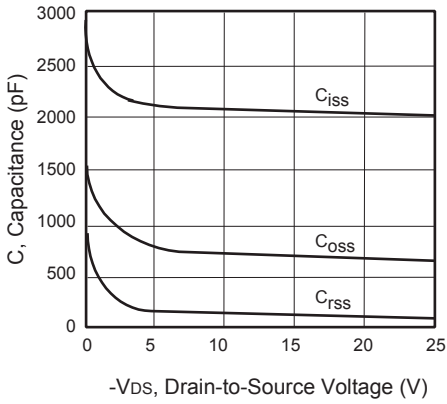


Figure 3. Capacitance

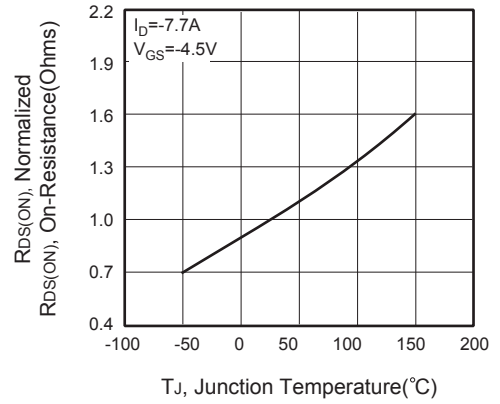


Figure 4. On-Resistance Variation with Temperature

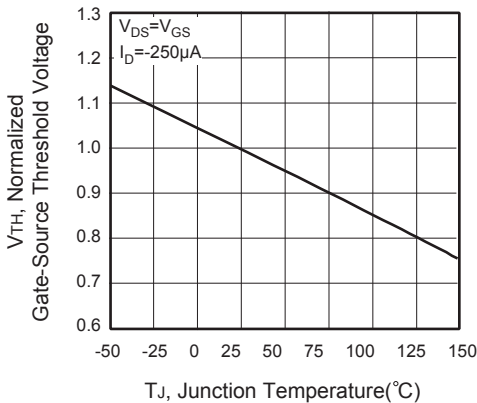


Figure 5. Gate Threshold Variation with Temperature

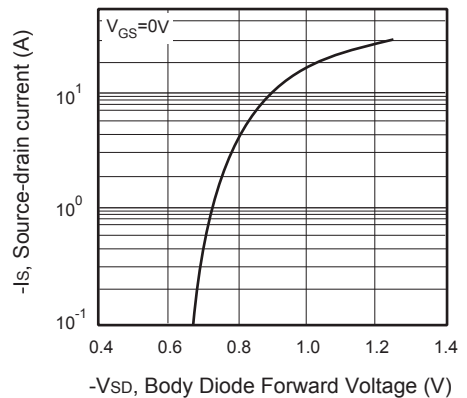


Figure 6. Body Diode Forward Voltage Variation with Source Current



CEM9424

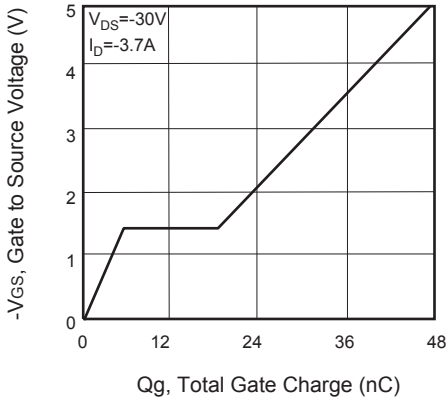


Figure 7. Gate Charge

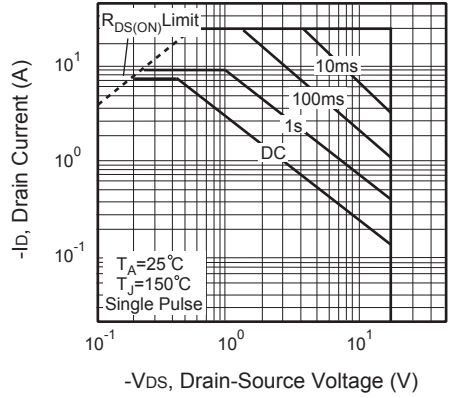


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

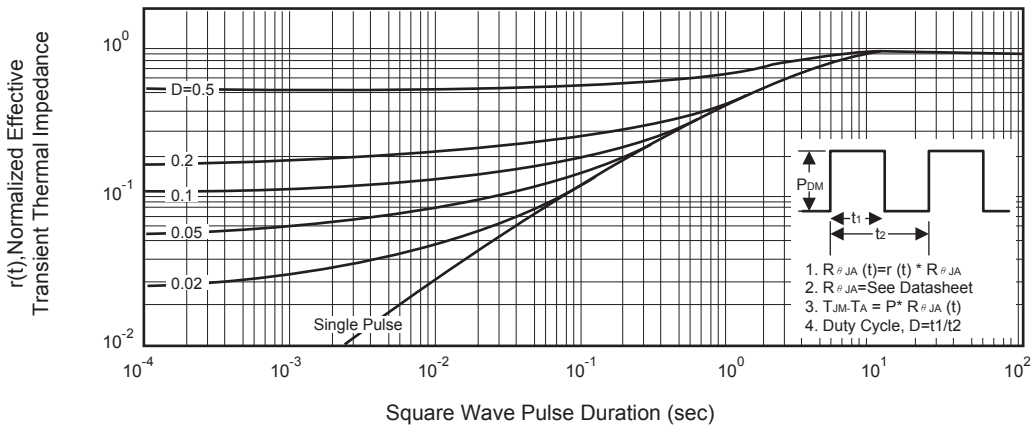


Figure 11. Normalized Thermal Transient Impedance Curve