Wide-Input Sensorless CC/CV Step-Down DC/DC Converter

FEATURES

- 42V Input Voltage Surge
- 40V Steady State Operation
- Up to 3A output current
- Output Voltage 2.5V to 10V
- Resistor Programmable
  - − Current Limit from 1.5A to 3A
  - − Cable Compensation from 0Ω to 0.4Ω
- ±7.5% CC Accuracy
  - − Compensation of Input /Output Voltage Change
  - − Temperature Compensation
- 2% Feedback Voltage Accuracy
- Up to 94% Efficiency
- 125kHz Switching Frequency Eases EMI Design
- Advanced Feature Set
  - − Integrated Soft Start
  - − Thermal Shutdown
  - − Protection Against Shorted ISET Pin
- Patented E-LTI technology improves load transient response.
- SOP-8EP Package

APPLICATIONS

- Car Charger/ Adaptor
- Rechargeable Portable Devices
- General-Purpose CC/CV Supply

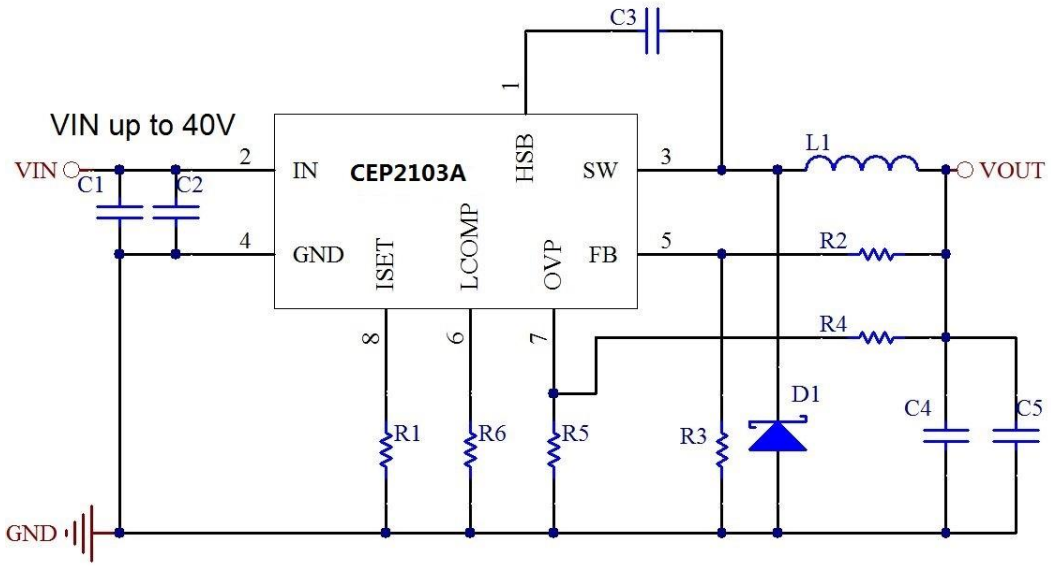
GENERAL DESCRIPTION

CEP2103A is a wide input voltage, high efficiency CC step-down DC/DC converter that operates in either CV (Constant Output Voltage) mode or CC (Constant Output Current) mode. CEP2103A provides up to 3A output current at 125kHz switching frequency.

CEP2103A provides OVP pin for output over voltage protection. If the voltage at this pin exceeds 1.25V then OVP circuit will turn off the PWM and cut off the output until the voltage of OVP pin lower than 1.25V.

Protection features include cycle-by-cycle current limit, thermal shutdown, and frequency foldback at short circuit. The devices are available in a SOP-8EP package and require very few external devices for operation.

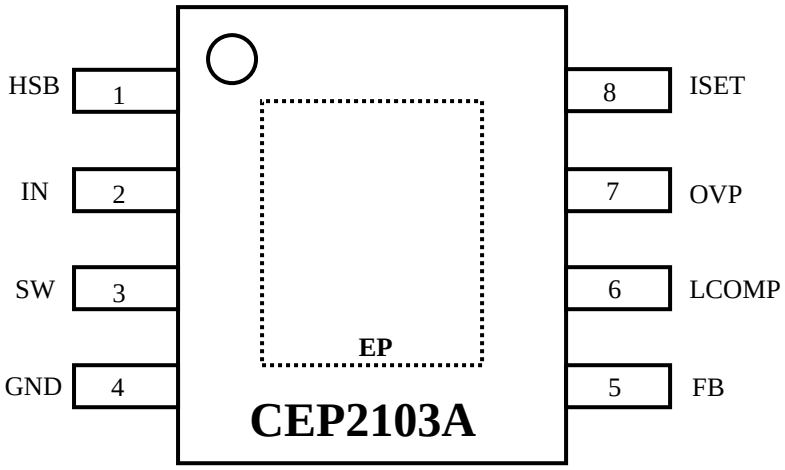
Typical Application Circuit for Car Charger



ORDERING INFORMATION

PART NUMBER	OPERATION TEMPERATURE RANGE	PACKAGE	PINS	PACKING	MOQ
CEP2103ASP8	-40°C to 85°C	SOP-8EP	8	TAPE & REEL	2.5K

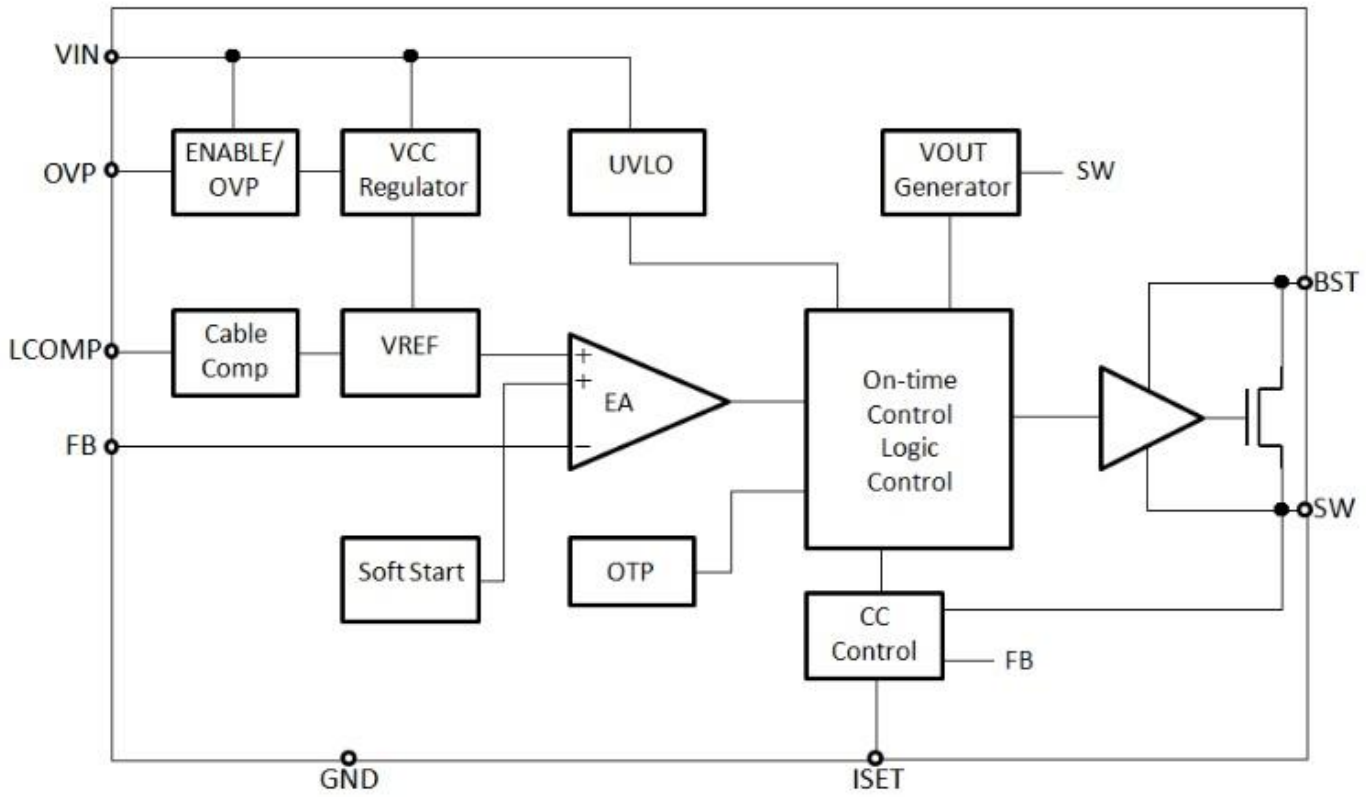
PIN CONFIGURATION



PIN DESCRIPTIONS

Pin No.	NAME	Description
1	HSB	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 22nF capacitor from HSB pin to SW pin.
2	IN	Power Supply Input. Bypass this pin with a 10μF ceramic capacitor to GND, placed as close to the IC as possible.
3	SW	Power Switching Output to External Inductor.
4	GND	Ground. Connect this pin to a large PCB copper area for best heat dissipation. Return FB, COMP, and ISET to this GND, and connect this GND to power GND at a single point for best noise immunity.
5	FB	Feedback Input. The voltage at this pin is regulated to 0.800V. Connect to the resistor divider between output and GND to set the output voltage.
6	LCOMP	Output cable resistance compensation.
7	OVP	OVP input. Overvoltage protection. The turnover voltage at this pin is 1.25V. The OVP circuit will turn off the PWM and cause the output floating until the voltage of OVP lower than 1.25V.
8	ISET	Output Current Setting Pin. Connect a resistor from ISET to GND to program the output current.
	Exposed Pad	Heat Dissipation Pad. Connect this exposed pad to large ground copper area with copper and vias.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
IN to GND	-0.3 to 42	V
SW to GND	-1 to VIN + 1	V
HSB to GND	VSW - 0.3 to VSW + 7	V
FB, EN, ISET, COMP to GND	-0.3 to + 6	V
Junction to Ambient Thermal Resistance	50	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Junction Temperature	-55 to 150	°C
Lead Temperature (Soldering 10 sec.)	300	°C

Note: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS
(VIN = 20V,TA = +25°C unless otherwise stated)

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Voltage		9		40	V
Input Voltage Surge		42			V
VIN UVLO Turn-On Voltage	Input Voltage Rising	8.3	8.6	8.9	V
VIN UVLO Hysteresis	Input Voltage Falling		0.6		V
Standby Supply Current	V_{FB} = 1V		0.9	1.4	mA
	V_{OUT} = 5V, No load		3		mA
Feedback Voltage		784	800	816	mV
Internal Soft-Start Time			900		uS
Switching Frequency	V_{FB} = 0.800V		125		KHz
Foldback Switching Frequency	V_{FB} = 0V		33		KHz
Minimum On-Time			250		nS
ISET Voltage			1		V
ISET to IOUT DC Room Temp Current Gain	IOUT / ISET, R_{ISET} = 19.6kΩ		26500		A/A
CC Controller DC Accuracy	R_{ISET} = 19.6kΩ, V_{OUT} = 3.5V Open-Loop DC Test	1295	1310	1325	mA
OVP Voltage Reference	OVP Pin Rising and Falling		1.25		V
High-Side Switch ON-Resistance			0.12		Ω
Thermal Shutdown Temperature	Temperature Rising		150		°C
Thermal Shutdown Temperature Hysteresis	Temperature Falling		50		°C

FUNCTIONAL DESCRIPTION

CV/CC Loop Regulation

As seen in Functional Block Diagram, the CEP2103A is a peak current mode pulse width modulation (PWM) converter with CC and CV control. The converter operates as follows:

A switching cycle starts when the rising edge of the Oscillator clock output causes the High-Side Power Switch to turn on and the Low-Side Power Switch to turn off. With the SW side of the inductor now connected to IN, the inductor current ramps up to store energy in the magnetic field. The inductor current level is measured by the Current Sense Amplifier and added to the Oscillator ramp signal. If the resulting summation is higher than the COMP voltage, the output of the PWM Comparator goes high. When this happens or when Oscillator clock output goes low, the High-Side Power Switch turns off.

At this point, the SW side of the inductor swings to a diode voltage below ground, causing the inductor current to decrease and magnetic energy to be transferred to output. This state continues until the cycle starts again. The High-Side Power Switch is driven by logic using HSB as the positive rail. This pin is charged to VSW + 5V when the Low-Side Power Switch turns on. The COMP voltage is the integration of the error between FB input and the internal 0.800V reference. If FB is lower than the reference voltage, COMP tends to go higher to increase current to the output. Output current will increase until it reaches the CC limit set by the ISET resistor. At this point, the device will transition from regulating output voltage to regulating output current, and the output voltage will drop with increasing load.

The Oscillator normally switches at 125kHz. However, if FB voltage is less than 0.6V, then the switching frequency decreases until it reaches a typical value of 30kHz at VFB = 0.15V.

OVP Pin

CEP2103A provides OVP pin for output over voltage protection. If the voltage at this pin exceeds 1.25V then OVP circuit will turn off the PWM and cut off the output until the voltage of OVP pin lower than 1.25V.

When the OVP effective that the output is floating.

Thermal Shutdown

The CEP2103A disables switching when its junction temperature exceeds 150°C and resumes when the temperature has dropped by 20°C.

APPLICATIONS INFORMATION

Output Voltage Setting

Figure 1:
Output Voltage Setting

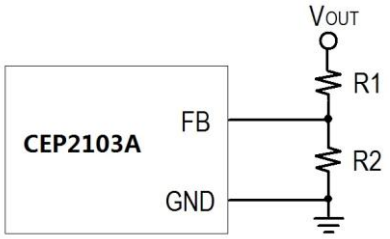


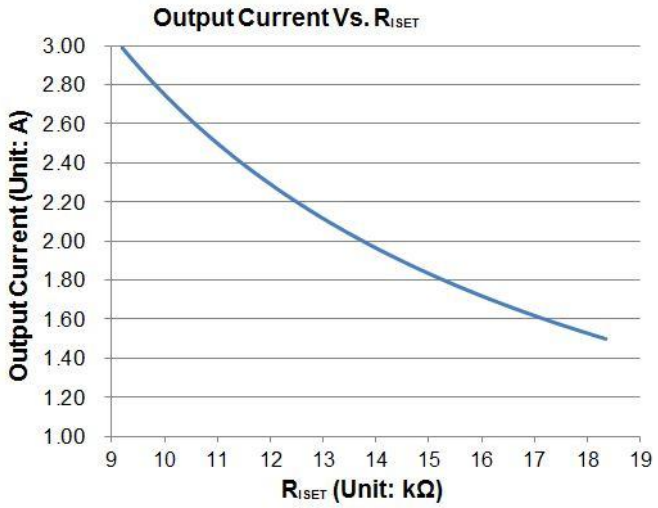
Figure 1 shows the connections for setting the output voltage. Select the proper ratio of the two feedback resistors R1 and R2 based on the output voltage. Typically, use R2 ≈10kΩ and determine R1 from the following equation:

$$R1 = R2\left(\frac{V_{OUT}}{0.800V} - 1\right) \qquad (1)$$

CC Current Setting

CEP2103A constant current value is set by a resistor connected between the ISET pin and GND. The CC output current is linearly proportional to the current flowing out of the ISET pin. The voltage at ISET is roughly 1V and the current gain from ISET to output is roughly 27500 (27.5mA/1μA). To determine the proper resistor for a desired current, please refer to Figure 2 below.

Figure 2:
Curve for Programming Output CC Current



Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value:
Higher inductance reduces the peak-to-peak ripple current. The tradeoff for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general, select an inductance value L based on ripple current requirement:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{LOADMAX} \times K_{RIPPLE}} \qquad (2)$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_{SW} is the switching frequency, $I_{LOADMAX}$ is the maximum load current, and K_{RIPPLE} is the ripple factor. Typically, choose K_{RIPPLE} = 30% to correspond to the peak-to-peak ripple current being 30% of the maximum load current.
With a selected inductor value the peak-to-peak inductor current is estimated as:

$$I_{LPK-PK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{L \times V_{IN} \times f_{SW}} \qquad (3)$$

The peak inductor current is estimated as:

$$I_{LPK} = I_{LOADMAX} + \frac{1}{2} I_{LPK-PK} \qquad (4)$$

The selected inductor should not saturate at I_{LPK}. The maximum output current is calculated as:

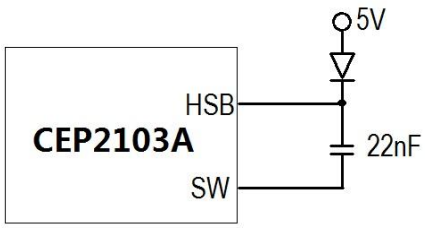
$$I_{OUTMAX} = I_{LIM} - \frac{1}{2} I_{LPK-PK} \quad (5)$$

I_{LIM} is the internal current limit, which is typically 4.2A.

External High Voltage Bias Diode

It is recommended that an external High Voltage Bias diode be added when the system has a 5V fixed input or the power supply generates a 5V output. This helps improve the efficiency of the regulator. The High Voltage Bias diode can be a low cost one such as IN4148.

Figure 4:
External High Voltage Bias Diode



This diode is also recommended for high duty cycle operation and high output voltage applications.

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.

The input capacitance needs to be higher than 10µF. The best choice is the ceramic type, however, low ESR tantalum or electrolytic types may also be used provided that the RMS ripple current rating is higher than 50% of the output current. The input capacitor should be placed close to the IN and G pins of the IC, with the shortest traces possible. In the case of tantalum or electrolytic types, they can be further away if a small parallel 0.1µF ceramic capacitor is placed right next to the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple. The output ripple voltage is:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{V_{IN}}{28 \times f_{SW}^2 L C_{OUT}} \quad (6)$$

Where I_{OUTMAX} is the maximum output current, K_{RIPPLE} is the ripple factor, R_{ESR} is the ESR of the output capacitor, f_{SW} is the switching frequency, L is the inductor value, and C_{OUT} is the output capacitance. In the case of ceramic output capacitors, R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic type. In the case of tantalum or electrolytic capacitors, the ripple is dominated by R_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.

For ceramic output capacitor, typically choose a capacitance of about 220µF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

Rectifier Diode

Use a Schottky diode as the rectifier to conduct current when the High-Side Power Switch is off. The Schottky diode must have current rating higher than the maximum output current and a reverse voltage rating higher than the maximum input voltage.

Output Cable Resistance Compensation

To compensate for resistive voltage drop across the charger's output cable, the CEP2103A integrates a simple, user-programmable cable voltage drop compensation using the impedance at the LCOMP pin. Use the curve in Figure 5 or list in Table1 to choose the proper resistance values for cable compensation.

Figure 5: Cable Compensation

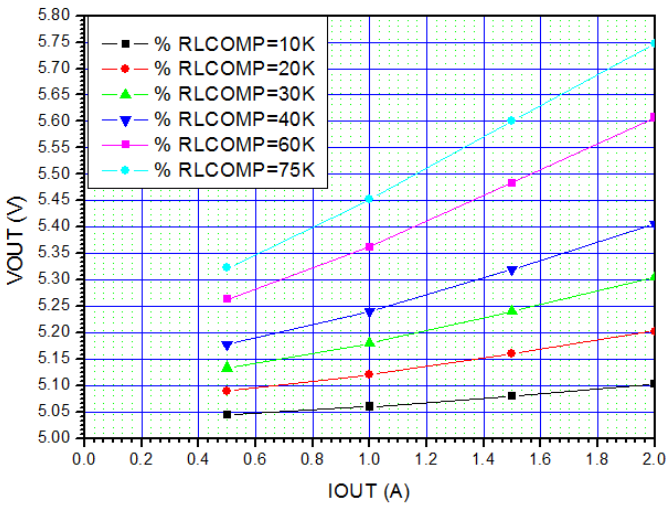


Table1: Recommend resistance values for cable compensation.

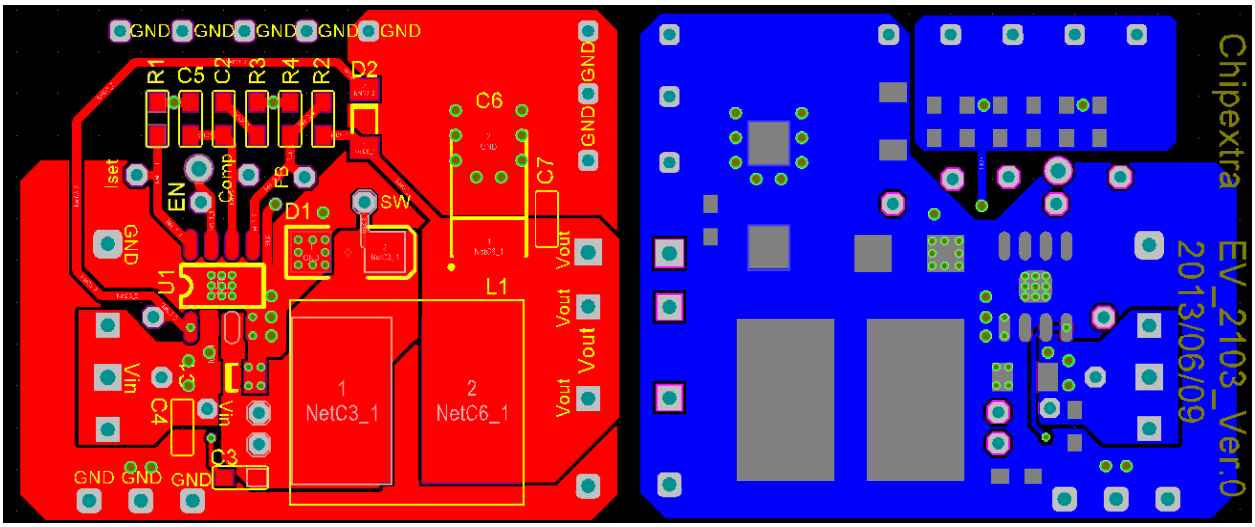
R_{LCOMP}(KΩ)	Equivalent R (Ω)
10	0.04
20	0.08
30	0.12
40	0.16
60	0.24
75	0.30

PC Board Layout Guidance

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC.

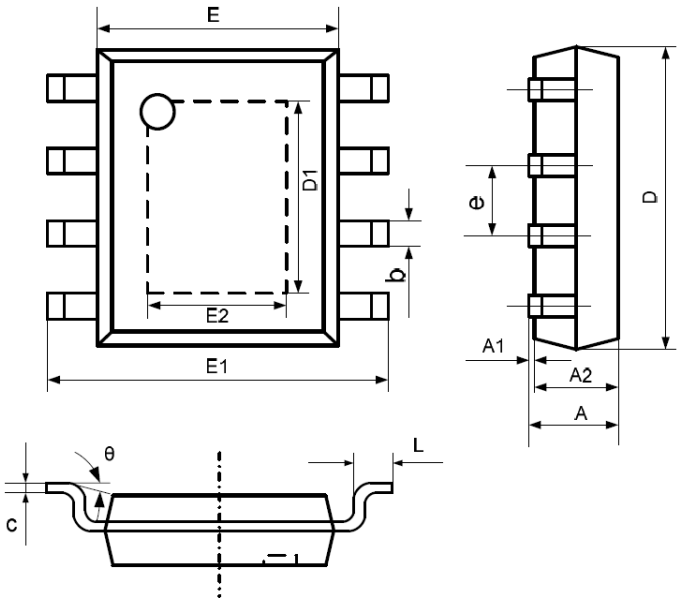
1) Arrange the power components to reduce the AC loop size consisting of CIN, IN pin, SW pin and the schottky diode.
2) Place input decoupling ceramic capacitor CIN as close to IN pin as possible. CIN is connected power GND with vias or short and wide path.
3) Return FB, COMP and ISET to signal GND pin,and connect the signal GND to power GND at a single point for best noise immunity. Connect exposed pad to power ground copper area with copper and vias.
4) Use copper plane for power GND for best heat dissipation and noise immunity.
5) Place feedback resistor close to FB pin.
6) Use short trace connecting HSB-CHSB-SW loop Figure 6 shows an example of PCB layout.

Figure 6: PCB Layout



PACKAGE OUTLINE

SOP-8EP PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.700	0.053	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°