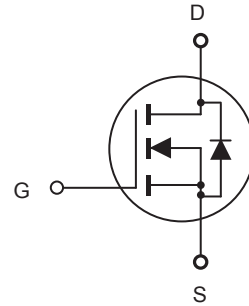


## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- 100V, 50A,  $R_{DS(ON)} = 30m\Omega$  @  $V_{GS} = 10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- TO-220 & TO-263 package.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Drain Current-Continuous	$I_D$	50	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	200	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above $25^\circ\text{C}$	$P_D$	136	W
		0.91	W/ $^\circ\text{C}$
Single Pulsed Avalanche Energy <sup>d</sup>	$E_{AS}$	397	mJ
Single Pulsed Avalanche Current <sup>d</sup>	$I_{AS}$	43.5	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

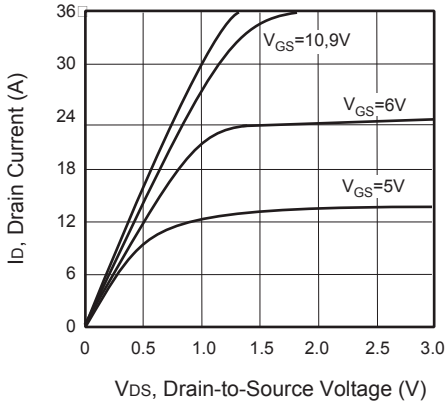
Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.1	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$



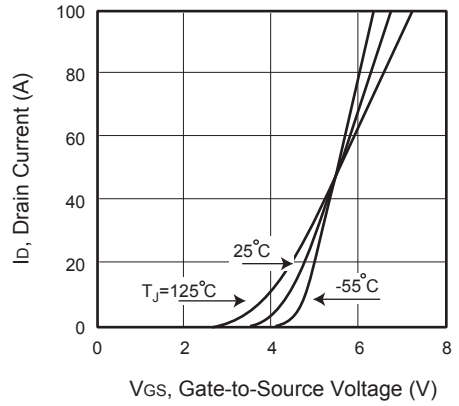
# CEP50N10/CEB50N10

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

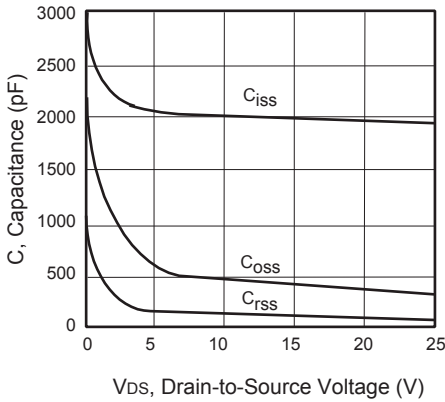
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 25V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -25V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 25A$		25	30	m $\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1955		pF
Output Capacitance	$C_{oss}$			300		pF
Reverse Transfer Capacitance	$C_{rss}$			35		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50V, I_D = 5A, V_{GS} = 10V, R_{GEN} = 25\Omega$		27	54	ns
Turn-On Rise Time	$t_r$			19	38	ns
Turn-Off Delay Time	$t_{d(off)}$			185	370	ns
Turn-Off Fall Time	$t_f$			35	70	ns
Total Gate Charge	$Q_g$	$V_{DS} = 80V, I_D = 37A, V_{GS} = 10V$		49	65	nC
Gate-Source Charge	$Q_{gs}$			10		nC
Gate-Drain Charge	$Q_{gd}$			16		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				50	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 40A$			1.5	V
<b>Notes :</b> a. Repetitive Rating : Pulse width limited by maximum junction temperature. b. Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . c. Guaranteed by design, not subject to production testing. d. L = 0.42mH, $I_{AS} = 43.5A, V_{DD} = 25V, R_G = 25\Omega$ , Starting $T_J = 25\text{ C}$						



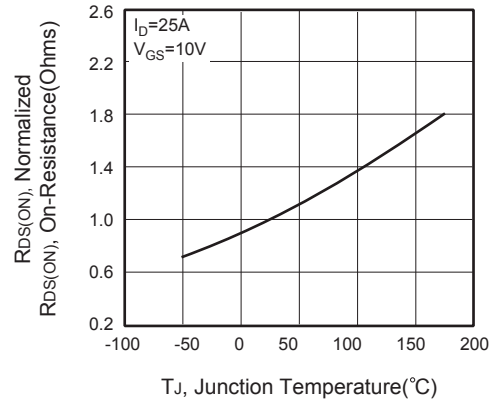
**Figure 1. Output Characteristics**



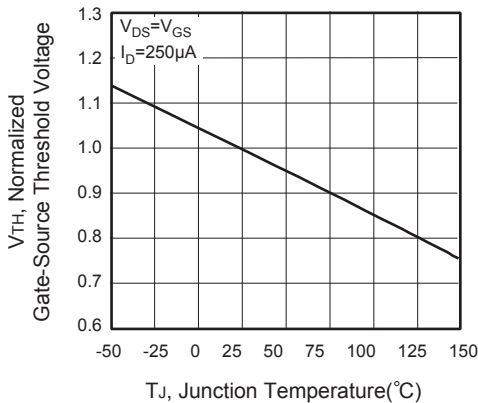
**Figure 2. Transfer Characteristics**



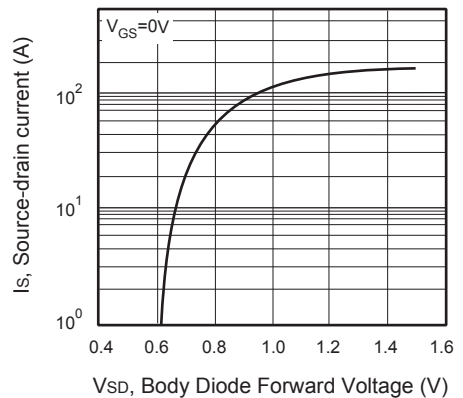
**Figure 3. Capacitance**



**Figure 4. On-Resistance Variation with Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Body Diode Forward Voltage Variation with Source Current**

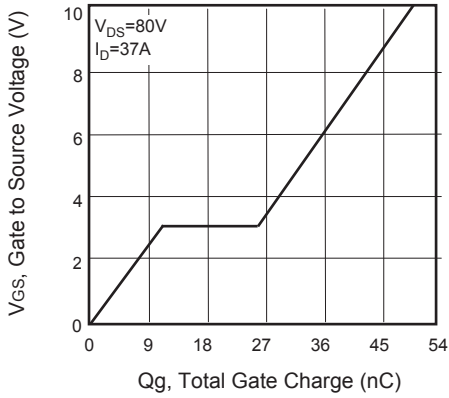


Figure 7. Gate Charge

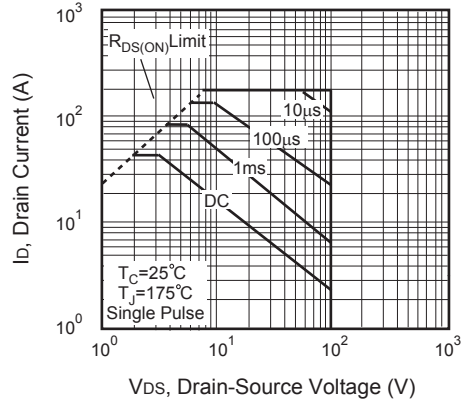


Figure 8. Maximum Safe Operating Area

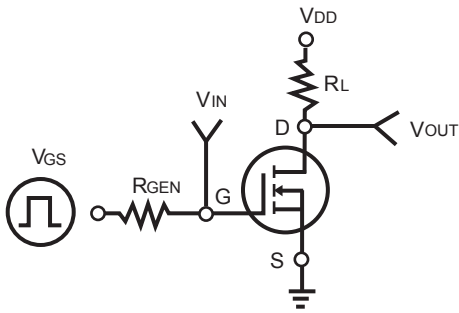


Figure 9. Switching Test Circuit

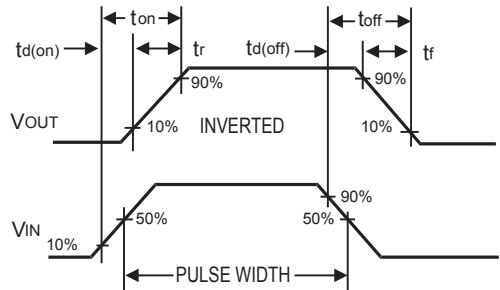


Figure 10. Switching Waveforms

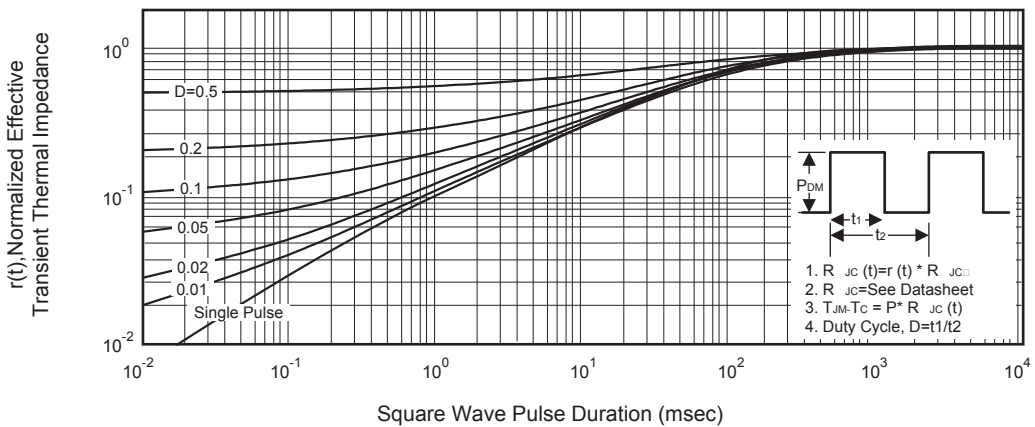


Figure 11. Normalized Thermal Transient Impedance Curve