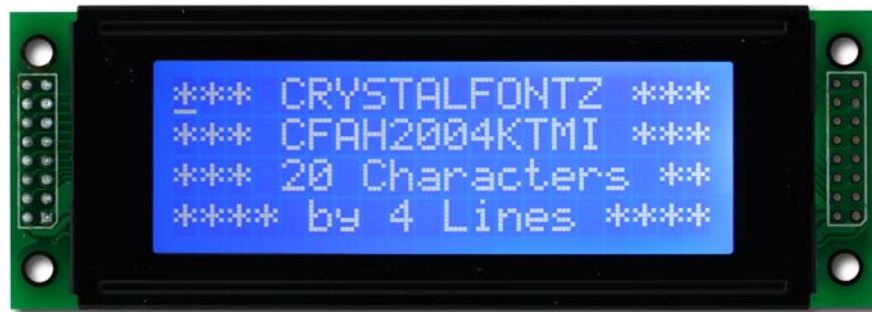




CrystalFontz America, Incorporated

CHARACTER LCD MODULE SPECIFICATIONS



CrystalFontz Model Number	CFAH2004K-TMI-JP
Hardware Version	Revision 0.0
Data Sheet Version	Revision 1.0, August 2010
Product Pages	www.crystalfontz.com/product/CFAH2004KTMIJP.html

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REVISION HISTORY

HARDWARE
Current hardware version: v0.0

DATA SHEET	
2010/08/23	<p>Current Data Sheet version: v1.0 Changes since last Data Sheet (v0.0a):</p> <ul style="list-style-type: none"> ● Wherever listed, changed controller from “Sunplus SPLC780C” to “Sunplus SPLC780D1”. Controller is still equivalent to a standard Hitachi HD44780. See APPENDIX C: SUNPLUS SPLC780D1 CONTROLLER DATA SHEET (Pg. 31). ● Wherever needed, added module nominal depth of “14.4 millimeters”. In previous Data Sheet, only maximum of “15.00 millimeters” was listed. Module depth has not changed. ● Wherever appropriate, added note “This module has two sets of pins that are identical. Either set of pins may be used.” ● In MAIN FEATURES (Pg. 6), <ul style="list-style-type: none"> - Corrected misspelling by changing “HD47780” to “HD44780” equivalent controller. - Expanded information for clarity. ● Added photos with pins labeled. See Quick Reference for Pin Functions (Front & Back Photos) (Pg. 13). ● Please read revised and expanded MODULE RELIABILITY AND LONGEVITY (Pg. 23) section. Changes include reduced power-on hours at 90% for white backlight from “10,000” hours to “5,000”. This reduction more accurately reflects typical backlight use. LEDs have not changed. ● Added section APPENDIX B: APPLICATION NOTE FOR 3.3V OPERATION (Pg. 29). ● Additional minor changes to improve drawings, tables, and text.
2006/01/01	<p>Data Sheet version: 0.0a Changes since last Data Sheet (v0.0):</p> <ul style="list-style-type: none"> ● Added “Luminous Intensity” specification (Pg. 12). ● Minor formatting and rewording changes to improve readability.
2005/12/01	New Data Sheet.



The Fine Print

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CONTENTS

MAIN FEATURES	6
Module Classification Information	6
Ordering Information	7
MECHANICAL SPECIFICATIONS	7
Physical Characteristics	7
Module Outline Drawing	8
ELECTRICAL SPECIFICATIONS	9
System Block Diagram	9
Temperature Range	10
Driving Method	10
Absolute Maximum Ratings	10
LCD Supply Voltage	11
Current Consumption	11
Details of Interface Pin Functions	12
Quick Reference for Pin Functions (Front & Back Photos)	13
Typical V_O Connections for Display Contrast	15
ESD (Electro-Static Discharge) Specifications	15
OPTICAL SPECIFICATIONS	16
Optical Characteristics	16
Optical Definitions	16
LED Backlight Characteristics	19
LCD CONTROLLER INTERFACE	21
Display Position DDRAM Address	21
Character Generator ROM (CGROM)	22
MODULE RELIABILITY AND LONGEVITY	23
Module Reliability	23
Module Longevity (EOL / Replacement Policy)	23
CARE AND HANDLING PRECAUTIONS	24
APPENDIX A: QUALITY ASSURANCE STANDARDS	26
APPENDIX B: APPLICATION NOTE FOR 3.3V OPERATION	29
APPENDIX C: SUNPLUS SPLC780D1 CONTROLLER DATA SHEET	31



LIST OF FIGURES

Figure 1. Module Outline Drawing	8
Figure 2. System Block Diagram	9
Figure 3. Back Left View of Pins (Labeled)	13
Figure 4. Back Right View of Pins (Labeled)	13
Figure 5. Front Left View of Pins (Labeled)	14
Figure 6. Front Right View of Pins (Labeled)	14
Figure 7. Typical V_O Connections	15
Figure 8. Definition of Operation Voltage (V_{OP}) (Negative)	17
Figure 9. Definition of Response Time (T_r , T_f) (Negative)	17
Figure 10. Definition of Horizontal and Vertical Viewing Angles ($CR > 2$)	18
Figure 11. Definition of 6:00 O’Clock and 12:00 O’Clock Viewing Angles	18
Figure 12. Typical LED Backlight Connections for “Always On”	19
Figure 13. Example of LED Backlight Connections for PWM Dimming	20
Figure 14. Character Generator ROM (CGROM)	22



MAIN FEATURES

- 20 characters by 4 lines module consists of an LCD panel, a PCB (Printed Circuit Board) with a built-in Sunplus SPLC780D1 controller, and an LED backlight.
- Module Dimensions.
 - Active Area is 70.4 (W) x 20.8 (H) millimeters.
 - Overall dimension is 116.0 (W) x 40.0 (H) x 15.0 maximum (D) millimeter package (4.57" (W) x 1.57" (H) x 0.59" (D)).
- This module has two sets of pins that are identical. You can use either set of pins.
- 4-bit or 8-bit parallel interface.
- Standard Hitachi HD44780 equivalent controller. See [APPENDIX C: SUNPLUS SPLC780D1 CONTROLLER DATA SHEET \(Pg. 31\)](#).
- White edge LED backlight with STN, negative, blue, transmissive mode LCD (displays light characters on a blue background).
- Wide temperature operation: -20°C to +70°C.
- RoHS compliant.

MODULE CLASSIFICATION INFORMATION



CFA H 20 04 K - T M I - J P *
1 2 3 4 5 6 7 8 9 10 11

1	Brand	CrystalFontz America, Inc.
2	Display Type	H – Character
3	Number of Characters (Width)	20 Characters
4	Number of Lines (Height)	4 Lines
5	Model Identifier	K
6	Backlight Type & Color	T – LED, white
7	Fluid Type, Image (Positive or Negative), & LCD Glass Color	T – STN, negative, blue
8	Polarizer Film Type, Wide (WT) Temperature Range, & Viewing Angle (O'clock)	I – Transmissive, WT, 6:00 ¹
9	Character Set (CGROM)	J – English and Japanese fonts
10	Controller	P – Sunplus SPLC780D1
11	Special Code	* – May have additional manufacturer's codes at this location.

¹Note: For more information on Viewing Angle, see [Definition of 6 O'Clock and 12:00 O'Clock Viewing Angles \(Pg. 18\)](#).



ORDERING INFORMATION

PART NUMBER	FLUID	LCD GLASS COLOR	IMAGE	POLARIZER FILM	BACKLIGHT COLOR/TYPE
CFAH2004K-TMI-JP	STN	blue	negative	transmissive	white LED 
<i>Additional variants (same form factor, different LCD mode or backlight):</i>					
CFAH2004K-YYH-JP	STN	yellow-green	positive	transflective	yellow-green LED 

MECHANICAL SPECIFICATIONS

PHYSICAL CHARACTERISTICS

ITEM	SIZE
Number of Characters and Lines	20 Characters x 4 Lines
Weight	68 grams (typical)

Pixel Detail (millimeters)		
	Width	Height
Pixel Size	0.55	0.55
Pixel Pitch	0.60	0.60

Character Detail (millimeters)		
	Width	Height
Character Size	2.95	4.75
Character Pitch	3.55	5.35

Viewing Area		
	Width	Height
Millimeters	76.0	25.2
Inches	2.99"	0.99"

Active Area		
	Width	Height
Millimeters	70.4	20.8
Inches	2.77"	0.82"

Module Overall		
	Width	Height
Millimeters	116.0	40.0
Inches	4.57"	1.57"

Module Depth		
	Maximum	Nominal
Millimeters	15.0	14.4
Inches	0.59"	0.57"



MODULE OUTLINE DRAWING

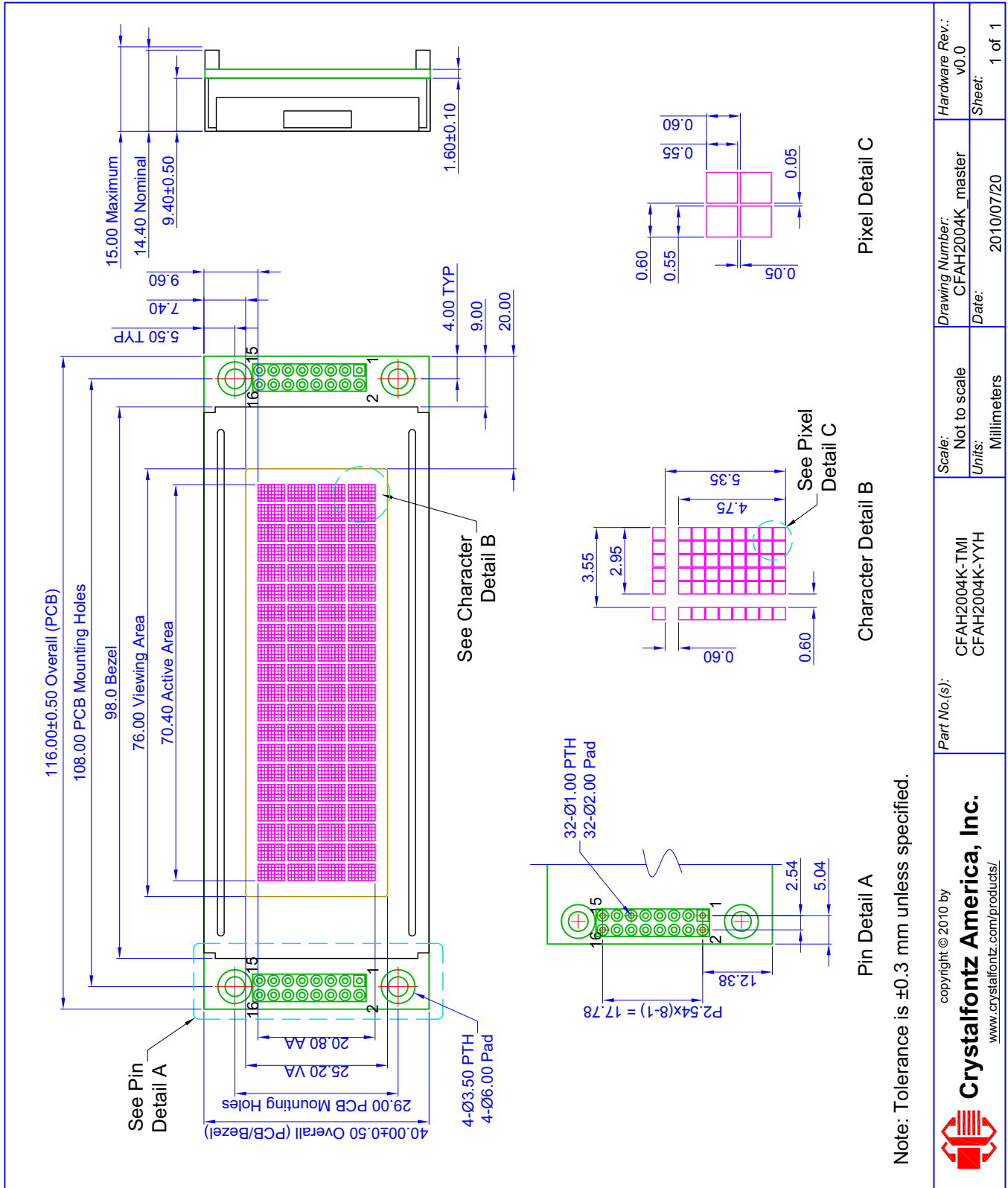


Figure 1. Module Outline Drawing

<p>copyright © 2010 by CrystalFontz America, Inc. www.crystalfontz.com/products/</p>	Part No.(s): CFAH2004K-TMI CFAH2004K-YYH	Scale: Not to scale Units: Millimeters	Drawing Number: CFAH2004K_master	Hardware Rev.: v0.0
	Date: 2010/07/20	Sheet: 1 of 1		



ELECTRICAL SPECIFICATIONS

SYSTEM BLOCK DIAGRAM

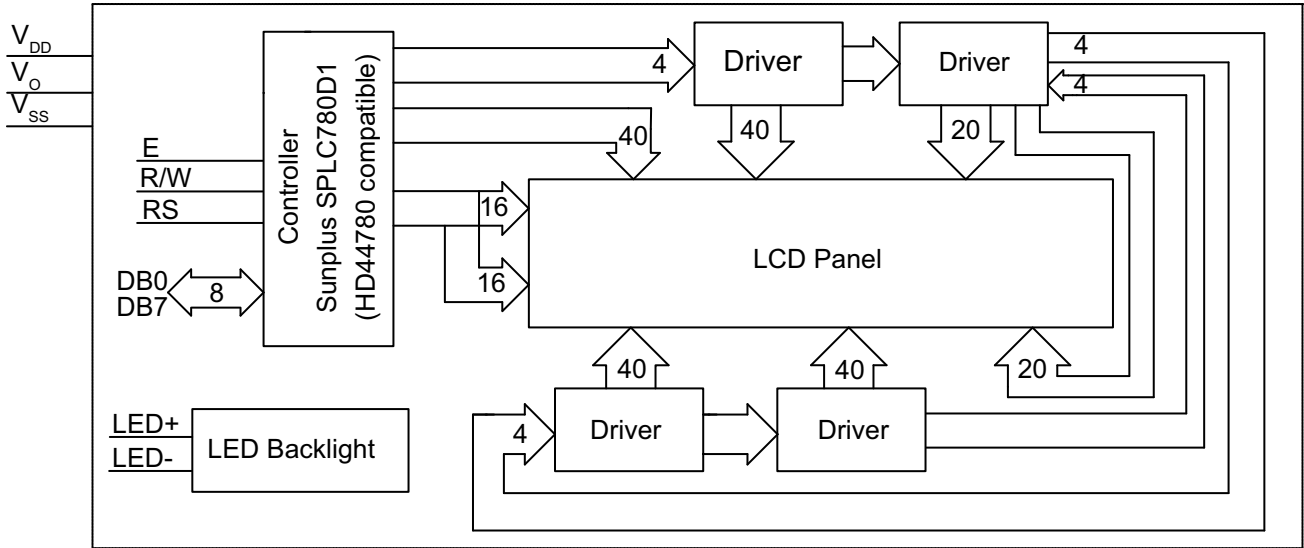


Figure 2. System Block Diagram



TEMPERATURE RANGE

	SYMBOL	MINIMUM	MAXIMUM
ABSOLUTE MAXIMUM RATINGS			
Operating Temperature*	T _{OP}	-20°C	+70°C
Storage Temperature*	T _{ST}	-30°C	+80°C
Humidity	RH	0%	90%
<i>*Note: Prolonged exposure at temperatures outside of this range may cause permanent damage to the module.</i>			

DRIVING METHOD

DRIVING METHOD	SPECIFICATION
Duty	1/16
Bias	1/5

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	ABSOLUTE MAXIMUM RATINGS
Operating Voltage	V _{DD}	-0.3v to +7.0v
Driver Supply Voltage	V _{LCD}	V _{LCD} = V _{DD} -12v to V _{LCD} = V _{DD} + 0.3v or V _O = -7v to V _O = +5.3v (for V _{DD} = +5v)
Input Voltage Range	V _{IN}	-0.3v to V _{DD} + 0.3v



LCD SUPPLY VOLTAGE

LCD SUPPLY VOLTAGE		MINIMUM	TYPICAL	MAXIMUM
Supply Voltage for Driving LCD ($V_{DD} - V_O$)	$T_A = 0^\circ\text{C}$			+4.8v
	$T_A = +25^\circ\text{C}$		+4.5v	
	$T_A = +50^\circ\text{C}$	+4.2v		

CURRENT CONSUMPTION

CURRENT CONSUMPTION		MINIMUM	TYPICAL	MAXIMUM
Supply Current (I_{DD}) $V_{DD} = +5\text{v}$			+1.2 mA	



DETAILS OF INTERFACE PIN FUNCTIONS

Note: This module has two sets of pins that are identical. You can use either set of pins.

PIN	SIGNAL	LEVEL	DIRECTION	DESCRIPTION
1	V _{SS}	0v		Ground. Must be connected to an external ground
2	V _{DD}	+5.0v		Supply voltage for logic. Must be connected to an external source. <i>Do NOT mix supply voltage and logic voltages.</i>
3	V _O	variable		Supply voltage for driving LCD is V _O = +1v typical at V _{DD} = +5v which gives a V _{LCD} = (V _{DD} - V _O) = +4v
4	RS	H/L	I	Register selection input. <i>High:</i> Data register (for read and write) <i>Low:</i> Instruction code (for write)
5	R \bar{W}	H/L	I	Host interface input. <i>High:</i> Read (Host←Module) <i>Low:</i> Write (Host→Module)
6	E	H,H→L	I	Read/write enable signal. <i>High:</i> Read data is enabled by a high level. <i>High→Low:</i> Write data is latched on the falling edge.
7	DB0	H/L	I/O	Bidirectional databus connects to 4-bit or 8-bit standard host databus.
8	DB1	H/L	I/O	
9	DB2	H/L	I/O	
10	DB3	H/L	I/O	
11	DB4	H/L	I/O	
12	DB5	H/L	I/O	
13	DB6	H/L	I/O	
14	DB7	H/L	I/O	
15	A (LED +)			Supply voltage for LED. "A" (anode) or "+" of LED backlight
16	K (LED -)			Supply voltage for LED. "K" (cathode or kathode for German and original Greek spelling) or "-" of LED backlight

For backlight connections, please refer to [LED Backlight Characteristics \(Pg. 19\)](#).



QUICK REFERENCE FOR PIN FUNCTIONS (FRONT & BACK PHOTOS)

Note: This module has two sets of pins that are identical. You can use either set of pins.

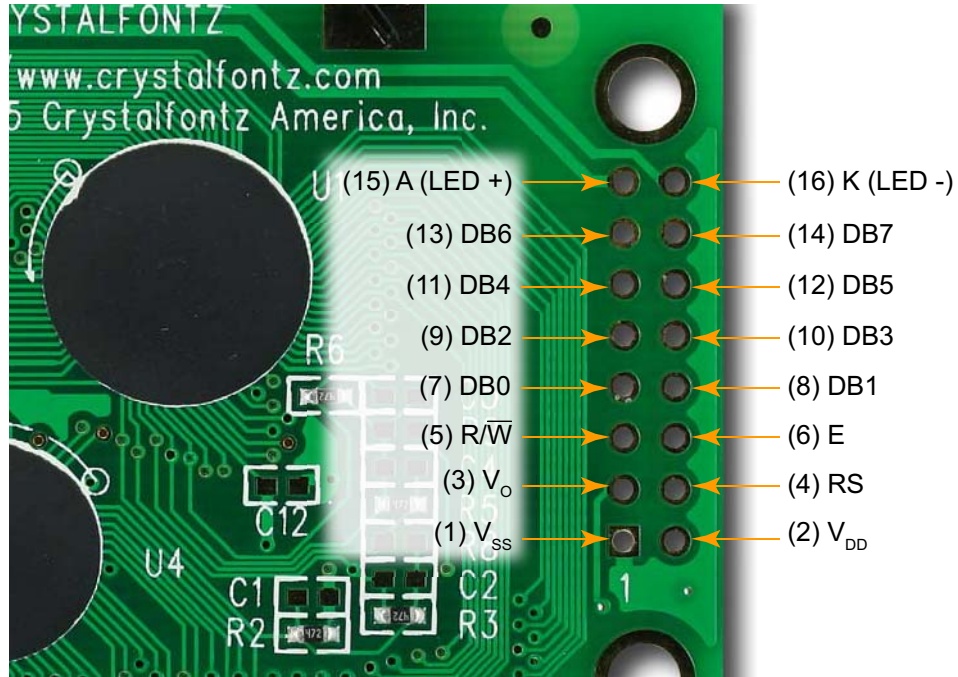


Figure 3. Back Left View of Pins (Labeled)

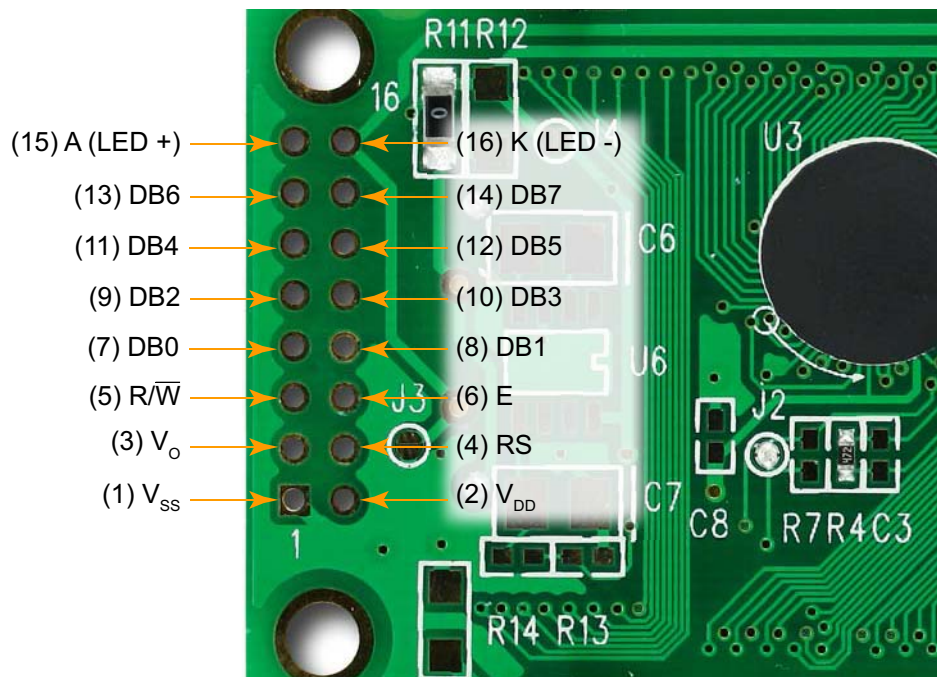


Figure 4. Back Right View of Pins (Labeled)

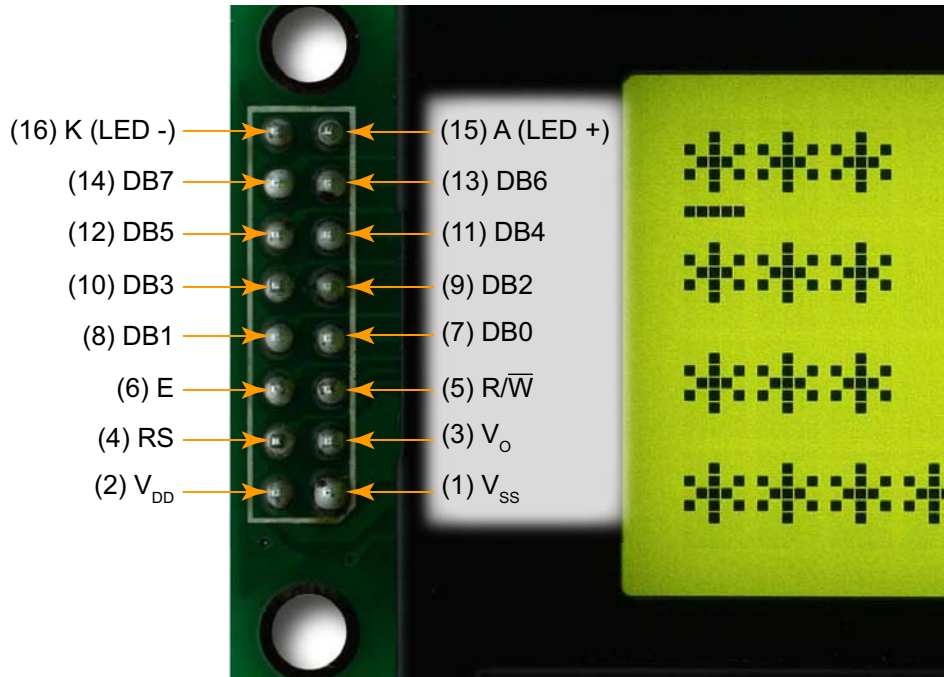


Figure 5. Front Left View of Pins (Labeled)

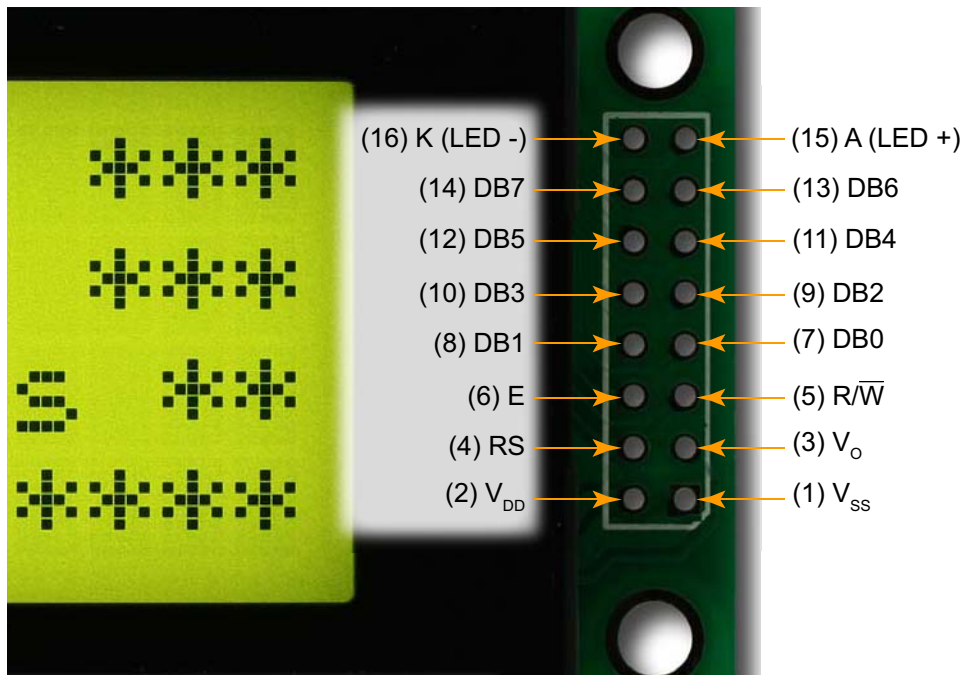


Figure 6. Front Right View of Pins (Labeled)



TYPICAL V_O CONNECTIONS FOR DISPLAY CONTRAST

Adjust V_O to +1v ($V_{LCD} = +4v$) as an initial setting. When the module is operational, readjust V_O for optimal display appearance.

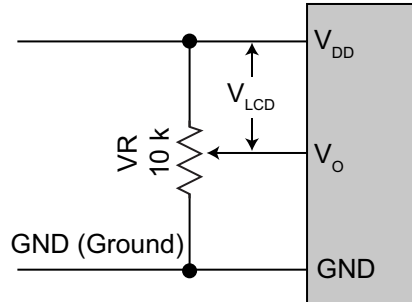


Figure 7. Typical V_O Connections

We recommend allowing field adjustment of V_O for all designs. The optimal value for V_O will change with temperature, variations in V_{DD} , and viewing angle. V_O will also vary module-to-module and batch-to-batch due to normal manufacturing variations.

Ideally, adjustments to V_O should be available to the end user so each user can adjust the display to the optimal contrast for their required viewing conditions. At a minimum, your design should allow V_O to be adjusted as part of your product's final test.

Although a potentiometer is shown as a typical connection, V_O can be driven by your microcontroller, either by using a DAC or a filtered PWM. Displays that require V_O to be negative may need a level-shifting circuit. Please do not hesitate to contact CrystalFontz application support for design assistance on your application.

ESD (ELECTRO-STATIC DISCHARGE) SPECIFICATIONS

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other static sensitive devices such as expansion cards, motherboards, or integrated circuits. Ground your body, work surfaces, and equipment.



OPTICAL SPECIFICATIONS

OPTICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MINIMUM	TYPICAL	MAXIMUM
Viewing Angle (6 o'clock) (Vertical, Horizontal)	(V) θ	CR \geq 2	-20°		35°
	(H) ϕ	CR \geq 2	-30°		30°
Contrast Ratio ¹	CR			3	
LCD Response Time ²	T rise	Ta = 25°C		250 ms	
	T fall	Ta = 25°C		250 ms	

¹Contrast Ratio = (brightness with pixels light)/(brightness with pixels dark).
²Response Time: The amount of time it takes a liquid crystal cell to go from active to inactive or back again.

OPTICAL DEFINITIONS

- Operating Voltage (V_{LCD}): V_{OP}
- Viewing Angle
 - Vertical (V) θ : 0°
 - Horizontal (H) ϕ : 0°
- Frame Frequency: 64 Hz
- Driving Waveform: 1/16 Duty, 1/5 Bias
- Ambient Temperature (Ta): 25°C



Definition of Operation Voltage (Vop)

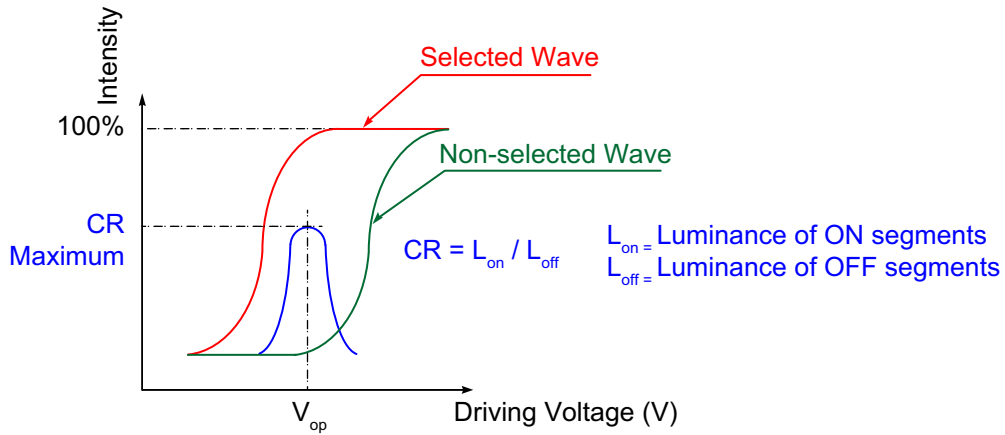


Figure 8. Definition of Operation Voltage (V_{OP}) (Negative)

Definition of Response Time (Tr, Tf)

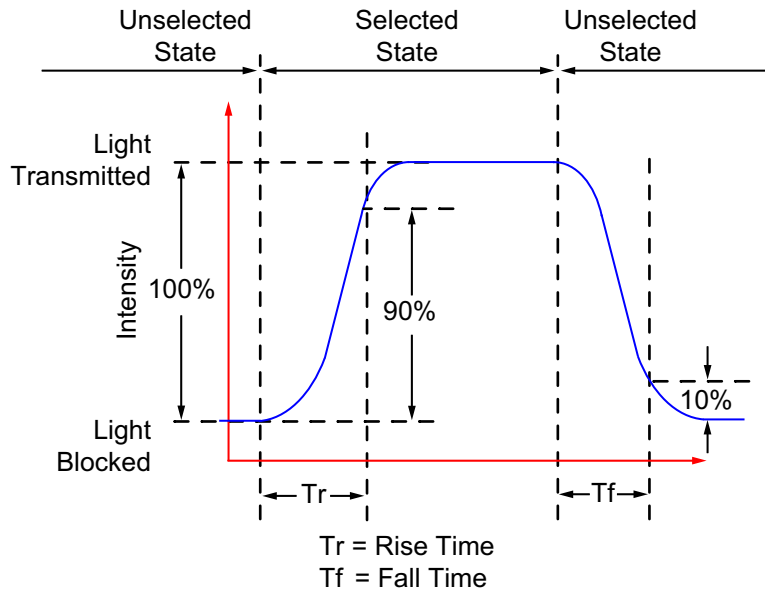


Figure 9. Definition of Response Time (Tr, Tf) (Negative)



Definition of Vertical and Horizontal Viewing Angles ($CR \geq 2$)

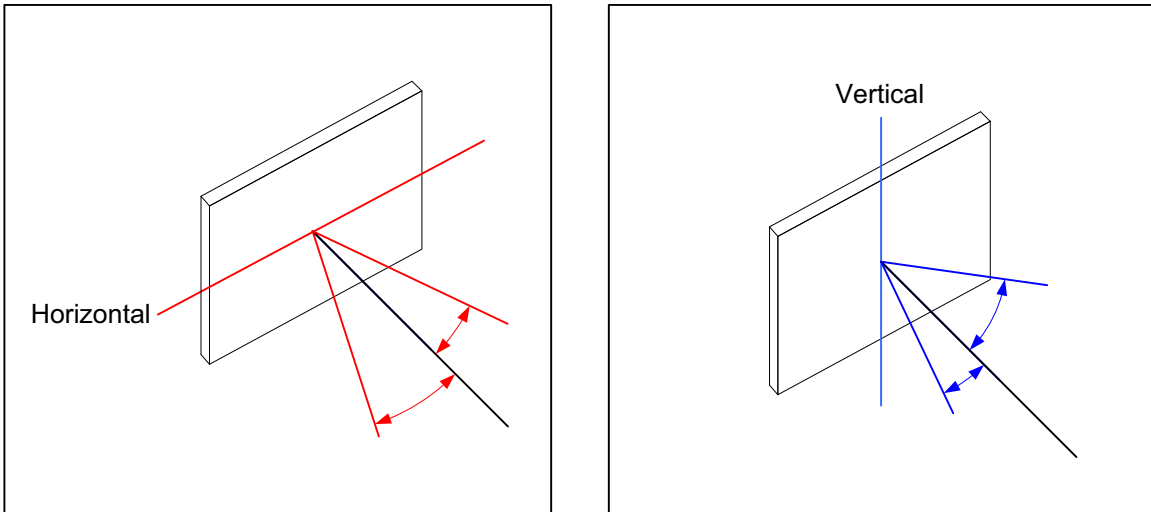


Figure 10. Definition of Horizontal and Vertical Viewing Angles ($CR > 2$)

Definition of 6 O'Clock and 12:00 O'Clock Viewing Angles

This module has a 6:00 o'clock viewing angle. A 6:00 o'clock viewing angle is a bottom viewing angle like what you would see when you look at a cell phone or calculator. A 12:00 o'clock viewing angle is a top viewing angle like what you would see when you look at the gauges in a golf cart or airplane.

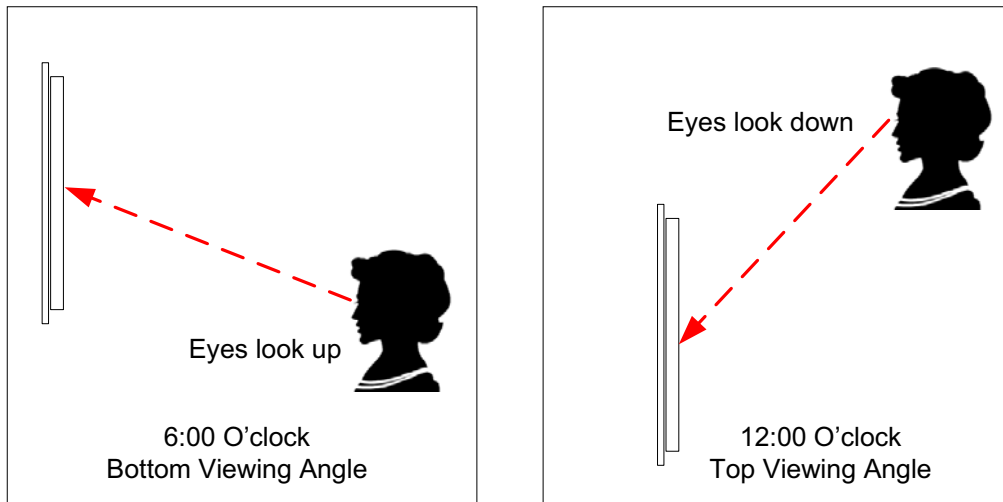


Figure 11. Definition of 6:00 O'Clock and 12:00 O'Clock Viewing Angles



LED BACKLIGHT CHARACTERISTICS

The CFAH2004K-TMI-JP uses an LED backlight. LED backlights are easy to use, but they are also easily damaged.

NOTE

Do not connect +5v directly to the backlight terminals. This will ruin the backlight.

LEDs are “current” devices. The important aspect of driving an LED is the current flowing through it, not the voltage across it. Ideally, a current source would be used to drive the LEDs. In practice, a simple current limiting resistor in line from a voltage source will work well in most applications and is much less complex than a current source.

You need to know what the forward voltage of the LEDs is so you can calculate the current limiting resistor (R_{LIMIT}). The forward voltage will vary slightly from display to display.

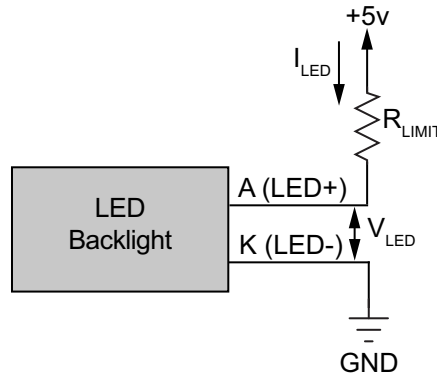


Figure 12. Typical LED Backlight Connections for “Always On”

The equation to calculate R_{LIMIT} is:

$$R_{LIMIT} \text{ (minimum)} = \frac{V_{DD} \text{ (Supply Voltage)} - V_{LED} \text{ (Typical LED Forward Voltage)}}{I_{LED} \text{ (Typical LED Forward Current)}}$$

The specific R_{LIMIT} calculation for the CFAH2004K-TMI-JP at $V_{DD} = +5v$ is:

$$R_{LIMIT} = \frac{5v - 4.0v}{0.03 \text{ A}} = 33.3\Omega \text{ (minimum)}$$

How to Calculate the Power Dissipation of the Resistor

The general equation to calculate the power dissipation of the resistor is:

$$P \text{ (power)} = I \text{ (current)} \times E \text{ (voltage)}$$

The specific power dissipation calculation for CFAH2004K-TMI-JP is:

$$\text{Power} = 0.06A \times (5v - 3.5v) = 0.09W = 90mW$$

Nominally, an 1/8 watt (125 mW) resistor should work. For longevity, we recommend a 1/4 or 1/2 watt resistor.



PWM Dimming

The backlight may be dimmed by PWM (Pulse Width Modulation). The typical range for the PWM frequency is from 100 to 300 Hz.

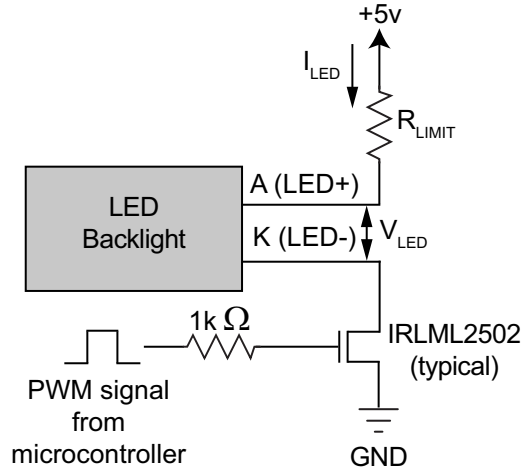


Figure 13. Example of LED Backlight Connections for PWM Dimming

LED Backlight Characteristics					
<i>light dots on blue background</i>					
ITEM	SYMBOL	TEST CONDITION	MINIMUM	TYPICAL	MAXIMUM
Forward Current	I_{LED}	$V = +4.0v$		30 mA	40 mA
Driving the backlight above 40 mA will shorten its lifetime.					
Forward Voltage	V_{LED}		+3.8v	+4.0v	+4.0v
Reverse Voltage (V_R)	V_R				+10v
Luminous Intensity	I_V	$I_{LED} = 30 mA$		29 cd/m ²	
The backlight is measured through the LCD. Direct backlight measurement is significantly brighter.					



LCD CONTROLLER INTERFACE

This module uses a Sunplus SPLC780D1 controller. The Sunplus SPLC780D1 is compatible with the industry standard Hitachi HD44780 controller. Software written for modules that use the HD44780 should work without modification.

For your reference, we added [APPENDIX C: SUNPLUS SPLC780D1 CONTROLLER DATA SHEET \(Pg. 31\)](#) to this Data Sheet.

DISPLAY POSITION DDRAM ADDRESS

The following table shows the relationship between the controller's addresses and the corresponding character location on the module.

		COLUMN																			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
ROW	0	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0xA	0xB	0xC	0xD	0xE	0xF	0x10	0x11	0x12	0x13
	1	0x40	0x41	0x42	0x43	0x44	0x45	0x46	0x47	0x48	0x49	0x4A	0x4B	0x4C	0x4D	0x4E	0x4F	0x50	0x51	0x52	0x53
	2	0x14	0x15	0x16	0x17	0x18	0x19	0x1A	0x1B	0x1C	0x1D	0x1E	0x1F	0x20	0x21	0x22	0x23	0x24	0x25	0x26	0x27
	3	0x54	0x55	0x56	0x57	0x58	0x59	0x5A	0x5B	0x5C	0x5D	0x5E	0x5F	0x60	0x61	0x62	0x63	0x64	0x65	0x66	0x67



CHARACTER GENERATOR ROM (CGROM)

To find the code for a given character, add the two numbers that are shown in bold for its row and column. For example, the lowercase “h” is in the column labeled “96₁₀” and in the row labeled “8₁₀”. So you would add 96 + 8 to get 104. When you send a byte with the value of 104 to the display, then a lowercase “h” will be shown. (See [APPENDIX C: SUNPLUS SPLC780D1 CONTROLLER DATA SHEET \(Pg. 31\)](#)).

upper lower 4 bits 4 bits	0 ₁₀ 0000 ₂	16 ₁₀ 0001 ₂	32 ₁₀ 0010 ₂	48 ₁₀ 0011 ₂	64 ₁₀ 0100 ₂	80 ₁₀ 0101 ₂	96 ₁₀ 0110 ₂	112 ₁₀ 0111 ₂	128 ₁₀ 1000 ₂	144 ₁₀ 1001 ₂	160 ₁₀ 1010 ₂	176 ₁₀ 1011 ₂	192 ₁₀ 1100 ₂	208 ₁₀ 1101 ₂	224 ₁₀ 1110 ₂	240 ₁₀ 1111 ₂	
0 ₁₀ 0000 ₂	CGRAM [0]			0	1	2	3	4	5	6	7	8	9	0	1	2	3
1 ₁₀ 0001 ₂	CGRAM [1]		!	1	A	Q	a	4				.	ア	チ	△	△	△
2 ₁₀ 0010 ₂	CGRAM [2]		"	2	B	R	b	r				"	イ	ウ	×	△	△
3 ₁₀ 0011 ₂	CGRAM [3]		#	3	C	S	c	s				」	ウ	テ	毛	△	△
4 ₁₀ 0100 ₂	CGRAM [4]		\$	4	D	T	d	t				√	エ	ト	カ	ワ	△
5 ₁₀ 0101 ₂	CGRAM [5]		%	5	E	U	e	u				・	オ	カ	工	△	△
6 ₁₀ 0110 ₂	CGRAM [6]		&	6	F	V	f	v				ヲ	カ	ニ	ヨ	△	△
7 ₁₀ 0111 ₂	CGRAM [7]		'	7	G	W	g	w				ヲ	チ	△	ラ	△	△
8 ₁₀ 1000 ₂			(8	H	X	h	x				イ	ウ	キ	リ	△	△
9 ₁₀ 1001 ₂)	9	I	Y	i	y				ウ	ク	リ	ル	△	△
10 ₁₀ 1010 ₂			*	:	J	Z	j	z				エ	コ	△	△	△	△
11 ₁₀ 1011 ₂			+	;	K	0	k	0				*	オ	△	△	△	△
12 ₁₀ 1100 ₂			,	<	L	#	l	#				カ	△	△	△	△	△
13 ₁₀ 1101 ₂			-	=	M	I	m	i				ユ	△	△	△	△	△
14 ₁₀ 1110 ₂			.	>	N	^	n	^				ヨ	△	△	△	△	△
15 ₁₀ 1111 ₂			/	?	O	_	o	_				ウ	△	△	△	△	△

Figure 14. Character Generator ROM (CGROM)



MODULE RELIABILITY AND LONGEVITY

MODULE RELIABILITY

ITEM	SPECIFICATION	
LCD excluding LED backlight	50,000 to 100,000 hours (typical)	
White LED Backlight ($I_{LED} \leq 30 \text{ mA}$)*	<i>Power-On Hours</i>	<i>% of Initial Brightness (New Module)</i>
* We recommend that the backlight of the white LED backlit modules be dimmed or turned off during periods of inactivity to conserve the white LED backlight lifetime.	<5,000	>90%
	<25,000	>50%

We list the lifetime of this white LED at <5,000 hours to emphasize that white LEDs do not have the extremely long lifetime typical of red or green LEDs. The white LEDs dim over time, especially if driven with high currents. The dimming may not be noticeable when a single display is installed. However, if a new display is installed next to a display that has been on continuously for a very long time, you will see the difference. To preserve the lifetime of white LEDs, we recommend that white LED backlights are dimmed or turned off when not needed. Also, please do not use more current than you need to achieve your brightness requirements.

MODULE LONGEVITY (EOL / REPLACEMENT POLICY)

Crystalfontz is committed to making all of our LCD modules available for as long as possible. For each module we introduce, we intend to offer it indefinitely. We do not preplan a module's obsolescence. The majority of modules we have introduced are still available.

We recognize that discontinuing a module may cause problems for some customers. However, rapidly changing technologies, component availability, or low customer order levels may force us to discontinue ("End of Life", EOL) a module. For example, we must occasionally discontinue a module when a supplier discontinues a component or a manufacturing process becomes obsolete. When we discontinue a module, we will do our best to find an acceptable replacement module with the same fit, form, and function.

In most situations, you will not notice a difference when comparing a "fit, form, and function" replacement module to the discontinued module it replaces. However, sometimes a change in component or process for the replacement module results in a slight variation, perhaps an improvement, over the previous design.

Although the replacement module is still within the stated Data Sheet specifications and tolerances of the discontinued module, changes may require modification to your circuit and/or firmware. Possible changes include:

- *LCD fluid, polarizers, or the LCD manufacturing process.* These items may change the appearance of the display, requiring an adjustment to V_O (See [Typical VO Connections for Display Contrast \(Pg. 15\)](#)).
- *Backlight LEDs.* Brightness may be affected (perhaps the new LEDs have better efficiency) or the current they draw may change (new LEDs may have a different VF).
- *Controller.* A new controller may require minor changes in your code.
- *Component tolerances.* Module components have manufacturing tolerances. In extreme cases, the tolerance stack can change the visual or operating characteristics.



Please understand that we avoid changing a module whenever possible; we only discontinue a module if we have no other option. We will post Part Change Notices on the product's web page as soon as possible. If interested, you can subscribe to future part change notifications.

CARE AND HANDLING PRECAUTIONS

For optimum operation of the module and to prolong its life, please follow the precautions below. Excessive voltage will shorten the life of the module. You must drive the display within the specified voltage limit. See [Temperature Range \(Pg. 10\)](#).

ESD (ELECTRO-STATIC DISCHARGE)

The circuitry is industry standard CMOS logic and susceptible to ESD damage. Please use industry standard antistatic precautions as you would for any other static sensitive devices such as expansion cards, motherboards, or integrated circuits. Ground your body, work surfaces, and equipment.

DESIGN AND MOUNTING

- The exposed surface of the “glass” is actually a polarizer laminated on top of the glass. To protect the soft plastic polarizer from damage, the module ships with a protective film over the polarizer. Please peel off the protective film slowly. Peeling off the protective film abruptly may generate static electricity.
- The polarizer is made out of soft plastic and is easily scratched or damaged. When handling the module, avoid touching the polarizer. Finger oils are difficult to remove.
- To protect the soft plastic polarizer from damage, place a transparent plate (for example, acrylic, polycarbonate, or glass) in front of the module, leaving a small gap between the plate and the display surface. We use GE HP-92 Lexan, which is readily available and works well.
- Do not disassemble or modify the module.
- Do not modify the tab of the metal holder or make connections to it.
- Do not reverse polarity to the power supply connections. Reversing polarity will immediately ruin the module.
- Use care to keep the exposed terminals clean. Contamination, including fingerprints, may make soldering difficult and the reliability of the soldered connection poor.
- For prototype work, hand soldering may be acceptable. Preset soldering iron to <math><260^{\circ}\text{C}</math>. Do not apply heat for more than 3 to 4 seconds.

AVOID SHOCK, IMPACT, TORQUE, AND TENSION

- Do not expose the module to strong mechanical shock, impact, torque, or tension.
- Do not drop, toss, bend, or twist the module.
- Do not place weight or pressure on the module.

IF LCD PANEL BREAKS

- If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or eyes.
- If the liquid crystal fluid touches your skin, clothes, or work surface, wash it off immediately using soap and plenty of water.
- Do not ingest the LCD panel.



CLEANING

- The polarizer (laminated to the glass) is soft plastic. The soft plastic is easily scratched or damaged. Be very careful when you clean the polarizer.
- Do not clean the polarizer with liquids. Do not wipe the polarizer with any type of cloth or swab (for example, Q-tips).
- Use the removable protective film to remove smudges (for example, fingerprints) and any foreign matter. If you no longer have the protective film, use standard transparent office tape (for example, Scotch® brand “Crystal Clear Tape”). If the polarizer is dusty, you may carefully blow it off with clean, dry, oil-free compressed air.

OPERATION

- We do not recommend connecting this module to a PC's parallel port as an "end product." This module is not "user friendly" and connecting them to a PC's parallel port is often difficult, frustrating, and can result in a "dead" display due to mishandling. For more information, see our forum thread at <http://www.crystalfontz.com/forum/showthread.php?s=&threadid=3257>.
- Your circuit should be designed to protect the module from ESD and power supply transients.
- Observe the operating temperature limitations: from -20°C minimum to +70°C maximum with minimal fluctuations. Operation outside of these limits may shorten the life and/or harm the display.
 - At lower temperatures of this range, response time is delayed.
 - At higher temperatures of this range, display becomes dark. (You may need to adjust the contrast.)
- Operate away from dust, moisture, and direct sunlight.

STORAGE AND RECYCLING

- Store in an ESD-approved container away from dust, moisture, and direct sunlight.
- Observe the storage temperature limitations: from -30°C minimum to +80°C maximum with minimal fluctuations. Rapid temperature changes can cause moisture to form, resulting in permanent damage.
- Do not allow weight to be placed on the modules while they are in storage.
- Please recycle your outdated Crystalfontz LCD modules at an approved facility.



APPENDIX A: QUALITY ASSURANCE STANDARDS

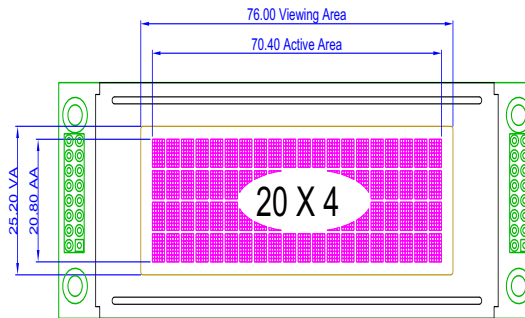
INSPECTION CONDITIONS

- Environment
 - Temperature: 25±5°C
 - Humidity: 30~85% RH (noncondensing)
- For visual inspection of active display area
 - Source lighting: two 20-Watt or one 40-Watt fluorescent light
 - Display adjusted for best contrast
 - Viewing distance: 30±5 cm (about 12 inches)
 - Viewing angle: inspect at 45° angle of vertical line right and left, top and bottom

COLOR DEFINITIONS

We try to describe the appearance of our LCD modules as accurately as possible. For the photos, we adjust the backlight (if any) and contrast for optimal appearance. Actual display appearance may vary due to (1) different operating conditions, (2) small variations of component tolerances, (3) inaccuracies of our camera, (4) color interpretation of the photos on your monitor, and/or (5) personal differences in the perception of color.

DEFINITION OF ACTIVE AREA AND VIEWING AREA



ACCEPTANCE SAMPLING

DEFECT TYPE	AQL*
Major	≤.65%
Minor	<1.0%
* Acceptable Quality Level: maximum allowable error rate or variation from standard	

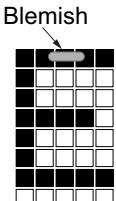
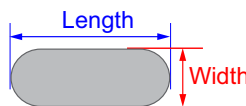
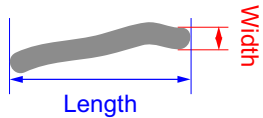


DEFECTS CLASSIFICATION

Defects are defined as:

- Major Defect: results in failure or substantially reduces usability of unit for its intended purpose
- Minor Defect: deviates from standards but is not likely to reduce usability for its intended purpose

ACCEPTANCE STANDARDS

#	DEFECT TYPE	CRITERIA			MAJOR / MINOR	
1	Electrical defects	1. No display, display malfunctions, or shorted segments. 2. Current consumption exceeds specifications.			Major	
2	Viewing area defect	Viewing area does not meet specifications.			Major	
3	Contrast adjustment defect	Contrast adjustment fails or malfunctions.			Major	
4	Blemishes or foreign matter on display segments		<i>Defect Size</i>	<i>Acceptable Qty</i>	Minor	
			≤0.30 mm	3		
			≤2 defects within 10 mm of each other			
5	Blemishes or foreign matter outside of display segments	Defect Size = (Width + Length)/2 	<i>Defect Size</i>	<i>Acceptable Qty</i>	Minor	
			≤0.15 mm	Ignore		
			0.15 to 0.20 mm	3		
			0.20 to 0.25 mm	2		
			> 0.30 mm	1		
6	Dark lines or scratches in display area		<i>Defect Width</i>	<i>Defect Length</i>	<i>Acceptable Qty</i>	Minor
			≤0.03 mm	≤3.0 mm	3	
			0.03 to 0.05	≤2.0 mm	2	
			0.05 to 0.08	≤2.0 mm	1	
			0.08 to 0.10	≤3.0 mm	0	
			≥0.10	>3.0 mm	0	



#	DEFECT TYPE	CRITERIA		MAJOR / MINOR
7	Bubbles between polarizer film and glass	<i>Defect Size</i>	<i>Acceptable Qty</i>	Minor
		≤0.20 mm	Ignore	
		0.20 to 0.40 mm	3	
		0.40 to 0.60 mm	2	
		≥0.60 mm	0	
8	Display pattern defect			Minor
		<i>Dot Size</i>	<i>Acceptable Qty</i>	
		$((A+B)/2) \leq 0.20$ mm	≤ 3 total defects ≤ 2 pinholes per digit	
		$C > 0$ mm		
		$((D+E)/2) \leq 0.25$ mm		
		$((F+G)/2) \leq 0.25$ mm		
9	Backlight defects	<ol style="list-style-type: none"> 1. Light fails or flickers.* 2. Color and luminance do not correspond to specifications.* 3. Exceeds standards for display's blemishes, foreign matter, dark lines or scratches. *Minor if display functions correctly. Major if the display fails.		Minor
10	PCB defects	<ol style="list-style-type: none"> 1. Oxidation or contamination on connectors.* 2. Wrong parts, missing parts, or parts not in specification.* 3. Jumpers set incorrectly. 4. Solder (if any) on bezel, LED pad, zebra pad, or screw hole pad is not smooth. *Minor if display functions correctly. Major if the display fails.		Minor
11	Soldering defects	<ol style="list-style-type: none"> 1. Unmelted solder paste. 2. Cold solder joints, missing solder connections, or oxidation.* 3. Solder bridges causing short circuits.* 4. Residue or solder balls. 5. Solder flux is black or brown. *Minor if display functions correctly. Major if the display fails.		Minor



APPENDIX B: APPLICATION NOTE FOR 3.3V OPERATION

This module can be used with a 3.3v power supply. In order to meet the requirements of V_{LCD} , you must provide a negative voltage source for V_O (pin 3, see [Details of Interface Pin Functions \(Pg. 12\)](#)). You need to drive V_O to below ground (typically -1v or -2v) until the V_{LCD} is met, making display contrast acceptable.

You can supply the negative voltage by one of the following methods:

1. Use an available source for the negative voltage.

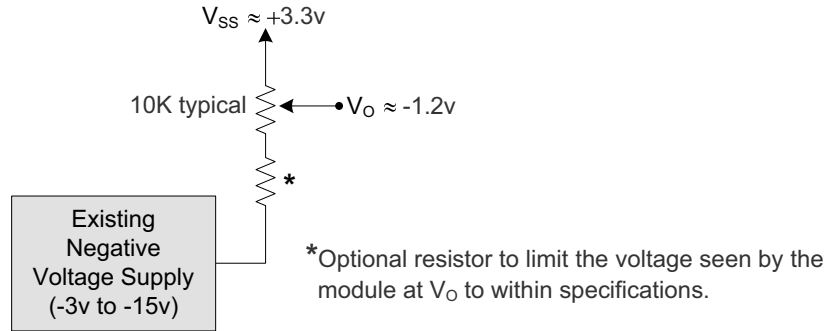


Figure 1. Use Existing Negative Voltage Supply

2. Use a “7660” CMOS switched-capacitor voltage converter or one of the many other available solutions for creating a negative voltage from a positive supply.

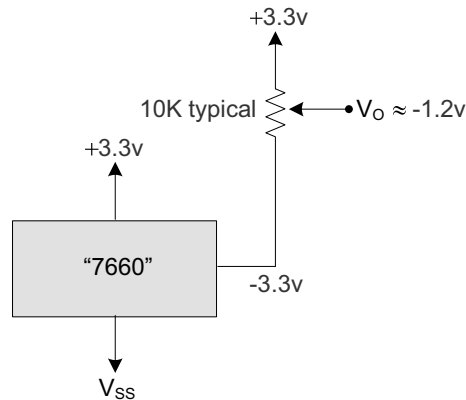


Figure 2. “7660” Switched-Capacitor Voltage Converter



- Use the circuit in the figure below to create the voltage for V_O by using a PWM (Pulse Width Modulation) output of your microcontroller. This circuit allows the contrast to be adjusted under software control.

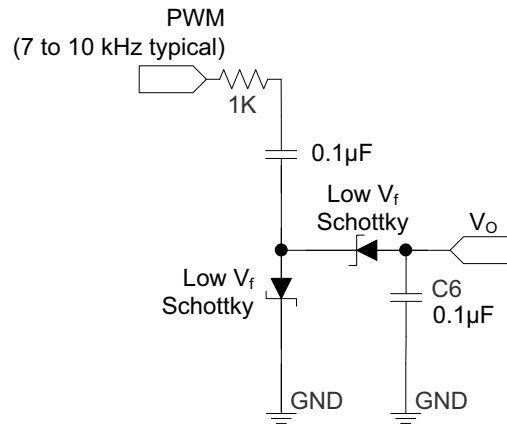


Figure 3. V_O Driving Circuit

Since V_O is pulled up internally by the LCD controller, this circuit will produce positive ($\approx +1\text{v}$) V_{LCD} ($V_{LCD} = \text{small}$, contrast is light) for low ($\approx 10\%$) or high (90%) duty cycles. For duty cycles near 50% , this circuit will produce negative ($\approx -2\text{v}$) levels of V_O ($V_{LCD} = \text{big}$, contrast is dark).

- Replace this module with the module in this series that has an on-board negative voltage generator. (The part number has a "V" at the end of it.)

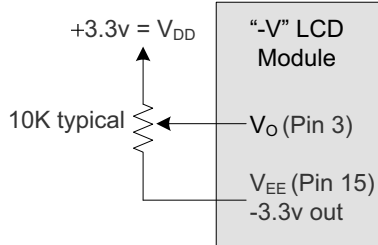


Figure 4. On-Board Negative Voltage Generator



APPENDIX C: SUNPLUS SPLC780D1 CONTROLLER DATA SHEET

The complete *Sunplus SPLC780D1 16COM/40SEG Controller/Driver Data Sheet* (September 21, 2007, 46 pages) follows.

SPLC780D1

16COM/40SEG Controller/Driver

Preliminary

SEP. 21, 2007

Version 0.1

Table of Contents

	<u>PAGE</u>
1. GENERAL DESCRIPTION	4
2. FEATURES	4
3. ORDERING INFORMATION	4
4. BLOCK DIAGRAM	5
5. SIGNAL DESCRIPTIONS	6
6. COMPARISON OF SPLC780D AND SPLC780D1	6
7. FUNCTIONAL DESCRIPTIONS	7
7.1. OSCILLATOR	7
7.2. CONTROL AND DISPLAY INSTRUCTIONS	7
7.3. INSTRUCTION TABLE	9
7.4. 8-BIT OPERATION AND 8-DIGIT 1-LINE DISPLAY (USING INTERNAL RESET)	10
7.5. 4-BIT OPERATION AND 8-DIGIT 1-LINE DISPLAY (USING INTERNAL RESET)	11
7.6. 8-BIT OPERATION AND 8-DIGIT 2-LINE DISPLAY (USING INTERNAL RESET)	11
7.7. RESET FUNCTION	12
7.8. DISPLAY DATA RAM (DD RAM)	14
7.9. TIMING GENERATION CIRCUIT	14
7.10. LCD DRIVER CIRCUIT	14
7.11. CHARACTER GENERATOR ROM (CG ROM)	14
7.12. CHARACTER GENERATOR RAM (CG RAM)	14
7.13. CURSOR/BLINK CONTROL CIRCUIT	18
7.14. INTERFACING TO MPU	19
7.15. SUPPLY VOLTAGE FOR LCD DRIVE	20
7.16. REGISTER --- IR (INSTRUCTION REGISTER) AND DR (DATA REGISTER)	23
7.17. BUSY FLAG (BF)	23
7.18. ADDRESS COUNTER (AC)	23
7.19. I/O PORT CONFIGURATION	23
8. ELECTRICAL SPECIFICATIONS	24
8.1. ABSOLUTE MAXIMUM RATINGS	24
8.2. DC CHARACTERISTICS (VDD = 2.7V TO 4.5V, T _A = 25°C)	24
8.3. AC CHARACTERISTICS (VDD = 2.7V TO 4.5V, T _A = 25°C)	25
8.4. DC CHARACTERISTICS (VDD = 4.5V TO 5.5V, T _A = 25°C)	26
8.5. AC CHARACTERISTICS (VDD = 4.5V TO 5.5V, T _A = 25°C)	26
9. APPLICATION CIRCUITS	29
9.1. R-OSCILLATOR	29
9.2. INTERFACE TO MPU	29
9.3. SPLC780D1 APPLICATION CIRCUIT	30
9.4. APPLICATIONS FOR LCD	31
10. CHARACTER GENERATOR ROM	33
10.1. SPLC780D1 - 001A	33
10.2. SPLC780D1 - 002A	34
10.3. SPLC780D1 - 003A	35
10.4. SPLC780D1 - 011A	36

10.5.SPLC780D1 – 021A.....	37
11. PACKAGE/PAD LOCATIONS	38
11.1. PAD ASSIGNMENT	38
11.2. PAD LOCATIONS.....	39
11.3. PIN ASSIGNMENT	40
11.4. PACKAGE INFORMATION (SPLC780D1-NNNV-HQ051)	41
12. LEAD FRAME PACKAGE PCB DESIGN AND MANUFACTURING GUIDELINES	42
13. DISCLAIMER.....	45
14. REVISION HISTORY	46

16COM/40SEG CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The SPLC780D1, a dot-matrix LCD controller and driver from ORISE, is a unique design for displaying alpha-numeric, Japanese-Kana characters and symbols. The SPLC780D1 provides two types of interfaces to MPU: 4-bit and 8-bit interfaces. The transferring speed of 8-bit is twice faster than 4-bit. A single SPLC780D1 is able to display up to two 8-character lines. By cascading with SPLC100 or SPLC063, the display capability can be extended. The CMOS technology ensures the power saves in the most efficient way and the performance keeps in the highest rank.

2. FEATURES

- Character generator ROM: 10880 bits
 - Character font 5 x 8 dots: 192 characters
 - Character font 5 x 10 dots: 64 characters
- Character generator RAM: 512 bits
 - Character font 5 x 8 dots: 8 characters
 - Character font 5 x 10 dots: 4 characters
- 4-bit or 8-bit MPU interfaces
- Direct driver for LCD: 16 COMs x 40 SEGs
- Duty factor (selected by program):
 - 1/8 duty: 1 line of 5 x 8 dots
 - 1/11 duty: 1 line of 5 x 10 dots
 - 1/16 duty: 2 lines of 5 x 8 dots / line
- Built-in power on automatic reset circuit
- Built-in oscillator circuit (with external resistor)
- Support external clock operation
- Low Power Consumption
- Package form: 80 QFP or bare chip available

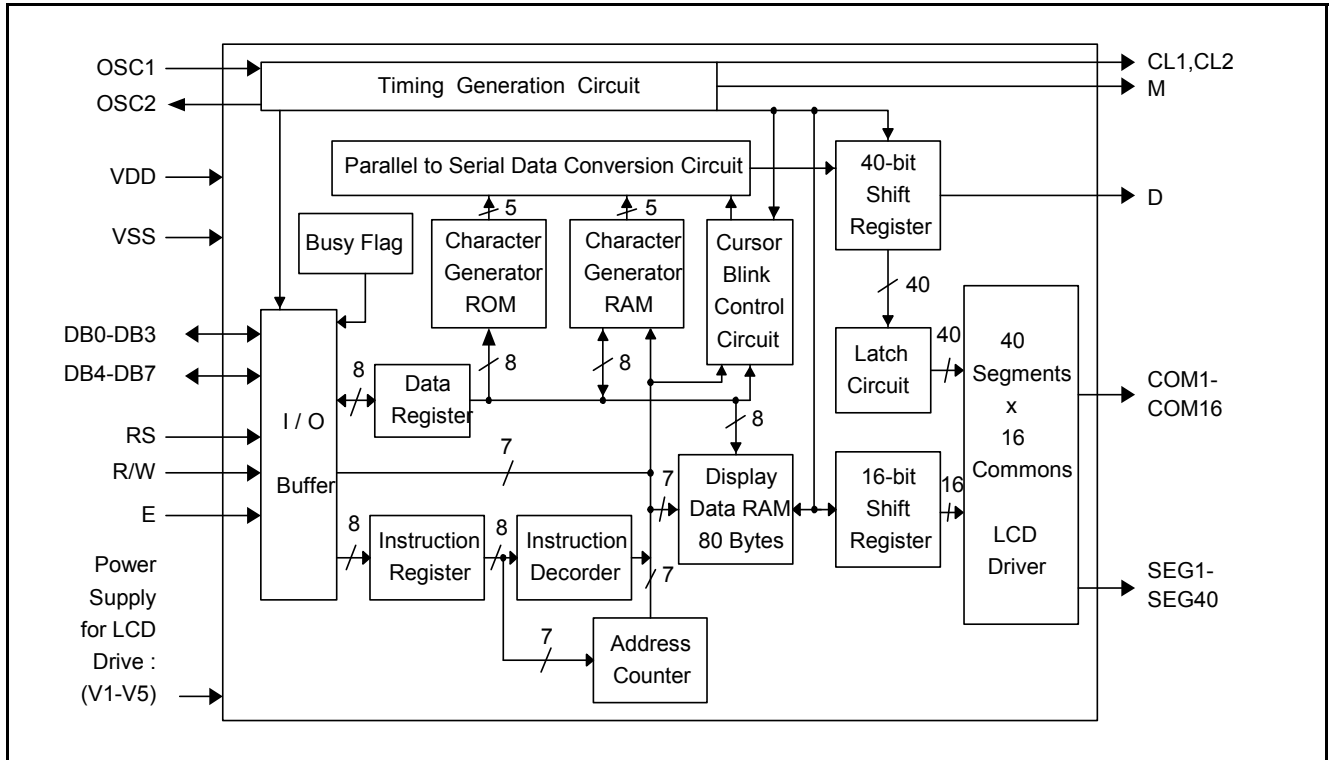
3. ORDERING INFORMATION

Product Number	Package Type
SPLC780D1-NnnV-C	Chip form
SPLC780D1-NnnV-HQ051	Green Package form - QFP 80L

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

4. BLOCK DIAGRAM



5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	33	I	Power input
VSS	23	I	Ground
OSC1 OSC2	24 25	-	Both OSC1 and OSC2 are connected to resist or for internal oscillator circuit. For external clock operation, the clock is input to OSC1.
V1 - V5	26 - 30	I	Supply voltage for LCD driving.
E	38	I	A start signal for reading or writing data.
R/W	37	I	A signal for selecting read or write actions. 1: Read, 0: Write.
RS	36	I	A signal for selecting registers. 1: Data Register (for read and write) 0: Instruction Register (for write), Busy flag - Address Counter (for read).
DB0 - DB3	39 - 42	I/O	Low 4-bit data
DB4 - DB7	43 - 46	I/O	High 4-bit data
CL1	31	O	Clock to latch serial data D.
CL2	32	O	Clock to shift serial data D.
M	34	O	Switch signal to convert LCD waveform to AC.
D	35	O	Sends character pattern data corresponding to each common signal serially. 1: Selection, 0: Non-selection.
SEG1 - SEG22 SEG23 - SEG40	22 - 1 80 - 63	O	Segment signals for LCD.
COM1 - COM16	47 - 62	O	Common signals for LCD.

6. COMPARISON OF SPLC780D AND SPLC780D1

	SPLC780D	SPLC780D1	Memo
Chip size	2860u*2450u	2860u*2450u	
PAD Size	90u * 90u	90u * 90u	Passivation Opening Window
Min. PAD Pitch	110u	110u	
LCD Voltage(V _{LCD})	3V ~ 9V	3V ~ 8V	
Absolute Maximum Rating	12v	10v	

Note: SPLC780D1 and SPLC780D have the same chip size and pad location.

7. FUNCTIONAL DESCRIPTIONS

7.1. Oscillator

SPLC780D1 oscillator supports not only the internal oscillator operation, but also the external clock operation.

7.2. Control and Display Instructions

Control and display instructions are described in details as follows:

7.2.1. Clear display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

It clears the entire display and sets Display Data RAM Address 0 in Address Counter.

7.2.2. Return home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

X: Do not care (0 or 1)

It sets Display Data RAM Address 0 in Address Counter and the display returns to its original position. The cursor or blink goes to the most-left side of the display (to the 1st line if 2 lines are displayed). The contents of the Display Data RAM do not change.

7.2.3. Entry mode set

During writing and reading data, it defines cursor moving direction and shifts the display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D = 1: Increment, I/D = 0: Decrement.

S = 1: The display shift, S = 0: The display does not shift.

S = 1	I/D = 1	It shifts the display to the left
S = 1	I/D = 0	It shifts the display to the right

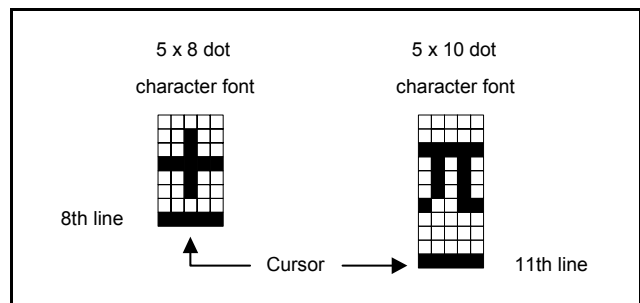
7.2.4. Display ON/OFF control

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

D = 1: Display on, D = 0: Display off

C = 1: Cursor on, C = 0: Cursor off

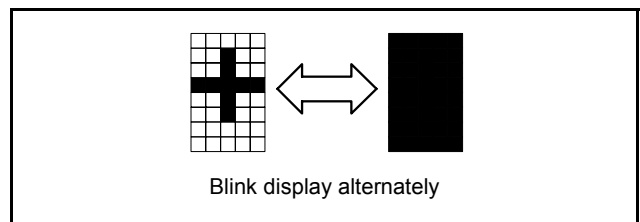
B = 1: Blinks on, B = 0: Blinks off



7.2.5. Cursor or display shift

Without changing DD RAM data, it moves cursor and shifts display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X



S/C	R/L	Description	Address Counter
0	0	Shift cursor to the left	AC = AC - 1
0	1	Shift cursor to the right	AC = AC + 1
1	0	Shift display to the left. Cursor follows the display shift	AC = AC
1	1	Shift display to the right. Cursor follows the display shift	AC = AC

7.2.6. Function set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

X: Do not care (0 or 1)

DL: It sets interface data length.

DL = 1: Data transferred with 8-bit length (DB7 - 0).

DL = 0: Data transferred with 4-bit length (DB7 - 4).

It requires two times to accomplish data transferring.

N: It sets the number of the display line.

N = 0: One-line display.

N = 1: Two-line display.

F: It sets the character font.

F = 0: 5 x 8 dots character font.

F = 1: 5 x 10 dots character font.

N	F	No. of Display Lines	Character Font	Duty Factor
0	0	1	5 x 8 dots	1 / 8
0	1	1	5 x 10 dots	1 / 11
1	X	2	5 x 8 dots	1 / 16

It cannot display two lines with 5 x 10 dots character font.

7.2.7. Set character generator RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	a	a	a	a	a	a

It sets Character Generator RAM Address (aaaaaa)₂ to the Address Counter.

Character Generator RAM data can be read or written after this setting.

7.2.8. Set display data RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	a	a	a	a	a	a	a

It sets Display Data RAM Address (aaaaaa)₂ to the Address Counter.

Display data RAM can be read or written after this setting.

In one-line display (N = 0),

$$(aaaaaaa)_2: (00)_{16} - (4F)_{16}.$$

In two-line display (N = 1),

$$(aaaaaaa)_2: (00)_{16} - (27)_{16} \text{ for the first line,}$$

$$(aaaaaaa)_2: (40)_{16} - (67)_{16} \text{ for the second line.}$$

7.2.9. Read busy flag and address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	a	a	a	a	a	a	a

When BF = 1, it indicates the system is busy now and it will not accept any instruction until not busy (BF = 0). At the same time, the content of Address Counter (aaaaaaa)₂ is read.

7.2.10. Write data to character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	d	d	d	d	d	d	d	d

It writes data (ddddddd)₂ to character generator RAM or display data RAM.

7.2.11. Read data from character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	d	d	d	d	d	d	d	d

It reads data (ddddddd)₂ from character generator RAM or display data RAM.

To read data correctly, do the following:

- 1). The address of the Character Generator RAM or Display Data RAM or shift the cursor instruction.
- 2). The "Read" instruction.

7.3. Instruction Table

Instruction	Instruction Code										Description	Execution time (Temp = 25°C)		
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		Fosc= 190KHz	Fosc= 270KHz	Fosc= 350KHz
Clear Display	0	0	0	0	0	0 0		0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	2.16ms	1.52ms	1.18ms
Return Home	0	0	0	0	0	0 0		0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	2.16ms	1.52ms	1.18ms
Entry Mode Set	0	0	0	0	0	0 0		1	I/D	S	Assign cursor moving direction and enable the shift of entire display	53μs	38μs	29μs
Display ON/OFF Control	0	0	0	0	0	0 1		D	C	B	Set display (D), cursor(C), and blinking of cursor(B) on/off control bit.	53μs	38μs	29μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	53μs	38μs	29μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5x10 dots/5x8 dots)	53μs	38μs	29μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	53μs	38μs	29μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	53μs	38μs	29μs
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.			
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	53μs	38μs	29μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	53μs	38μs	29μs

Note1: "--": don't care

Note2: In the operation condition under -20°C ~ 75°C, the maximum execution time for majority of instruction sets is 100us, except two instructions, "Clear Display" and "Return Home", in which maximum execution time can take up to 4.1ms.

7.4. 8-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on. (SPLC780D1 starts initializing)	<input type="text"/>	Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 <input type="text" value="0 0 0 0 1 1 0 0 X X"/>	<input type="text"/>	Set to 8-bit operation and select 1-line display line and character font.
3	Display on / off control <input type="text" value="0 0 0 0 0 0 1 1 1 0"/>	<input type="text" value="-"/>	Display on. Cursor appear.
4	Entry mode set <input type="text" value="0 0 0 0 0 0 0 1 1 0"/>	<input type="text" value="-"/>	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 1 0 1 1 1"/>	<input type="text" value="W_"/>	Write " W ". The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 0 0 1 0 1"/>	<input type="text" value="WE_"/>	Write " E ". The cursor is incremented by one and shifted to the right.
7	:	:	
8	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 0 0 1 0 1"/>	<input type="text" value="WELCOME_"/>	Write " E ". The cursor is incremented by one and shifted to the right.
9	Entry mode set <input type="text" value="0 0 0 0 0 0 0 1 1 1"/>	<input type="text" value="WELCOME_"/>	Set mode for display shift when writing
10	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 0 1 0 0 0 0 0"/>	<input type="text" value="ELCOME_"/>	Write " "(space). The cursor is incremented by one and shifted to the right.
11	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 0 0 0 1 1"/>	<input type="text" value="LCOME C_"/>	Write " C ". The cursor is incremented by one and shifted to the right.
12	:	:	
13	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 1 1 0 0 1"/>	<input type="text" value="COMPAMY_"/>	Write " Y ". The cursor is incremented by one and shifted to the right.
14	Cursor or display shift <input type="text" value="0 0 0 0 0 1 0 0 X X"/>	<input type="text" value="COMPAMY_"/>	Only shift the cursor's position to the left (Y).
15	Cursor or display shift <input type="text" value="0 0 0 0 0 1 0 0 X X"/>	<input type="text" value="COMPAMY_"/>	Only shift the cursor's position to the left (M).
16	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 0 1 1 1 0"/>	<input type="text" value="OMPANY_"/>	Write " N ". The display moves to the left.
17	Cursor or display shift <input type="text" value="0 0 0 0 0 1 1 1 X X"/>	<input type="text" value="COMPAMY_"/>	Shift the display and the cursor's position to the right.
18	Cursor or display shift <input type="text" value="0 0 0 0 0 1 0 1 X X"/>	<input type="text" value="OMPANY_"/>	Shift the display and the cursor's position to the right.
19	Write data to CG RAM / DD RAM <input type="text" value="1 0 0 1 0 0 0 0 0 0"/>	<input type="text" value="COMPAMY_"/>	Write " " (space). The cursor is incremented by one and shifted to the right.
20	:	:	:
21	Return home <input type="text" value="0 0 0 0 0 0 0 0 1 0"/>	<input type="text" value="WELCOME_"/>	Both the display and the cursor return to the original position (address 0).

7.5. 4-Bit Operation and 8-Digit 1-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on. (SPLC780D1 starts initializing)	<input type="text"/>	Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 <input type="text"/>	<input type="text"/>	Set to 4-bit operation.
3	<input type="text"/> <input type="text"/>	<input type="text"/>	Set to 4-bit operation and select 1-line display line and character font.
4	<input type="text"/> <input type="text"/>	<input type="text"/>	Display on. Cursor appears.
5	<input type="text"/> <input type="text"/>	<input type="text"/>	Increase address by one. It will shift the cursor to the right when writing to the DD RAM / CG RAM. Now the display has no shift.
6	<input type="text"/> <input type="text"/>	<input type="text"/>	Write " W ". The cursor is incremented by one and shifted to the right.

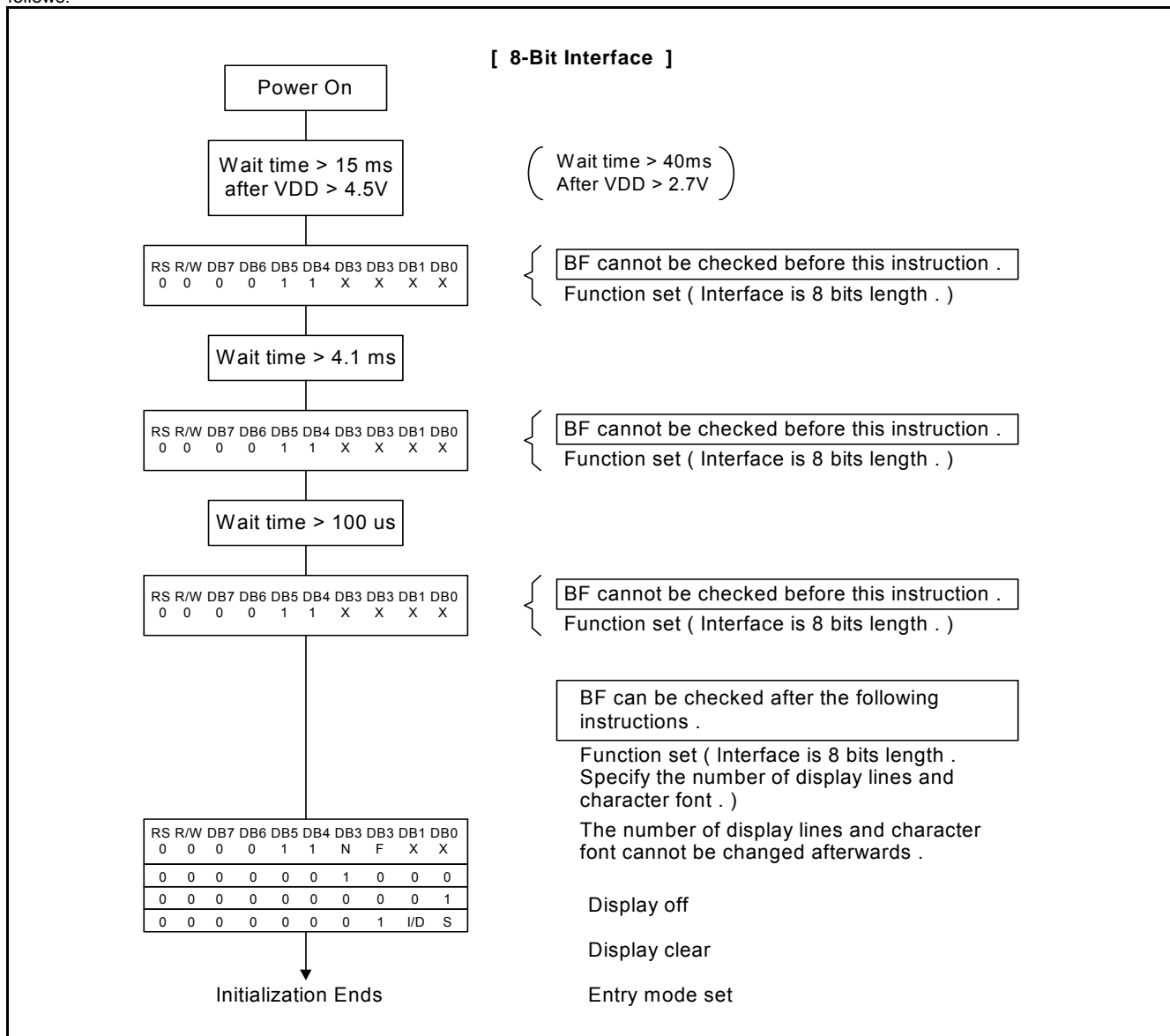
7.6. 8-Bit Operation and 8-Digit 2-Line Display (Using Internal Reset)

No.	Instruction	Display	Operation
1	Power on. (SPLC780D1 starts initializing)	<input type="text"/> <input type="text"/>	Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 <input type="text"/>	<input type="text"/> <input type="text"/>	Set to 8-bit operation and select 2-line display line and 5 x 8 dot character font.
3	Display on / off control <input type="text"/>	<input type="text"/> <input type="text"/>	Display on. Cursor appear.
4	Entry mode set <input type="text"/>	<input type="text"/> <input type="text"/>	Increase address by one. It will shift the cursor to the right when writing to the DD RAM / CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM <input type="text"/>	<input type="text"/> <input type="text"/>	Write " W ". The cursor is incremented by one and shifted to the right.
6	:	:	:
7	Write data to CG RAM / DD RAM <input type="text"/>	<input type="text"/> <input type="text"/>	Write " E ". The cursor is incremented by one and shifted to the right.
8	Set DD RAM address <input type="text"/>	<input type="text"/> <input type="text"/>	It sets DD RAM's address. The cursor is moved to the beginning position of the 2nd line.
9	Write data to CG RAM / DD RAM <input type="text"/>	<input type="text"/> <input type="text"/>	Write " T ". The cursor is incremented by one and shifted to the right.
10	:	:	:
11	Write data to CG RAM / DD RAM <input type="text"/>	<input type="text"/> <input type="text"/>	Write " T ". The cursor is incremented by one and shifted to the right.

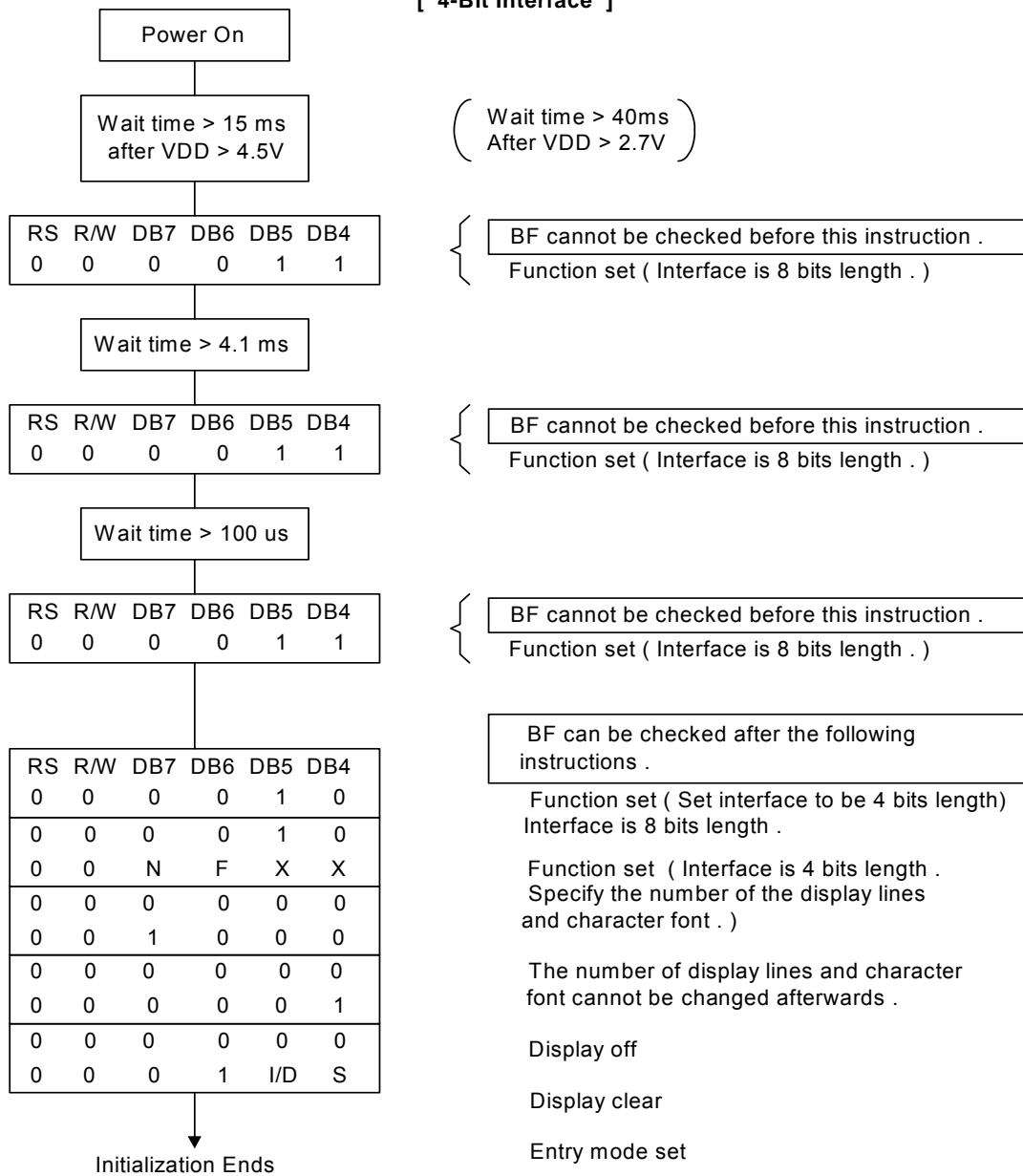
No.	Instruction	Display	Operation												
12	Entry mode set <table border="1" style="margin-left: 20px;"> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td> </tr> </table>	0	0	0	0	0	0	0	1	1	1	<table border="1" style="margin-left: 20px;"> <tr> <td>WELCOME</td> </tr> <tr> <td>TO PART_</td> </tr> </table>	WELCOME	TO PART_	When writing, it sets mode for the display shift.
0	0	0	0	0	0	0	1	1	1						
WELCOME															
TO PART_															
13	Write data to CG RAM / DD RAM <table border="1" style="margin-left: 20px;"> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td> </tr> </table>	1	0	0	1	0	1	1	0	0	1	<table border="1" style="margin-left: 20px;"> <tr> <td>ELCOME</td> </tr> <tr> <td>O PARTY_</td> </tr> </table>	ELCOME	O PARTY_	Write " Y ". The cursor is incremented by one and shifted to the right.
1	0	0	1	0	1	1	0	0	1						
ELCOME															
O PARTY_															
14	:	:	:												
15	Return home <table border="1" style="margin-left: 20px;"> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td> </tr> </table>	0	0	0	0	0	0	0	0	1	0	<table border="1" style="margin-left: 20px;"> <tr> <td>WELCOME</td> </tr> <tr> <td>TO PARTY</td> </tr> </table>	WELCOME	TO PARTY	Both the display and the cursor return to the original position (address 0).
0	0	0	0	0	0	0	0	1	0						
WELCOME															
TO PARTY															

7.7. Reset Function

At power on, SPLC780D1 starts the internal auto-reset circuit and executes the initial instructions. The initial procedures are shown as follows:



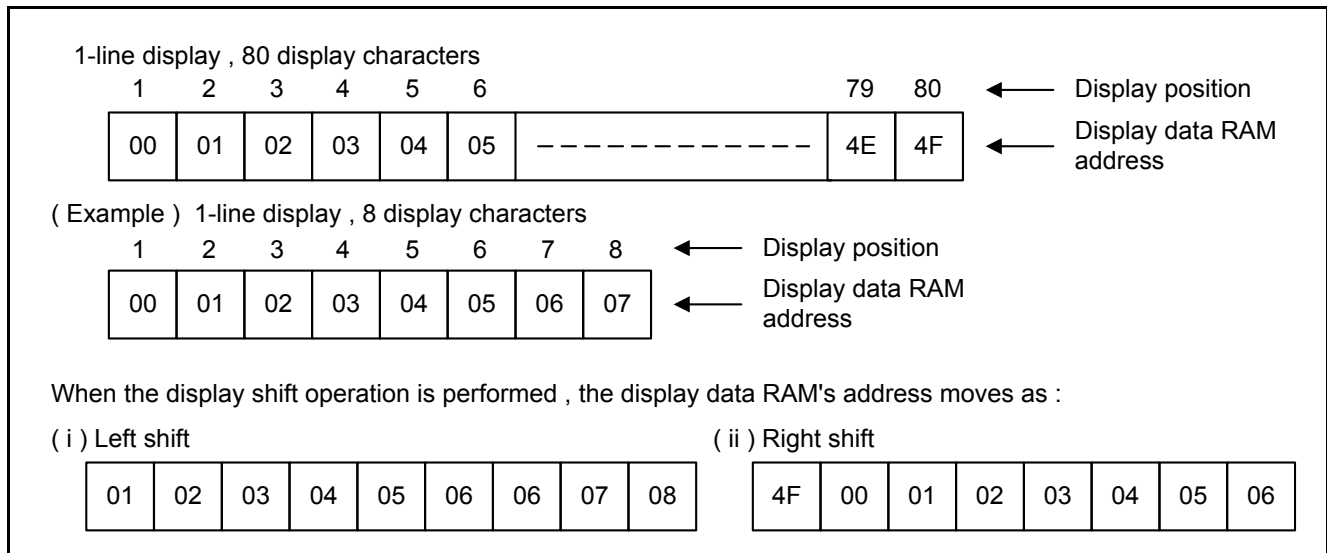
[4-Bit Interface]



7.8. Display Data RAM (DD RAM)

The 80-bit DD RAM is normally used for storing display data. Those DD RAM not used for display data can be used as general data RAM. Its address is configured in the Address Counter.

The relationships between Display Data RAM Address and LCD's position are depicted as follows.



7.9. Timing Generation Circuit

The timing generating circuit is a ble to generate timing signals to the internal circuits. In order to prevent the internal timing interface, the MPU access timing and the RAM access timing are generated independently.

7.10. LCD Driver Circuit

Total of 16 commons and 40 segments signal drivers are valid in the LCD driver circuit. When a program specifies the character fonts and line numbers, the corresponding common signals output drive-waveforms and the others still output unselected waveforms.

7.11. Character Generator ROM (CG ROM)

Using 8-bit character code, the character generator ROM generates 5 x 8 dots or 5 x 10 dots character patterns. It also can generate 192's 5 x 8 dots character patterns and 64's 5 x 10 dots character patterns.

7.12. Character Generator RAM (CG RAM)

Users can easily change the character patterns in the character generator RAM through program. It can be written to 5 x 8 dots, 8-character patterns or 5 x 10 dots for 4-character patterns.

The following diagram shows the SPLC780D1 character patterns:

Correspondence between Character Codes and Character Patterns.

		Higher 4-bit (D4 to D7) of Character Code (Hexadecimal)																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
Lower 4-bit (D0 to D3) of Character Code (Hexadecimal)	0	CG RAM (1)																
	1	CG RAM (2)																
	2	CG RAM (3)																
	3	CG RAM (4)																
	4	CG RAM (5)																
	5	CG RAM (6)																
	6	CG RAM (7)																
	7	CG RAM (8)																
	8	CG RAM (1)																
	9	CG RAM (2)																
	A	CG RAM (3)																
	B	CG RAM (4)																
	C	CG RAM (5)																
	D	CG RAM (6)																
	E	CG RAM (7)																
	F	CG RAM (8)																

The relationships between Character Generator RAM Addresses, Character Generator RAM Data (character patterns), and Character Codes are depicted as follows:



7.12.1. 5 x 8 dot character patterns

Character Code (DD RAM Data)								CG RAM Address						Character Patterns (CG RAM Data)												
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0					
0	0	0	0	X	/	/	/	/	/	/	0	0	0	/	/	/	/	/	/	/	1	1	1	1	1	
											0	0	1								0	0				
											0	1	0								0	0				
											0	1	1								0	0				
											1	0	0								0	0				
											1	0	1								0	0				
											1	1	0								0	0				
											1	1	1								0	0				
0	0	0	0	X	/	/	/	/	/	/	0	0	0	/	/	/	/	/	/	/	/	0	1	1	1	0
											0	0	1									0	0			
											0	1	0									0	0			
											0	1	1									0	0			
											1	0	0									0	0			
											1	0	1									0	0			
											1	1	0									0	0			
											1	1	1									0	0			

Character Pattern Example (1)

Cursor Position ←

Character Pattern Example (2)



- Note1:**  It means that the bit0~2 of the character code correspond to the bit3~5 of the CG RAM address.
- Note2:**  These areas are not used for display, but can be used for the general data RAM.
- Note3:** When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.
- Note4:** " 1 " : Selected, " 0 " : No selected, " X " : Do not care (0 or 1).
- Note5:** For example (1), set character code (b2 = b1 = b0 = 0, b3 = 0 or 1, b7-b4 = 0) to display " T ". That means character code (00) 16, and (08) 16 can display " T " character.
- Note6:** The bits 0-2 of the character code RAM is the character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.

7.12.2. 5 X 10 dot character patterns

Character Code (DD RAM Data)								CG RAM Address						Character Patterns (CG RAM Data)								
b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0	
										0	0	0	0					1	0	0	0	1
										0	0	0	1					1	0	0	0	1
										0	0	1	0					1	0	0	0	1
										0	0	1	1					1	0	0	0	1
										0	1	0	0					1	0	0	0	1
0	0	0	0	X	0	0	X	0	0	0	1	0	1	X	X	X	1	0	0	0	1	
										0	1	1	0					1	0	0	0	1
										0	1	1	1					1	0	0	0	1
										1	0	0	0					1	0	0	0	1
										1	0	0	1					1	1	1	1	1
										1	0	1	0					0	0	0	0	0
										1	0	1	1									
										1	1	0	0									
										1	1	0	1					X	X	X	X	X
										1	1	1	0									
										1	1	1	1									

 Character
 Pattern
 Example (1)

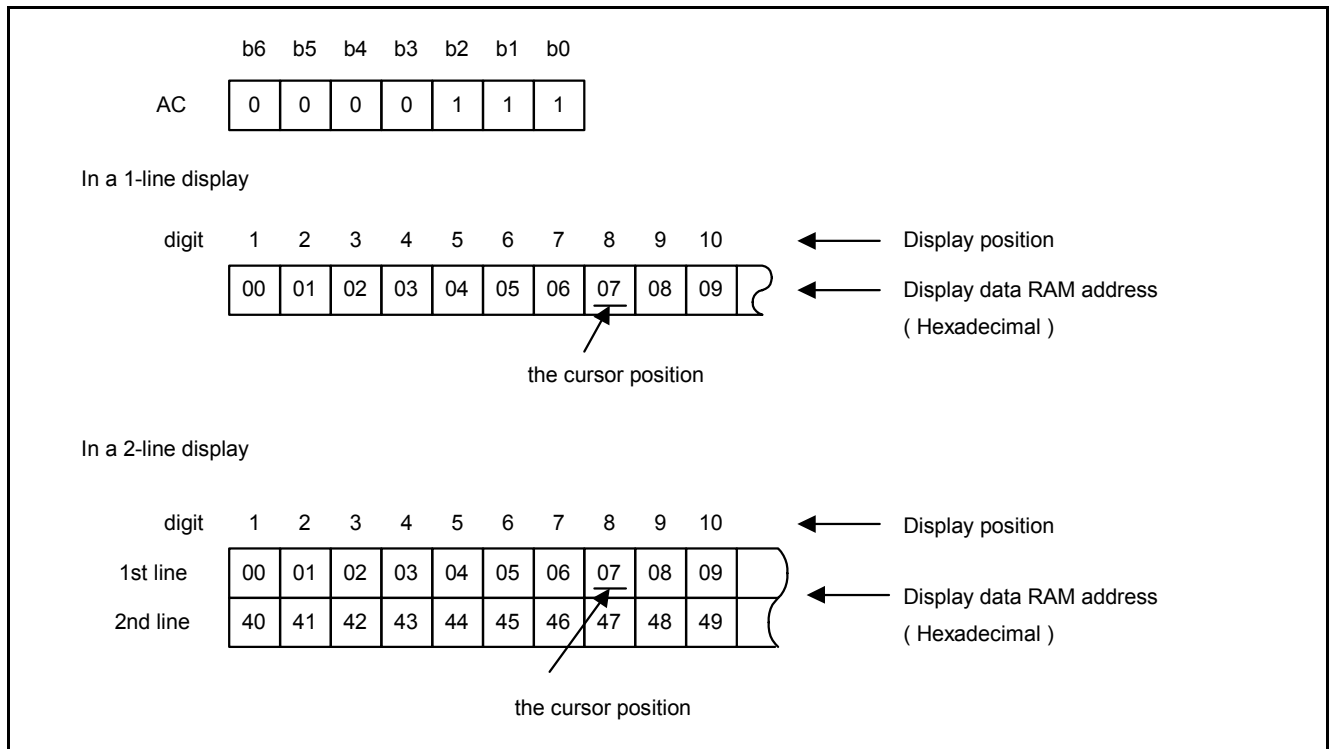
 Cursor
 Position
 ←

- Note1:**  It means that the bit1~2 of the character code correspond to the bit4~5 of the CG RAM address.
- Note2:**  These areas are not used for display, but can be used for the general data RAM.
- Note3:** When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.
- Note4:** " 1 ": Selected, " 0 ": No selected, " X ": Do not care (0 or 1).
- Note5:** For example (1), set character code (b2 = b1 = 0, b3 = b0 = 0 or 1, b7-b4 = 0) to display " U ". That means all of the character codes (00) 16, (01) 16, (08) 16, and (09) 16 can display " U " character.
- Note6:** The bits 0-3 of the character code RAM is the character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.

7.13. Cursor/Blink Control Circuit

This circuit generates the cursor or blink in the cursor / blink control circuit. The cursor or the blink appears in the digit at the Display Data RAM Address defined in the Address Counter.

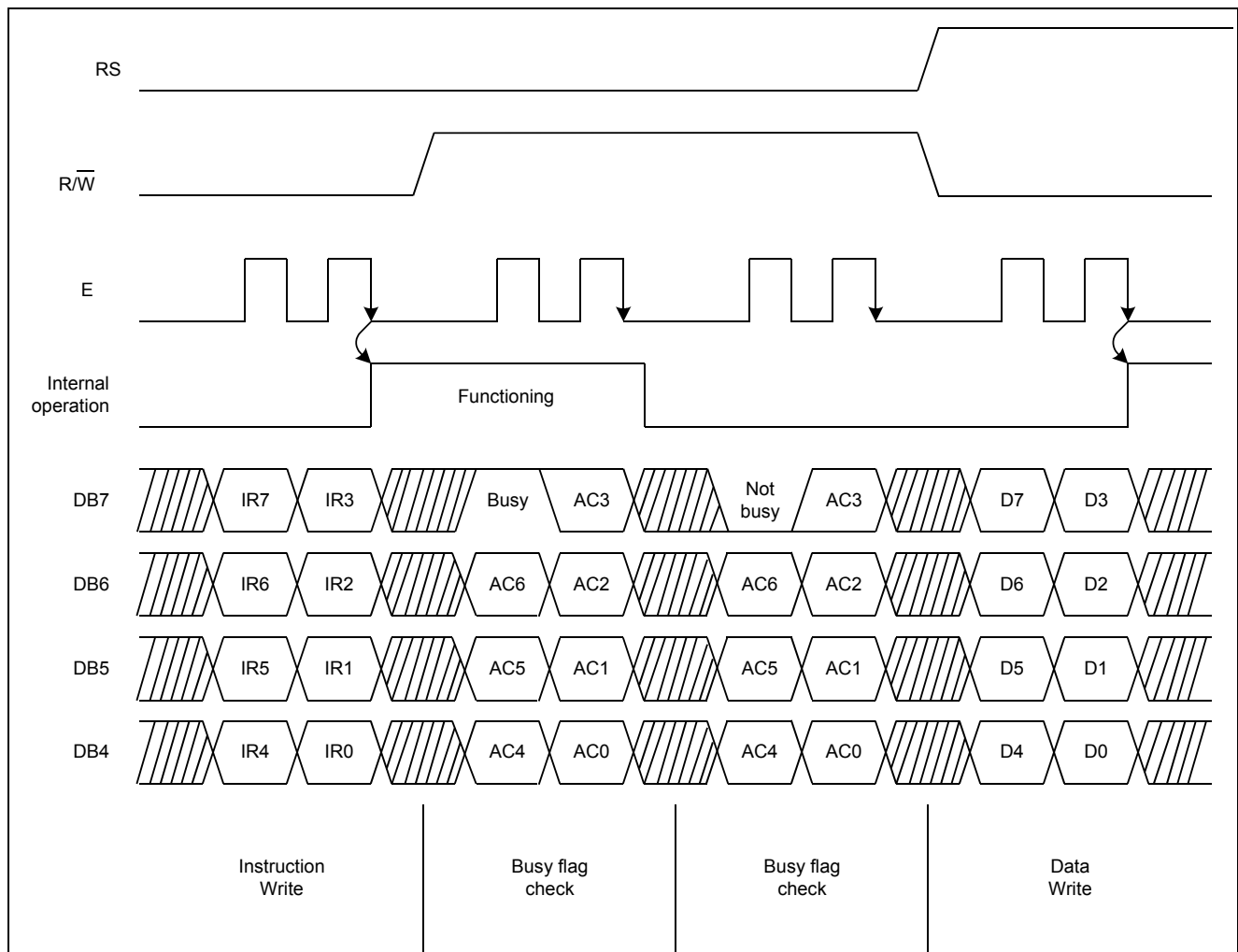
When the Address Counter is (07) 16, the cursor position is shown as belows:



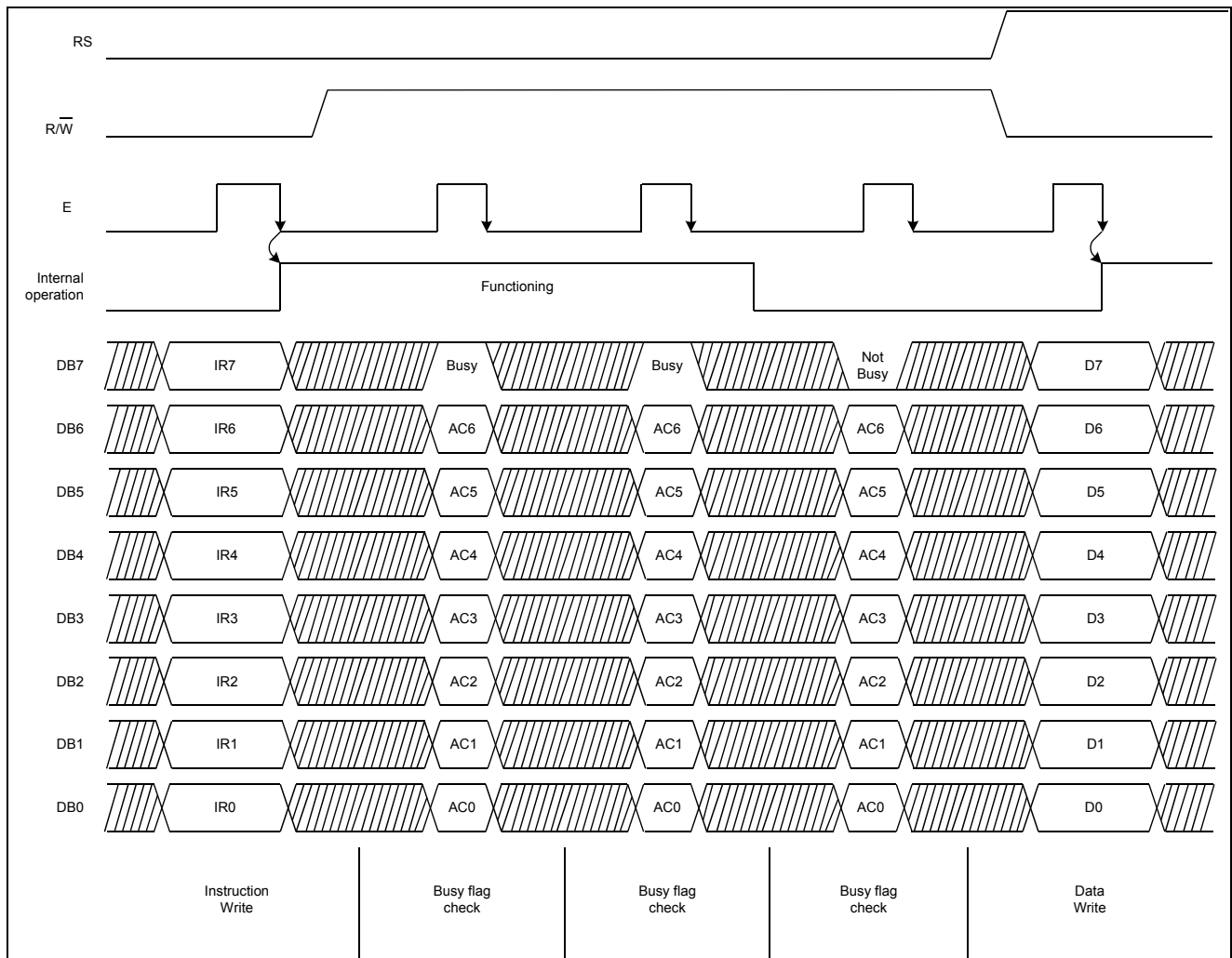
7.14. Interfacing to MPU

There are two types of data operations: 4-bit and 8-bit operations. Using 4-bit MPU, the interfacing 4-bit data is transferred by 4-busline (DB4 to DB7). Thus, DB0 to DB3 bus lines are not used. Using 4-bit MPU to interface 8-bit data requires two times transferring. First, the higher 4-bit data is transferred by

4-busline (for 8-bit operation, DB7 to DB4). Secondly, the lower 4-bit data is transferred by 4-busline (for 8-bit operation, DB3 to DB0). For 8-bit MPU, the 8-bit data is transferred by 8-buslines (DB0 to DB7).



Example of 4-bit Data Transfer Timing Sequence



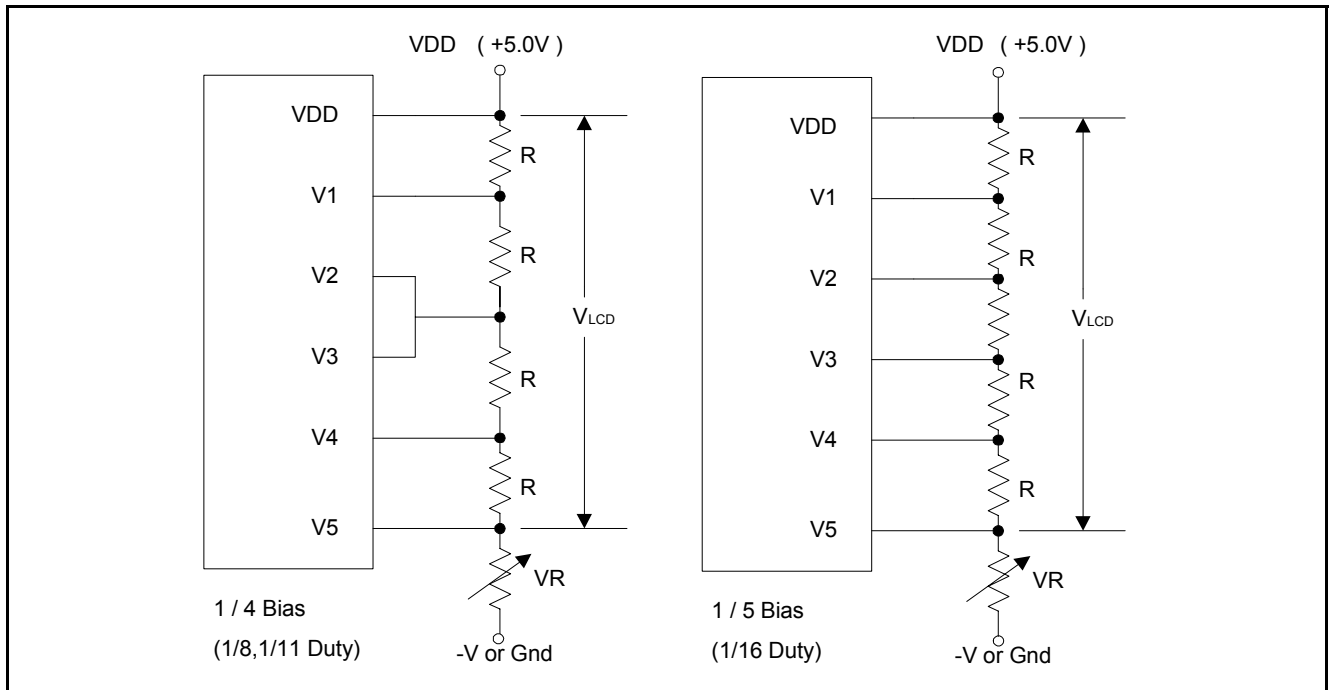
Example of 8-bit Data Transfer Timing Sequence

7.15. Supply Voltage for LCD Drive

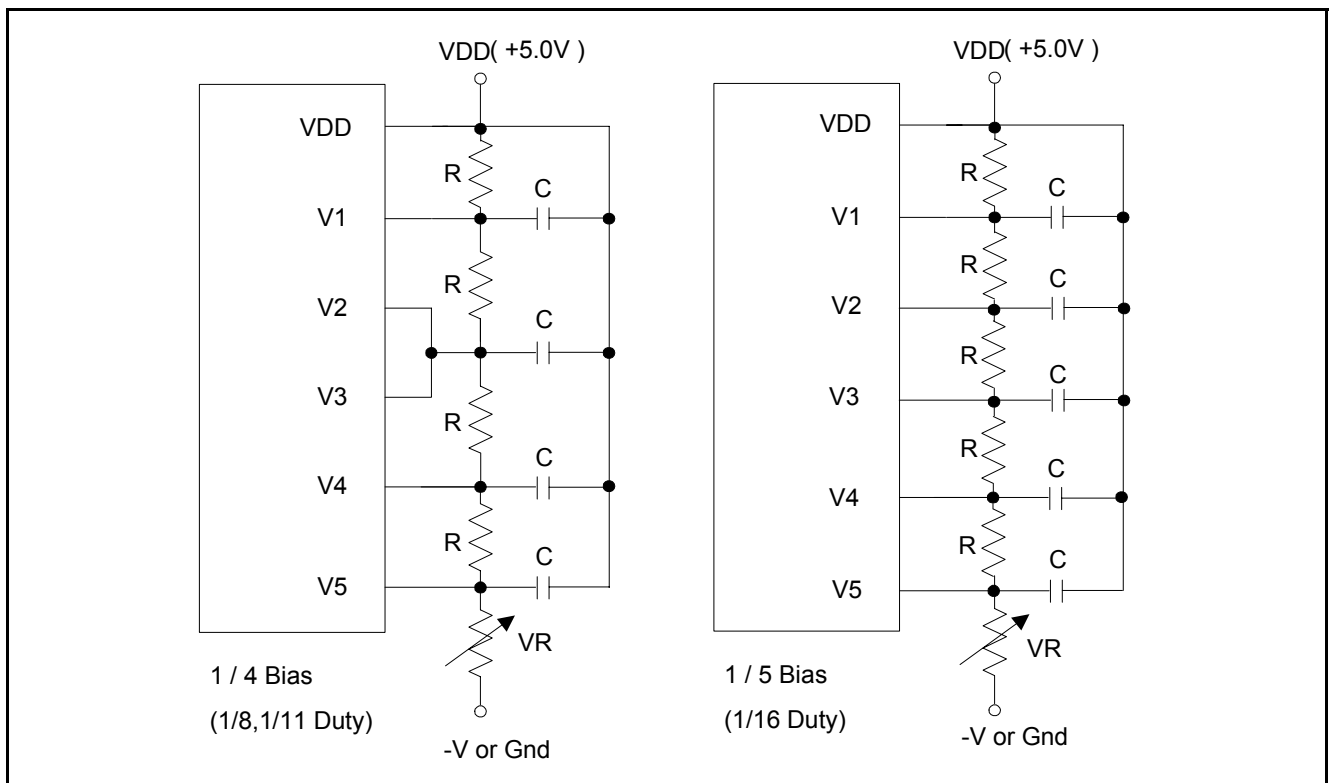
Different voltages can be supplied to SPLC780D1's pins (V5 - 1) for obtaining LCD drive-waveform. The relationships between bias, duty factor and supply voltages are shown as follows:

Supply Voltage	Duty Factor	1/8, 1/11	1/16
		1/4	1/5
V1		$VDD - 1/4 V_{LCD}$	$VDD - 1/5 V_{LCD}$
V2		$VDD - 1/2 V_{LCD}$	$VDD - 2/5 V_{LCD}$
V3		$VDD - 1/2 V_{LCD}$	$VDD - 3/5 V_{LCD}$
V4		$VDD - 3/4 V_{LCD}$	$VDD - 4/5 V_{LCD}$
V5		$VDD - V_{LCD}$	$VDD - V_{LCD}$

7.15.1. The power connections for LCD (1/4 Bias, 1/5 Bias) are shown belows:



The bypass-capacitor improves the LCD display quality.



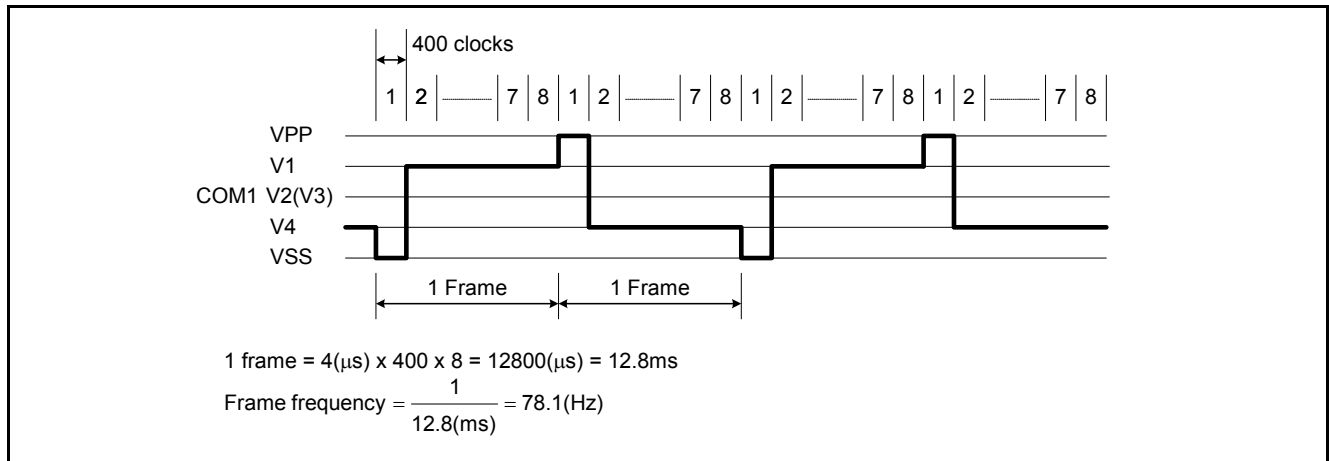
The bias voltage must have the following relations:

$$VDD > V1 > V2 \geq V3 > V4 > V5.$$

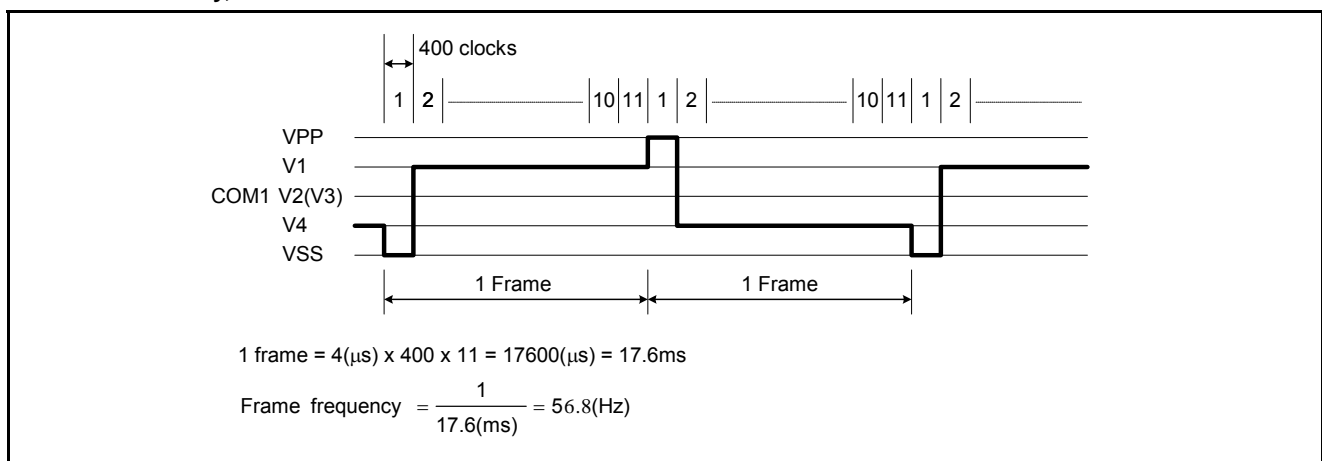
7.15.2. The relationship between LCD frame's frequency and oscillator's frequency.

(Assume the oscillation frequency is 250KHz, 1 clock cycle time = 4.0 μ s)

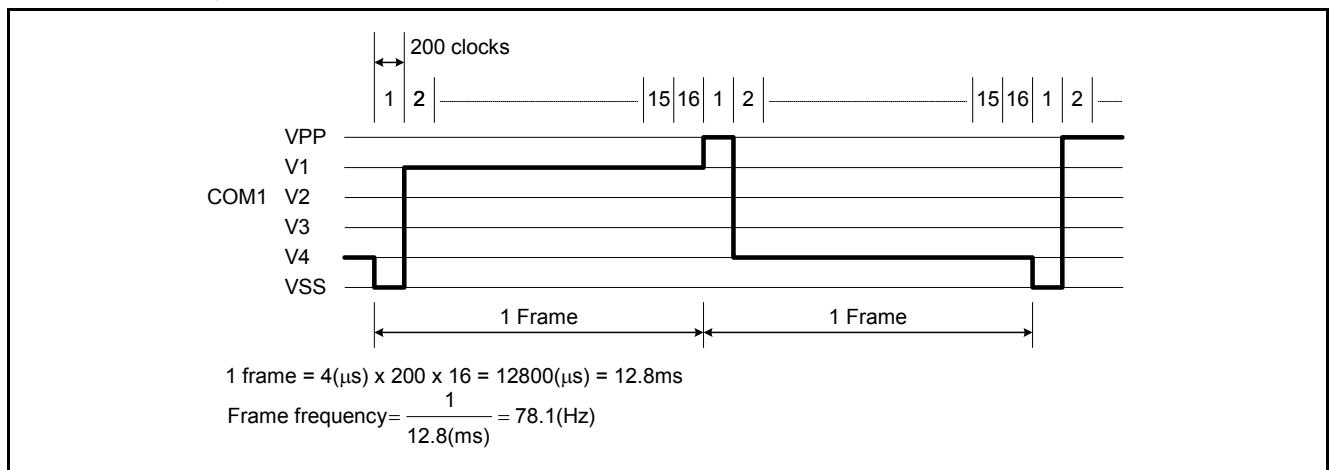
7.15.2.1. 1/8 Duty, TYPE-B waveform



7.15.2.2. 1/11 Duty, TYPE-B waveform



7.15.2.3. 1/16 Duty, TYPE-B waveform



7.16. REGISTER --- IR (Instruction Register) and DR (Data Register)

SPLC780D1 contains two 8-bit registers: Instruction Register (IR) and Data Register (DR). Using combinations of the RS pin and the R/W pin selects the IR and DR, see below:

RS	R/W	Operation
0	0	IR write (Display clear, etc.)
0	1	Read busy flag (DB7) and Address Counter (DB0 - DB6)
1	0	DR write (DR to Display data RAM or Character generator RAM)
1	1	DR read (Display data RAM or Character generator RAM to DR)

The IR can be written by MPU, but it cannot be read by MPU.

7.17. Busy Flag (BF)

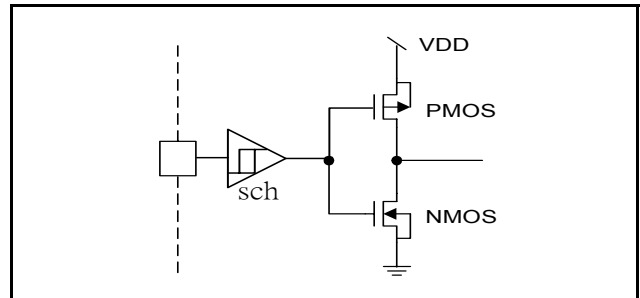
When RS = 0 and R/W = 1, the busy flag is output to DB7. As the busy flag = 1, SPLC780D1 is in busy state and does not accept any instruction until the busy flag = 0.

7.18. Address Counter (AC)

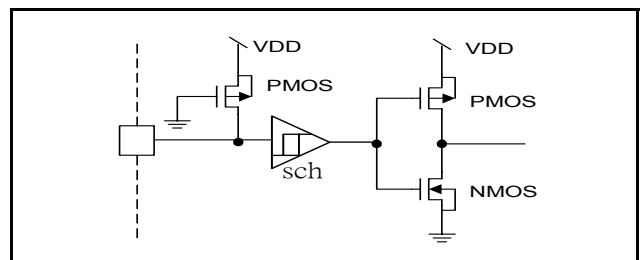
The Address Counter assigns addresses to Display Data RAM and Character Generator RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. After writing to/reading from Display Data RAM or Character Generator RAM, AC is automatically incremented by one (or decremented by one). The contents of AC are output to DB0 - DB6 when RS = 0 and R/W = 1.

7.19. I/O Port Configuration

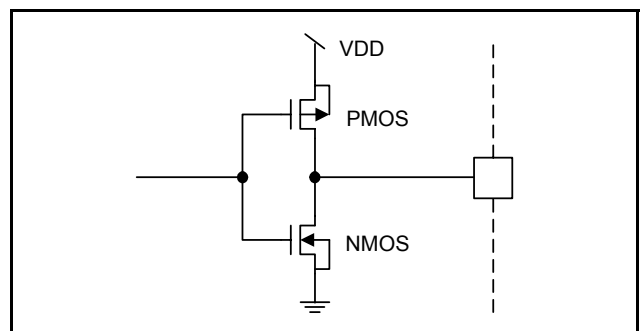
7.19.1. Input port: E



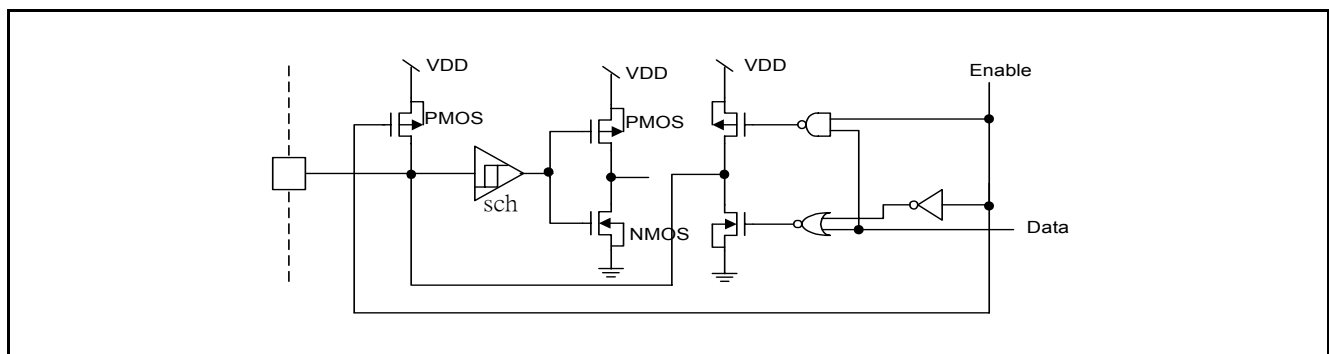
7.19.2. Input port: R/W, RS



7.19.3. Output port: CL1, CL2, M, D



7.19.4. Input / Output port: DB7 - DB0



8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD	-0.3V to +7.0V
Driver Supply Voltage	V _{LCD}	VDD - 10V to VDD + 0.3V
Input Voltage Range	V _{IN}	-0.3V to VDD + 0.3V
Operating Temperature	T _A	-30°C to +80°C
Storage Temperature	T _{STO}	-55°C to +125°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

8.2. DC Characteristics (VDD = 2.7V to 4.5V, T_A = 25°C)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I _{DD}	-	0.2	0.4	mA	External clock (Note)
Input High Voltage	V _{IH1}	0.7VDD	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V _{IL1}	-0.3	-	0.55	V	
Input High Voltage	V _{IH2}	0.7VDD	-	VDD	V	Pin OSC1
Input Low Voltage	V _{IL2}	-0.2	-	0.2VDD	V	
Input High Current	I _{IH}	-1.0	-	1.0	μA	Pins: (RS, R/W, DB0 - DB7) VDD = 3.0V
Input Low Current	I _{IL}	-10.0	-50	-120	μA	
Output High Voltage (TTL)	V _{OH1}	0.75VDD	-	-	V	I _{OH} = - 0.1mA Pins: DB0 - DB7
Output Low Voltage (TTL)	V _{OL1}	-	-	0.2VDD	V	I _{OL} = 0.1mA Pins: DB0 - DB7
Output High Voltage (CMOS)	V _{OH2}	0.8VDD	-	-	V	I _{OH} = - 40μA, Pins: CL1, CL2, M, D
Output Low Voltage (CMOS)	V _{OL2}	-	-	0.2VDD	V	I _{OL} = 40μA, Pins: CL1, CL2, M, D
Driver ON Resistance (COM)	R _{COM}	-	-	20	KΩ	I _O = ±50μA, V _{LCD} = 4.0V Pins: COM1 - COM16
Driver ON Resistance (SEG)	R _{SEG}	-	-	30	KΩ	I _O = ±50μA, V _{LCD} = 4.0V Pins: SEG1 - SEG40
LCD Voltage	V _{LCD}	3.0	-	8.0	V	VDD-V5, 1/4 bias or 1/5 bias

Note: F_{osc} = 250KHz, VDD = 3.0V, pin E = "L", RS, R/W, DB0 - DB7 are open, all outputs are no loads.

8.3. AC Characteristics (VDD = 2.7V to 4.5V, T_A = 25°C)

8.3.1. Internal clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F _{OSC1}	190	270 350		KHz	VDD = 3.0V, Rf = 75KΩ±2%

8.3.2. External clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
External Frequency	F _{OSC2}	125	250	350	KHz	
Duty Cycle		45	50	55	%	
Rise/Fall Time	t _r , t _f	-	-	0.2	μs	

8.3.3. Write mode (Writing data from MPU to SPLC780D1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t _C	1000	-	-	ns	Pin E
E Pulse Width	t _{PW}	450	-	-	ns	Pin E
E Rise/Fall Time	t _R , t _F	-	-	25	ns	Pin E
Address Setup Time	t _{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t _{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t _{SP2}	195	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t _{HD2}	10	-	-	ns	Pins: DB0 - DB7

8.3.4. Read mode (Reading data from SPLC780D1 to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t _C	1000	-	-	ns	Pin E
E Pulse Width	t _W	450	-	-	ns	Pin E
E Rise/Fall Time	t _R , t _F	-	-	25	ns	Pin E
Address Setup Time	t _{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t _{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t _D	-	-	360	ns	Pins: DB0 - DB7
Data hold time	t _{HD2}	5.0	-	-	ns	Pin DB0 - DB7

8.4. DC Characteristics (VDD = 4.5V to 5.5V, TA = 25°C)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I _{DD}	-	0.55	0.8	mA	External clock (Note)
Input High Voltage	V _{IH1}	2.5	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7) VDD=5V
Input Low Voltage	V _{IL1}	-0.3	-	0.6	V	
Input High Voltage	V _{IH2}	VDD-1	-	VDD	V	Pin OSC1
Input Low Voltage	V _{IL2}	-0.2	-	1.0	V	Pin OSC1
Input High Current	I _{IH}	-2.0	-	2.0	μA	Pins: (RS, R/W, DB0 - DB7) VDD = 5.0V
Input Low Current	I _{IL}	-20	-125	-250	μA	
Output High Voltage (TTL)	V _{OH1}	2.4	-	VDD	V	I _{OH} = - 0.1mA Pins: DB0 - DB7
Output Low Voltage (TTL)	V _{OL1}	-	-	0.4	V	I _{OL} = 0.1mA Pins: DB0 - DB7
Output High Voltage (CMOS)	V _{OH2}	0.9VDD	-	VDD	V	I _{OH} = - 40μA, Pins: CL1, CL2, M, D
Output Low Voltage (CMOS)	V _{OL2}	-	-	0.1VDD	V	I _{OL} = 40μA, Pins: CL1, CL2, M, D
Driver ON Resistance (COM)	R _{COM}	-	-	20	KΩ	I _O = ±50μA, V _{LCD} = 4.0V Pins: COM1 - COM16
Driver ON Resistance (SEG)	R _{SEG}	-	-	30	KΩ	I _O = ±50μA, V _{LCD} = 4.0V Pins: SEG1 - SEG40
LCD Voltage	V _{LCD}	3.0	-	8	V	VDD-V5, 1/4 bias or 1/5 bias

Note: F_{osc} = 250KHz, VDD = 5.0V, pin E = "L", RS, R/W, DB0 - DB7 are open, all outputs are no loads.

8.5. AC Characteristics (VDD = 4.5V to 5.5V, TA = 25°C)

8.5.1. Internal clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F _{OSC1}	190	270	350	KHz	VDD = 5.0V, Rf = 91KΩ±2%

8.5.2. External clock operation

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
External Frequency	F _{OSC2}	125	250	350	KHz	
Duty Cycle		45	50	55	%	
Rise/Fall Time	t _r , t _f	-	-	0.2	μs	

8.5.3. Write mode (Writing Data from MPU to SPLC780D1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	400	-	-	ns	Pin E
E Pulse Width	t_{PW}	150	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	30	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	40	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

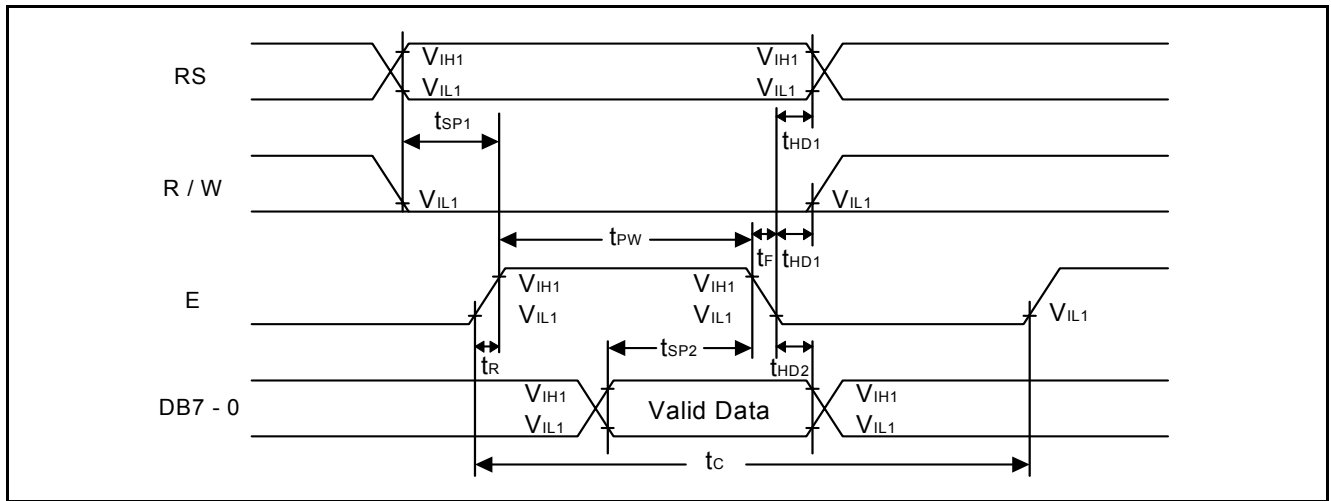
8.5.4. Read mode (Reading Data from SPLC780D1 to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	400	-	-	ns	Pin E
E Pulse Width	t_W	150	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	30	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	100	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pin DB0 - DB7

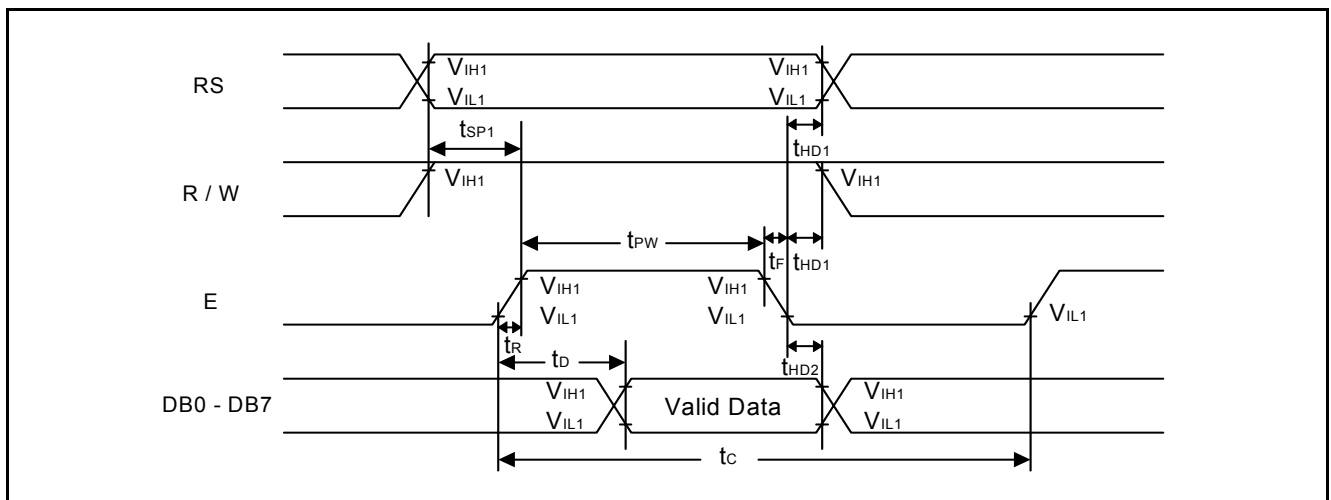
8.5.5. Interface mode with LCD Driver (SPLC100B1)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Clock pulse width high	t_{PWH}	800	-	-	ns	Pins: CL1, CL2
Clock pulse width low	t_{PWL}	800	-	-	ns	Pins: CL1, CL2
Clock setup time	t_{CSP}	500	-	-	ns	Pins: CL1, CL2
Data setup time	t_{DSP}	300	-	-	ns	Pins: D
Data hold time	t_{HD}	300	-	-	ns	Pins: D
M delay time	t_D	-1000	-	1000	ns	Pins: M

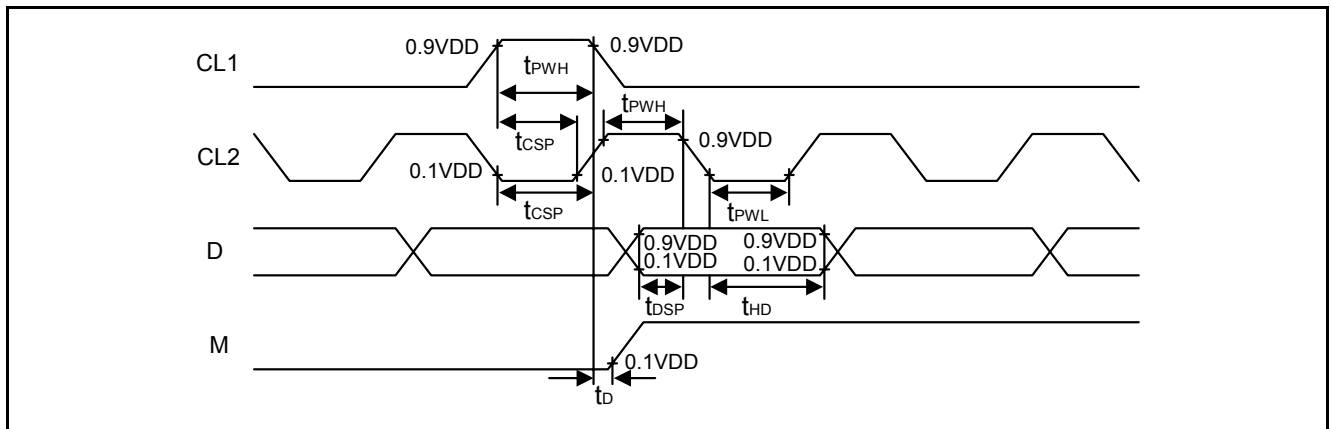
8.5.6. Write mode timing diagram (Writing Data from MPU to SPLC780D1)



8.5.7. Read mode timing diagram (Reading Data from SPLC780D1 to MPU)



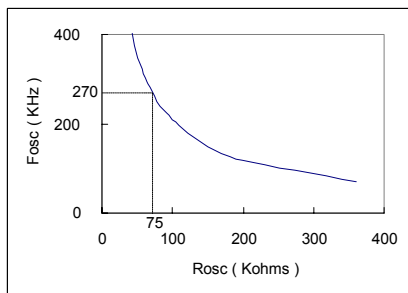
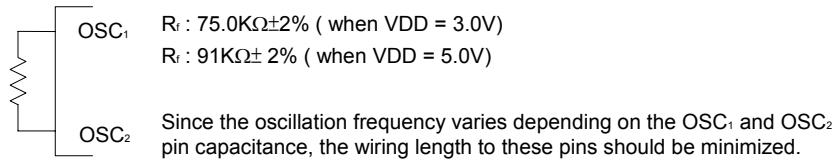
8.5.8. Interface mode with SPLC100B1 timing diagram



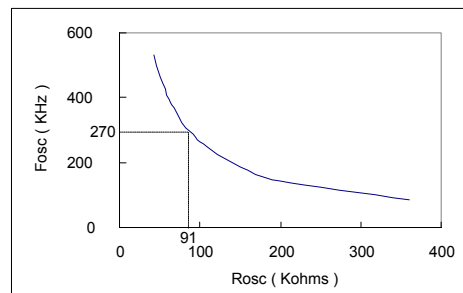
9. APPLICATION CIRCUITS

9.1. R-Oscillator

The oscillation resistor R_f is used only for the internal oscillator operation mode.



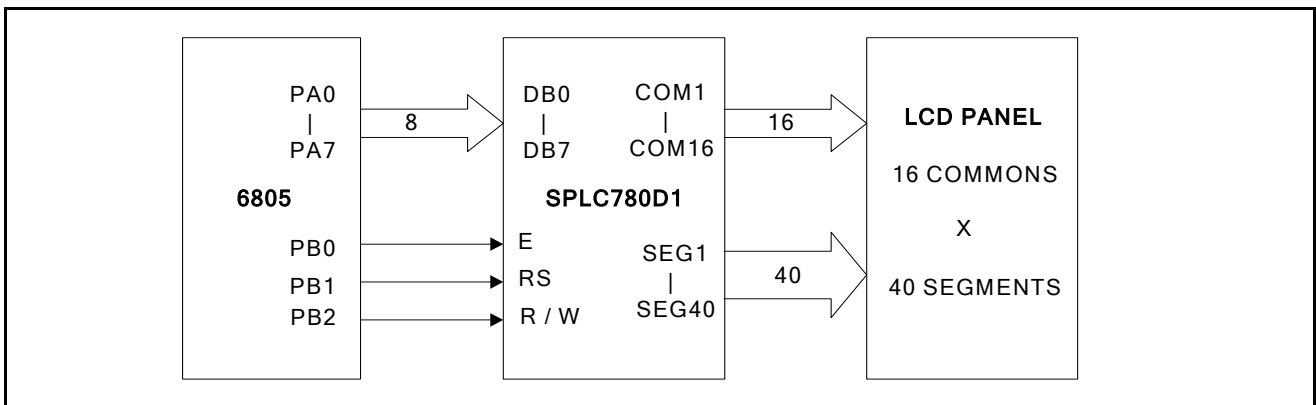
VDD = 3.0V



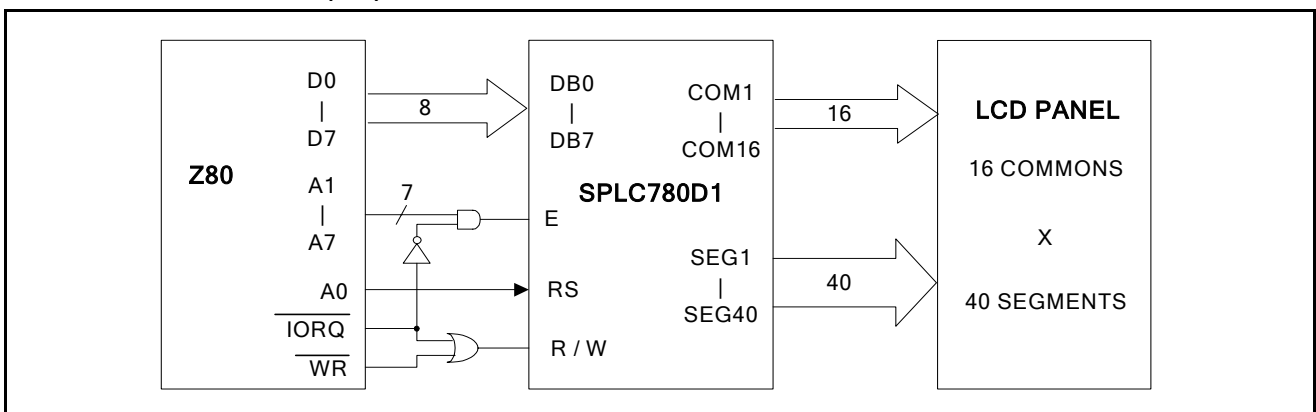
VDD = 5.0V

9.2. Interface to MPU

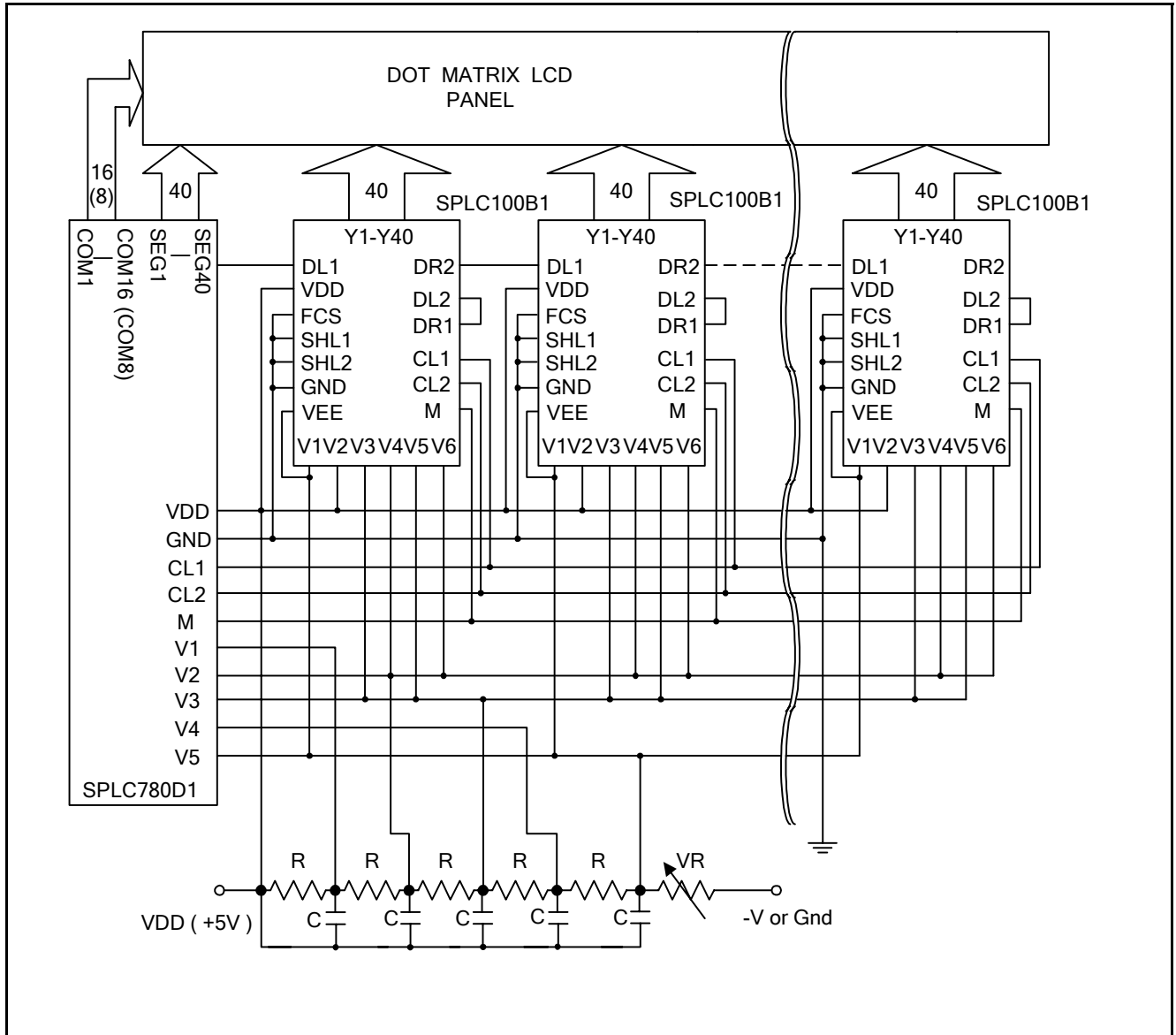
9.2.1. Interface to 8-bit MPU (6805)



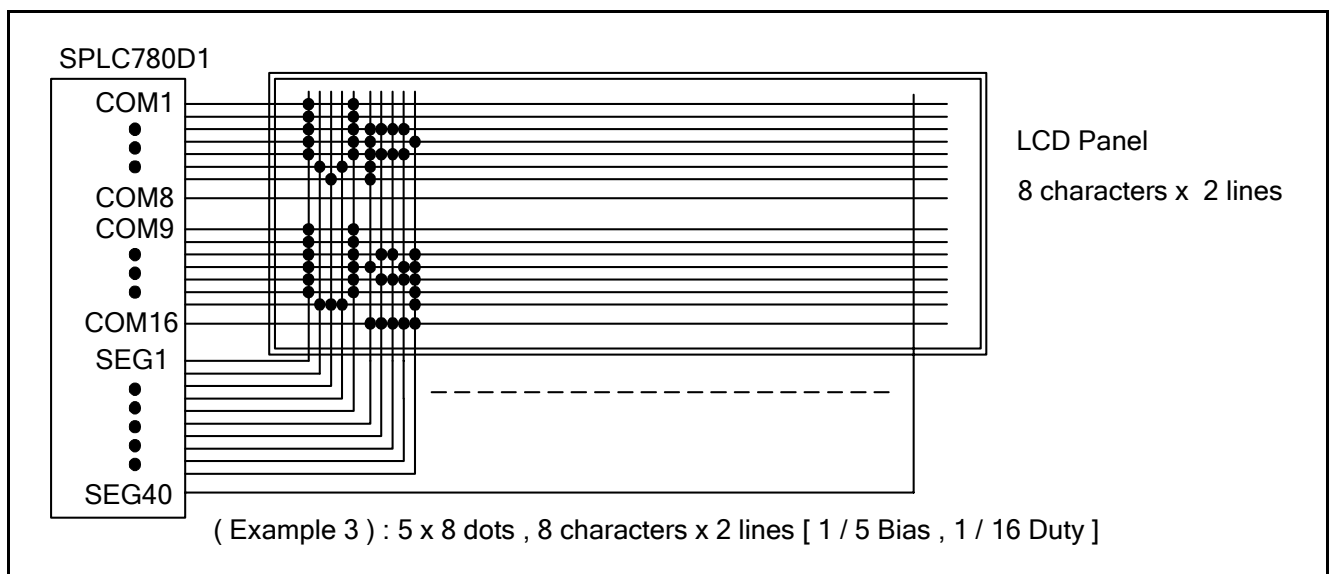
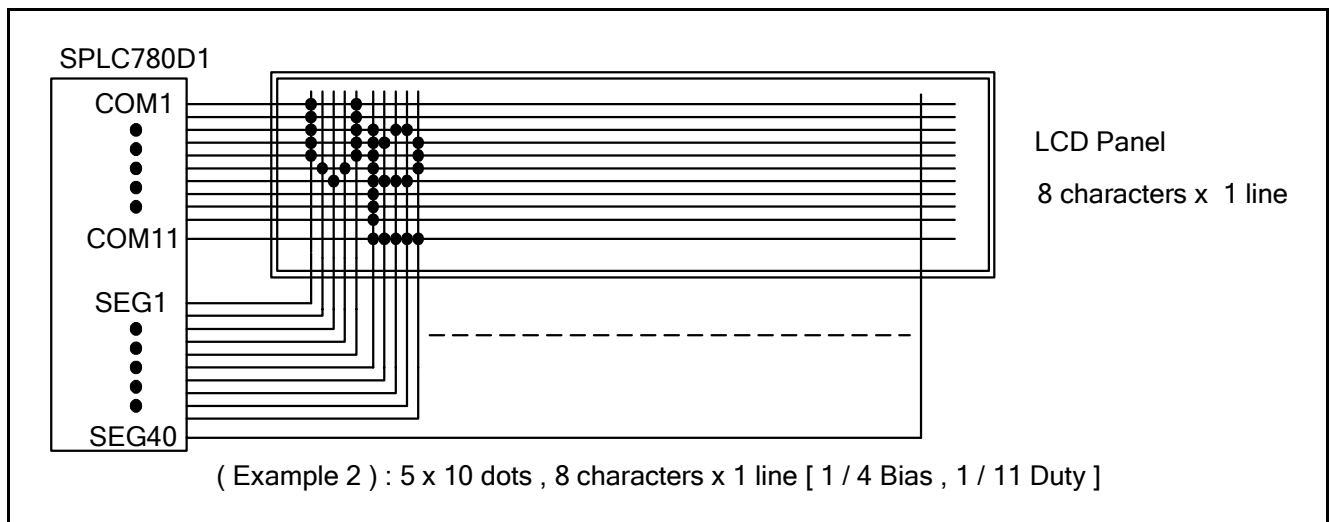
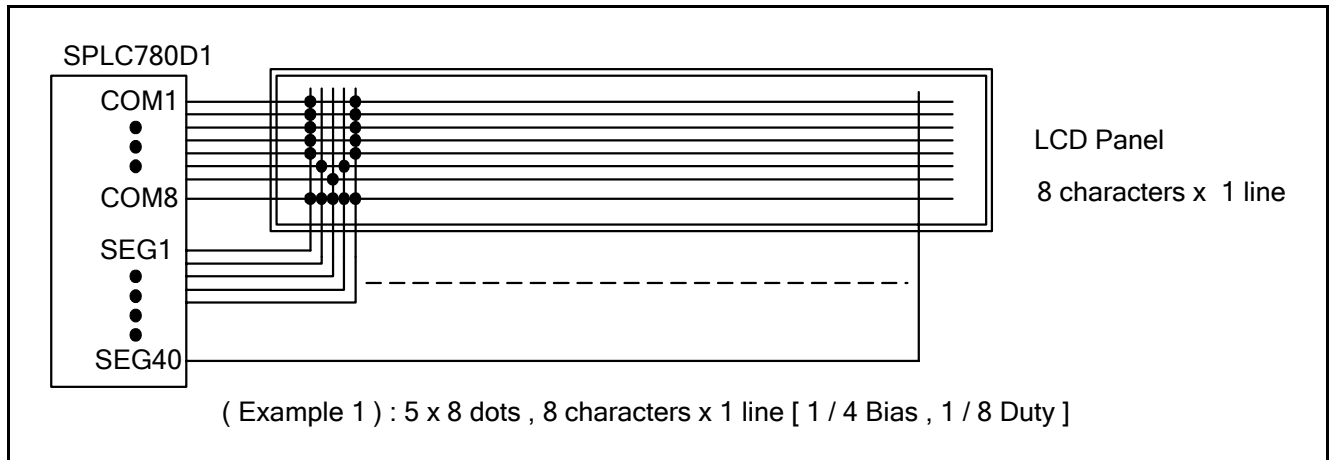
9.2.2. Interface to 8-bit MPU (Z80)

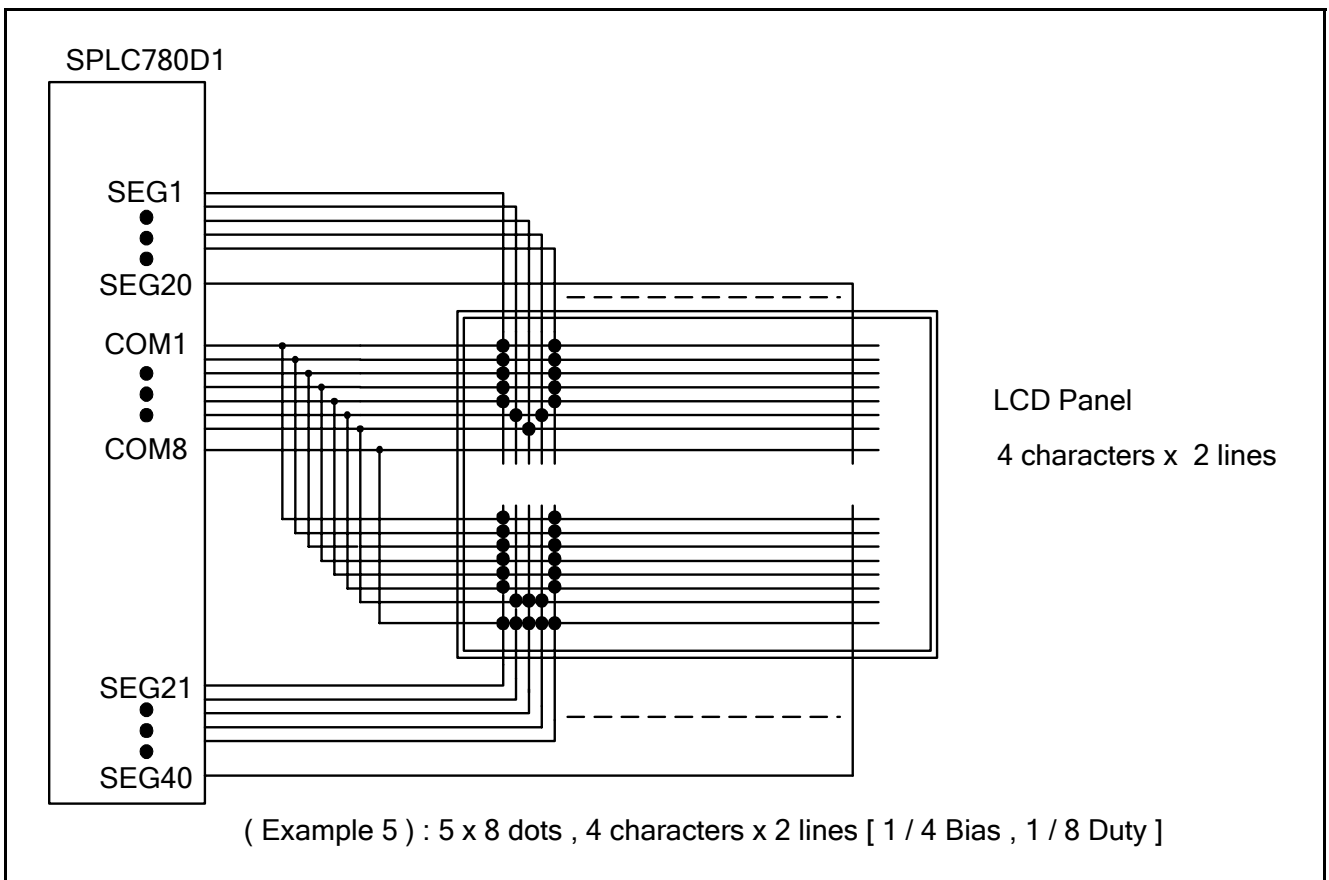
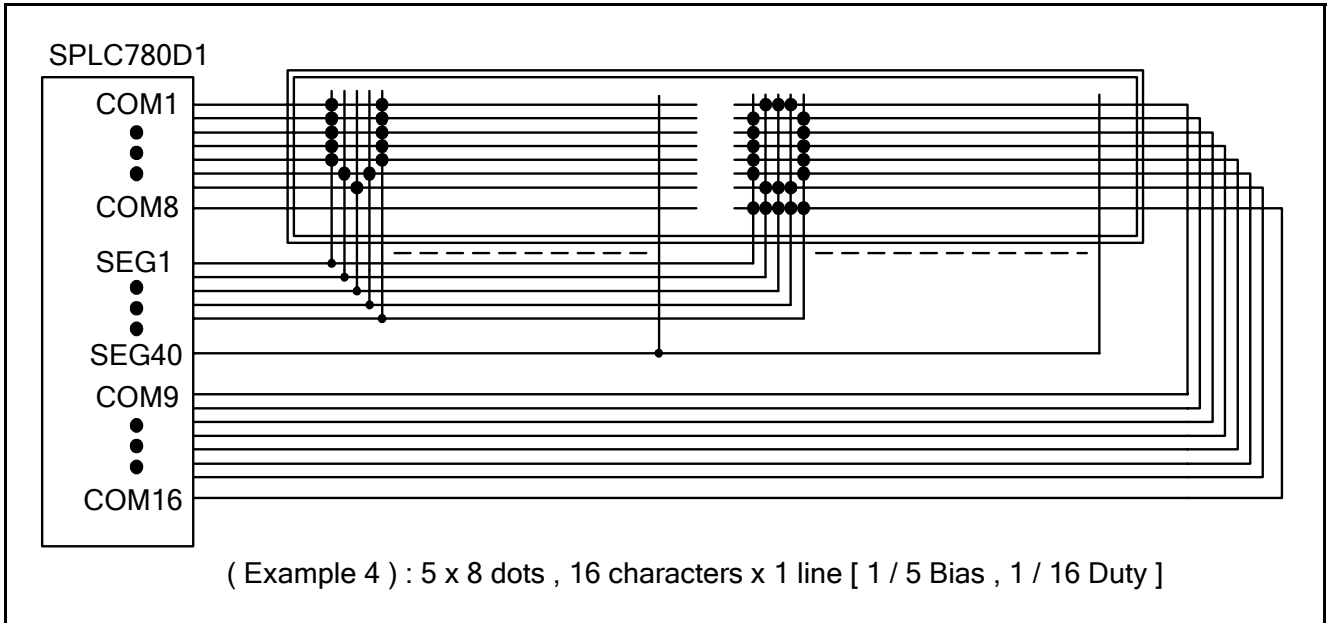


9.3. SPLC780D1 Application Circuit



9.4. Applications for LCD





10. CHARACTER GENERATOR ROM

10.1. SPLC780D1 – 001A

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL				0	1	2	3	4	5	6	7	8	9	A	B	C
LLLH		!	①	②	③	④	⑤	⑥		。	ア	チ	ウ	⑧	⑨	
LLHL			"	2	R	b	r			「	イ	ウ	×	⑩	⑪	
LLHH			#	3	C	S	c	s		」	ウ	テ	モ	⑫	⑬	
LHLL			※	4	D	T	d	t		、	エ	ト	ホ	⑭	⑮	
LHLH			ズ	5	E	U	e	u		・	オ	大	ユ	⑯	⑰	
LHHL			＆	6	F	U	f	u		ヲ	カ	ニ	ヨ	⑱	⑲	
LHHH			〒	7	G	W	g	w		ア	キ	又	ラ	㉑	㉒	
HLLL			＜	8	H	X	h	x		イ	夕	利	ト	㉓	㉔	
HLLH			＞	9	I	Y	i	y		ウ	ケ	ル	”	㉕	㉖	
HLHL			*	※	J	Z	j	z		エ	コ	ハ	レ	㉗	㉘	
HLHH			+	※	K	L	k	l		オ	カ	ヒ	ロ	°	㉙	
HHLL			,	＜	L	¥	l	¥		ホ	シ	フ	ワ	※	㉚	
HHLH			—	=	M	J	m	j		ユ	又	ハ	シ	㉛	㉜	
HHHL			・	＞	N	^	n	^		ヨ	セ	ホ	”	㉝	㉞	
HHHH			/	？	O	L	o	←		ウ	ウ	ア	”	㉟	㊀	

10.2. SPLC780D1 – 002A

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL				0	1	2	3	4	5	6	7	8	9	A	B	C
LLLH			!	1	2	3	4	5	6	7	8	9	A	B	C	D
LLHL			"	2	3	4	5	6	7	8	9	A	B	C	D	E
LLHH			#	3	4	5	6	7	8	9	A	B	C	D	E	F
LHLL			\$	4	5	6	7	8	9	A	B	C	D	E	F	G
LHLH			%	5	6	7	8	9	A	B	C	D	E	F	G	H
LHHL			&	6	7	8	9	A	B	C	D	E	F	G	H	I
LHHH			'	7	8	9	A	B	C	D	E	F	G	H	I	J
HLLL			(8	9	A	B	C	D	E	F	G	H	I	J	K
HLLH)	9	A	B	C	D	E	F	G	H	I	J	K	L
HLHL			*	A	B	C	D	E	F	G	H	I	J	K	L	M
HLHH			+	B	C	D	E	F	G	H	I	J	K	L	M	N
HHLL			,	C	D	E	F	G	H	I	J	K	L	M	N	O
HHLH			-	D	E	F	G	H	I	J	K	L	M	N	O	P
HHHL			.	E	F	G	H	I	J	K	L	M	N	O	P	Q
HHHH			/	F	G	H	I	J	K	L	M	N	O	P	Q	R

10.3. SPLC780D1 – 003A

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
	LLLL	士	日	月	年	月	日	年	月	日	年	月	日	年	月	日
LLLH	三	!	1	A	Q	9	0	2	”	J	十	Y	0			
LLHL	?”	2	B	R	b	r	e	s	*	∞	∞	∞	∞	∞	∞	∞
LLHH	△	#	3	C	S	c	s	∞	∞	∞	∞	∞	∞	∞	∞	∞
LHLL	Y	4	D	T	d	t	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
LHLH	U	5	E	U	e	u	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
LHHL	Y	6	F	U	f	u	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
LHHH	U	7	G	W	w	u	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
HLLL	Y	0	B	H	h	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
HLLH	U	9	I	Y	y	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
HLHL	∞	∞	J	Z	z	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
HLHH	J	+	K	K	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
HHLL	=	<	L	L	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
HHLH	∞	—	=	M	m	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
HHHL	∞	.	>	N	n	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞
HHHH	∞	/	?	0	0	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞	∞

10.4. SPLC780D1 – 011A

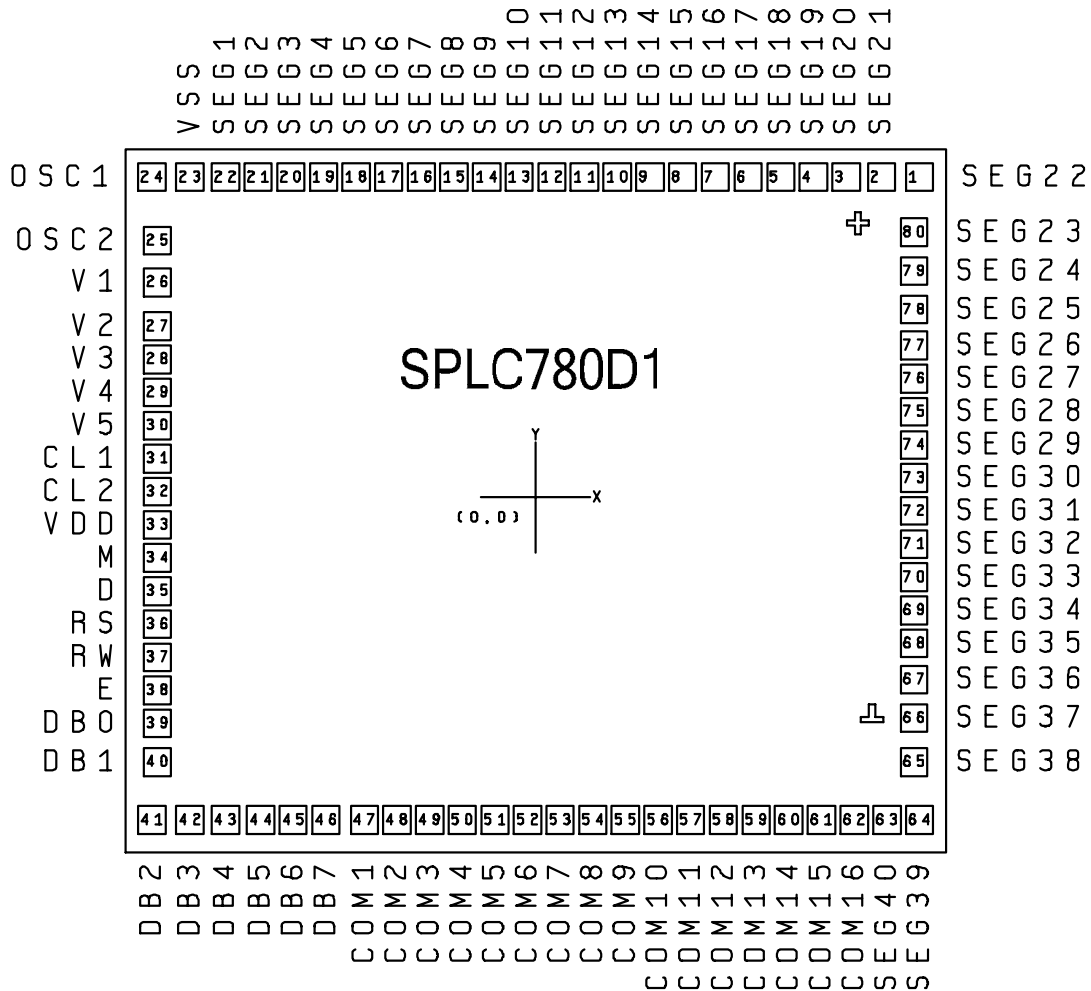
Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL				0	1	2	3	4	5	6	7	8	9	A	B	C
LLLH			D	E	F	G	H	I	J	K	L	M	N	O	P	Q
LLHL			R	S	T	U	V	W	X	Y	Z	[]	^	_	0
LLHH			1	2	3	4	5	6	7	8	9	A	B	C	D	E
LHLL			F	G	H	I	J	K	L	M	N	O	P	Q	R	S
LHLH			T	U	V	W	X	Y	Z	[]	^	_	0	1	2
LHHL			3	4	5	6	7	8	9	A	B	C	D	E	F	G
LHHH			H	I	J	K	L	M	N	O	P	Q	R	S	T	U
HLLL			V	W	X	Y	Z	[]	^	_	0	1	2	3	4
HLLH			5	6	7	8	9	A	B	C	D	E	F	G	H	I
HLHL			J	K	L	M	N	O	P	Q	R	S	T	U	V	W
HLHH			X	Y	Z	[]	^	_	0	1	2	3	4	5	6
HHLL			7	8	9	A	B	C	D	E	F	G	H	I	J	K
HHLH			L	M	N	O	P	Q	R	S	T	U	V	W	X	Y
HHHL			Z	[]	^	_	0	1	2	3	4	5	6	7	8
HHHH			9	A	B	C	D	E	F	G	H	I	J	K	L	M

10.5. SPLC780D1 – 021A

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
LLLH	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V
LLHL	W	X	Y	Z	[\]	^	_	`	{		}	~	?	@
LLHH	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P
LHLL	Q	R	S	T	U	V	W	X	Y	Z	[\]	^	_	`
LHLH	{		}	~	?	@	A	B	C	D	E	F	G	H	I	J
LHHL	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
LHHH	[\]	^	_	`	{		}	~	?	@	A	B	C	D
HLLL	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
HLLH	U	V	W	X	Y	Z	[\]	^	_	`	{		}	~
HLHL	{		}	~	?	@	A	B	C	D	E	F	G	H	I	J
HLHH	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
HHLL	[\]	^	_	`	{		}	~	?	@	A	B	C	D
HHLH	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
HHHL	U	V	W	X	Y	Z	[\]	^	_	`	{		}	~
HHHH	{		}	~	?	@	A	B	C	D	E	F	G	H	I	J

11. PACKAGE/PAD LOCATIONS

11.1. PAD Assignment



Chip Size: 2860 μ m x 2450 μ m

PAD Size: 90 μ m x 90 μ m

This IC substrate should be connected to VDD

Note1: Chip size included scribe line.

Note2: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

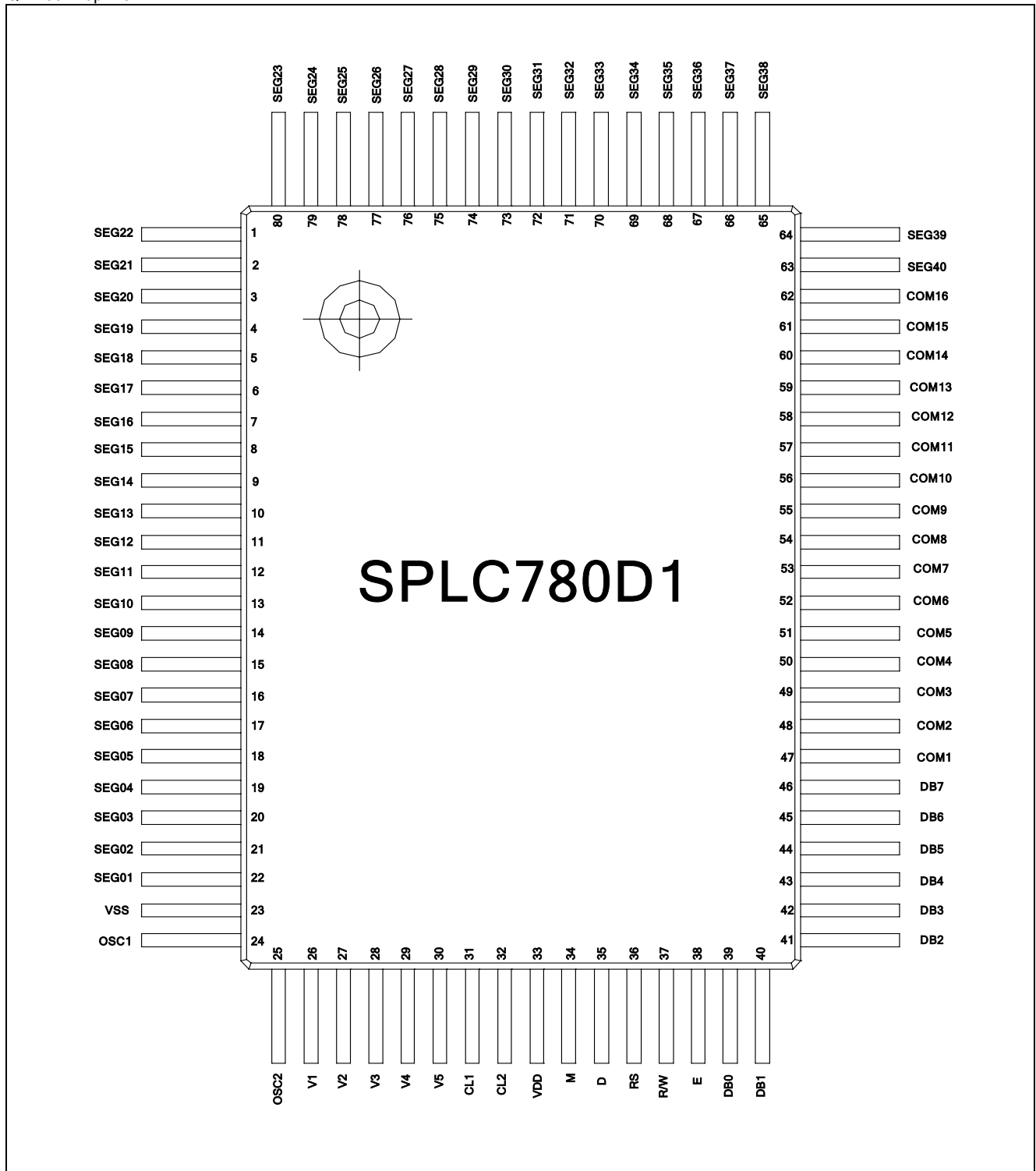
Note3: The 0.1 μ F capacitor between VDD and VSS should be placed to IC as close as possible.

11.2. PAD Locations

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	SEG22	1295.0	1058.5	41	DB2	-1295.0	-1058.5
2	SEG21	1175.0	1058.5	42	DB3	-1175.0	-1058.5
3	SEG20	1055.0	1058.5	43	DB4	-1055.0	-1058.5
4	SEG19	940.0	1058.5	44	DB5	-940.0	-1058.5
5	SEG18	825.0	1058.5	45	DB6	-825.0	-1058.5
6	SEG17	715.0	1058.5	46	DB7	-715.0	-1058.5
7	SEG16	605.0	1058.5	47	COM1	-605.0	-1058.5
8	SEG15	495.0	1058.5	48	COM2	-495.0	-1058.5
9	SEG14	385.0	1058.5	49	COM3	-385.0	-1058.5
10	SEG13	275.0	1058.5	50	COM4	-275.0	-1058.5
11	SEG12	165.0	1058.5	51	COM5	-165.0	-1058.5
12	SEG11	55.0	1058.5	52	COM6	-55.0	-1058.5
13	SEG10	-55.0	1058.5	53	COM7	55.0	-1058.5
14	SEG9	-165.0	1058.5	54	COM8	165.0	-1058.5
15	SEG8	-275.0	1058.5	55	COM9	275.0	-1058.5
16	SEG7	-385.0	1058.5	56	COM10	385.0	-1058.5
17	SEG6	-495.0	1058.5	57	COM11	495.0	-1058.5
18	SEG5	-605.0	1058.5	58	COM12	605.0	-1058.5
19	SEG4	-715.0	1058.5	59	COM13	715.0	-1058.5
20	SEG3	-825.0	1058.5	60	COM14	825.0	-1058.5
21	SEG2	-940.0	1058.5	61	COM15	940.0	-1058.5
22	SEG1	-1055.0	1058.5	62	COM16	1055.0	-1058.5
23	VSS	-1175.0	1058.5	63	SEG40	1175.0	-1058.5
24	OSC1	-1295.0	1058.5	64	SEG39	1295.0	-1058.5
25	OSC2	-1268.0	853.7	65	SEG38	1259.8	-856.3
26	V1	-1259.8	733.7	66	SEG37	1259.8	-736.3
27	V2	-1259.8	613.7	67	SEG36	1259.8	-616.3
28	V3	-1259.8	498.7	68	SEG35	1259.8	-501.3
29	V4	-1259.8	383.7	69	SEG34	1259.8	-386.3
30	V5	-1259.8	273.7	70	SEG33	1259.8	-276.3
31	CL1	-1259.8	163.7	71	SEG32	1259.8	-166.3
32	CL2	-1259.8	53.7	72	SEG31	1259.8	-56.3
33	VDD	-1259.8	-56.3	73	SEG30	1259.8	53.7
34	M	-1259.8	-166.3	74	SEG29	1259.8	163.7
35	D	-1259.8	-276.3	75	SEG28	1259.8	273.7
36	RS	-1259.8	-386.3	76	SEG27	1259.8	383.7
37	R/W	-1259.8	-501.3	77	SEG26	1259.8	498.7
38	E	-1259.8	-616.3	78	SEG25	1259.8	613.7
39	DB0	-1259.8	-736.3	79	SEG24	1259.8	733.7
40	DB1	-1259.8	-856.3	80	SEG23	1259.8	853.7

11.3. PIN Assignment

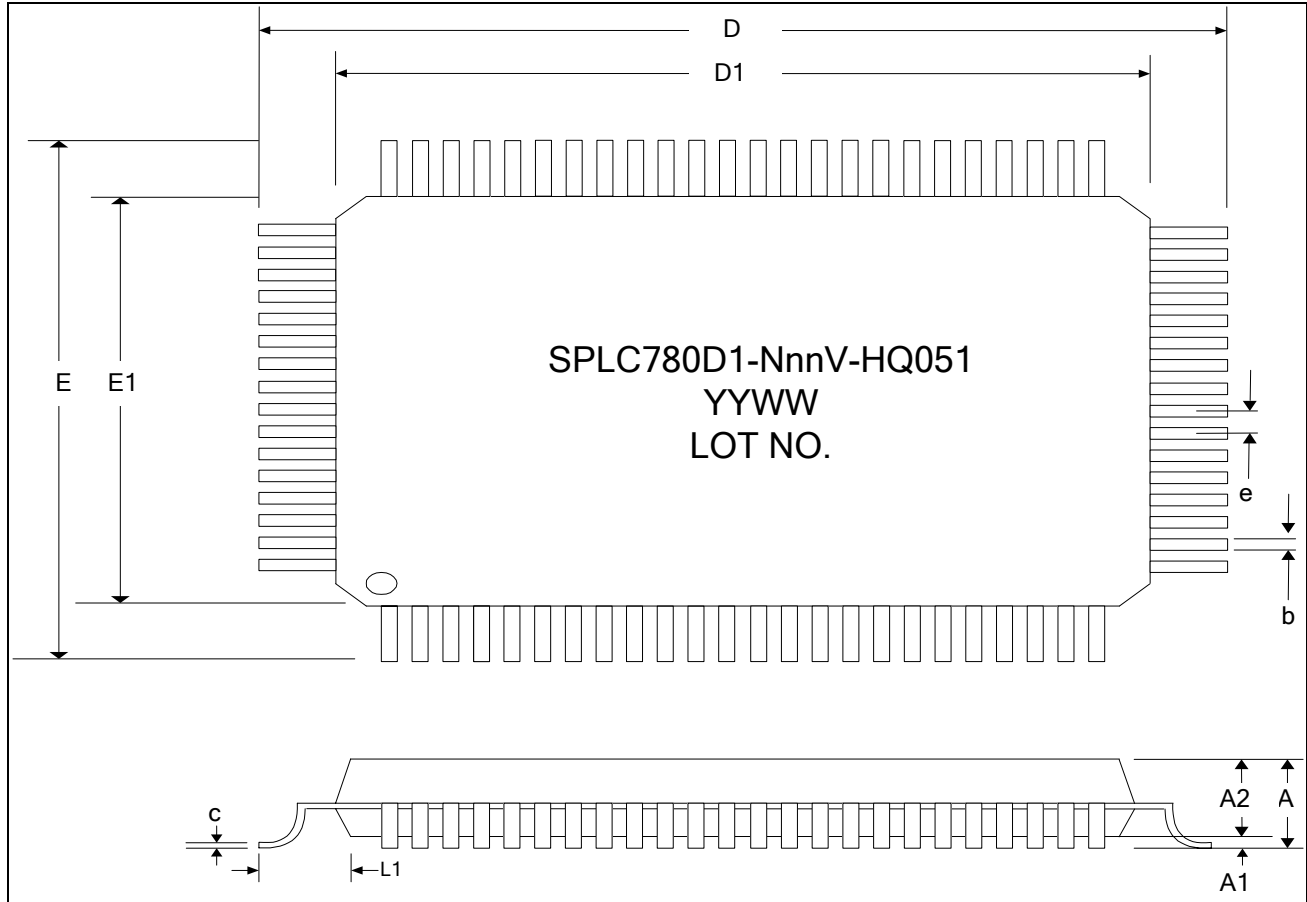
QFP 80L Top View



11.4. Package Information (SPLC780D1-NnnV-HQ051)

QFP 80L Outline Dimensions

Unit: Millimeter



Symbol	Min.	Nom.	Max.	Unit
D		23.20 REF		Millimeter
D1		20.00 REF		Millimeter
E		17.20 REF		Millimeter
E1		14.00 REF		Millimeter
e		0.80 REF		Millimeter
b	0.30	0.35	0.45	Millimeter
A	-	-	3.40	Millimeter
A1	0.25	-	-	Millimeter
A2	2.50	2.72	2.90	Millimeter
c	0.11	0.15	0.23	Millimeter
L1		1.60 REF		Millimeter

12. LEAD FRAME PACKAGE PCB DESIGN AND MANUFACTURING GUIDELINES

12.1. Purpose

The purpose of this specification is to identify plastic surface mount devices (SMDs) those are sensitive to moisture-induced stress, so that they can be properly design PCB and assembly packaged, stored and handled to avoid s ubsequent mechanical damage during the assembly solder reflow attachment and /or repair operation.

12.2. Scope

12.2.1. PCB layout guideline

12.2.2. PCB process

12.2.3. Storage Condition and Period for Package

12.2.4. Recommended SMT Temperature Profile

12.3. Noun definition

12.3.1. NSMD: Non Solder Mask Defined

12.3.2. SMD: Solder Mask Defined

12.3.3. CSP: Chip scale Package

12.3.4. PCB :Printed Circuit Board

12.4. Responsibility unity:

ORISETECH Quality Assurance unity

12.5. Contents

12.5.1. Applicable documents

IPC-SM-782: Surface Mount Design & Land Pattern Standard

IPC-7351 Generic Requirements for Surface Mount Design and Land Pattern Standard.

IPC-7525: Stencil Design Guidelines

J-STD-020: IPC/JEDEC Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Device

IPC JEDEC: J-STD-033A Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

IPC-HDBK-001: Handbook & Guide to the Requirements of Soldered Electronic Assemblies with Amendment 1

IPC -6016: Qualification & Performance Specification for High Density Interconnect (HDI) Layers or Boards

IPC-STD-003: Solderability Tests for Printed Boards

JESD22-B111: Board Level Drop Test of Components for Handheld Electronic Products

JESD22-B110: Subassembly Mechanical Shock

IPC-A-610: Acceptability of Electronic Assemblies

12.5.2. PCB layout guideline

PCB designer comply with IPC-SM-782 and IPC-7095 requirements is recommended

12.5.3. PCB process

12.5.3.1. Board material

The Glass transition temperature (Tg) of Board material greater than 170 degree C is recommended for Pb-free and Green package.

12.5.3.2. Surface Finishes

In order to achieve high assembly yields, use of a surface finish that is planar

And has good solderability performance is important. Below methods are all known to provide an acceptable land pad surface.

*OSP (Organic Solderability Preservative)

*Nihau (Electroplated nickel /gold)

*Immersion Ag

*Immersion Sn

- 12.5.3.3. Solder Paste: No clean flux is recommended.**
- 12.5.3.4. Stencil Design Guidelines: Refer to IPC-7525 Stencil Design Guidelines process**
- 12.5.3.5. Reflow Oven: Forced convection reflow with nitrogen is recommended for Pb-free and Green package..**
- 12.5.3.6. Reflow profile: Using more than 8 zone oven is recommended for Pb-free and Green package.**
- 12.5.3.7. To use IPC-A-610 is recommended for soldered electrical and electronic assemblies.**
- 12.5.4. Storage condition and period for package**
 - Orise technology evaluates a ll plastic surface mount devices (SMDs) to ICP/JEDEC J-STD-020A, moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices, or refers to IPC JEDEC J-STD-033A Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices
- 12.5.4.1. The primary facts for the package storage include oxidation, static, and therefore, the following rules are recommended to be applied for the storage.**
- 12.5.4.2. The storage temperature should be 25°C ± 5°C, and the humidity should be in the range of 50% ± 10% R.H. after opening the dry pack.**
 - After the dry bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing.
- 12.5.4.3. Must be:**
 - a. Mounted within 168 hours(Level 3) and 72 hours(Level 4) at factory conditions of ≤ 30°C/ 60% R.H. or
 - b. Stored at ≤ 20% R.H.
- 12.5.4.4. Devices require baking, before mounting, if:**
 - a. Humidity Indicator Card shown warning message when read at 25°C±5°C, or
 - b. 12.5.4.3 is not met.
- 12.5.4.5. If baking is required. Devices may be baking for:**
 - a. 192 hour at 40°C+5°C/-0°C and <5% R.H. for low temperature device containers, or
 - b. 24 hours at 125±5°C for high temperature device containers
- 12.5.4.6. The storage condition should be consistent with the operation condition to prevent dewing phenomena.**
- 12.5.4.7. The storage location should be kept away from water and smoke; an isolated area with positive pressure control is preferred.**
- 12.5.4.8. For a long-term storage, it is recommended to keep in a container with Nitrogen in it.**
- 12.5.4.9. Avoid heavy objects stacked on the pack.**
- 12.5.4.10. Avoid the static damage; use an anti-static bag for the package.**

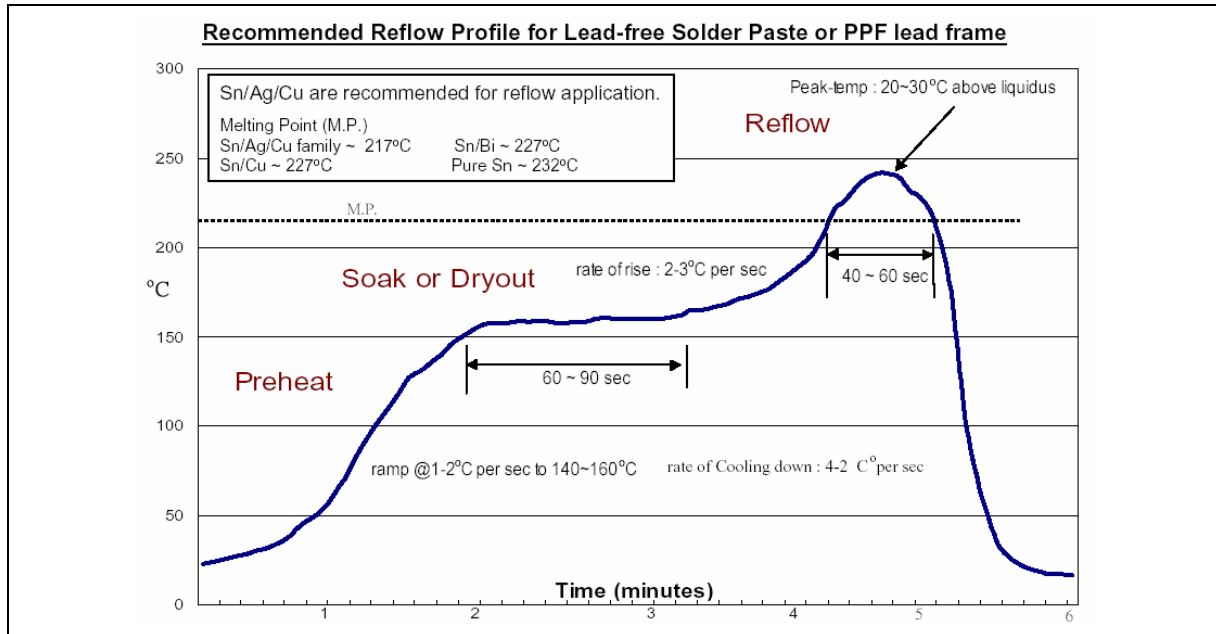
12.5.5. The classification of moisture sensitivity for Orise’s product packages are shown in the following

For Lead Free / Green Packages

Package	Moisture sensitivity level	Max. Reflow temperature	Floor life storage condition	Dry pack
QFP	LEVEL 3	255 +5/-0°C	168Hrs @ ≤ 30°C/ 60% R.H.	Yes

12.5.6. Recommended SMT Temperature Profile

This “Recommended” temperature profile is a rough guideline for SMT process reference. Most of ORISE leadframe base product choice Matte Tin and Sn/Bi for plating recipe. For PPF (Pre-Plated Frame) product with 63/37 solder paste, we recommend 240°C~245°C for peak temperature.



12.6. References

IPC:

<http://www.ipc.org>

*NEMI (National Electronics Manufacturing Initiative)

<http://www.nemi.org>

*HDPUG (High Density Package Users Group)

<http://www.hdpug.org>

*JEDEC (Joint Electronic Device Engineering Council)

<http://www.jedec.org>

*JEITA (Japan Electronic Industry Association)

<http://www.jeita.org>

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14. REVISION HISTORY

Date	Revision #	Description	Page
SEP. 21, 2007	0.1	Original	46