

ADVANCE INFORMATION

CG6264AM

2Mb (128K x 16) Pseudo Static RAM

Features

- Wide voltage range: **2.70V–3.30V**
- Access Time: 70ns
- Ultra-low active power
 - **Typical active current: 2.0mA @ f = 1 MHz**
 - **Typical active current: 13mA @ f = f_{max}**
- Ultra low standby power
- Easy memory expansion with \overline{CE} , CE₂, and \overline{OE} features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Offered in a 48 Ball BGA Package

Functional Description^[1]

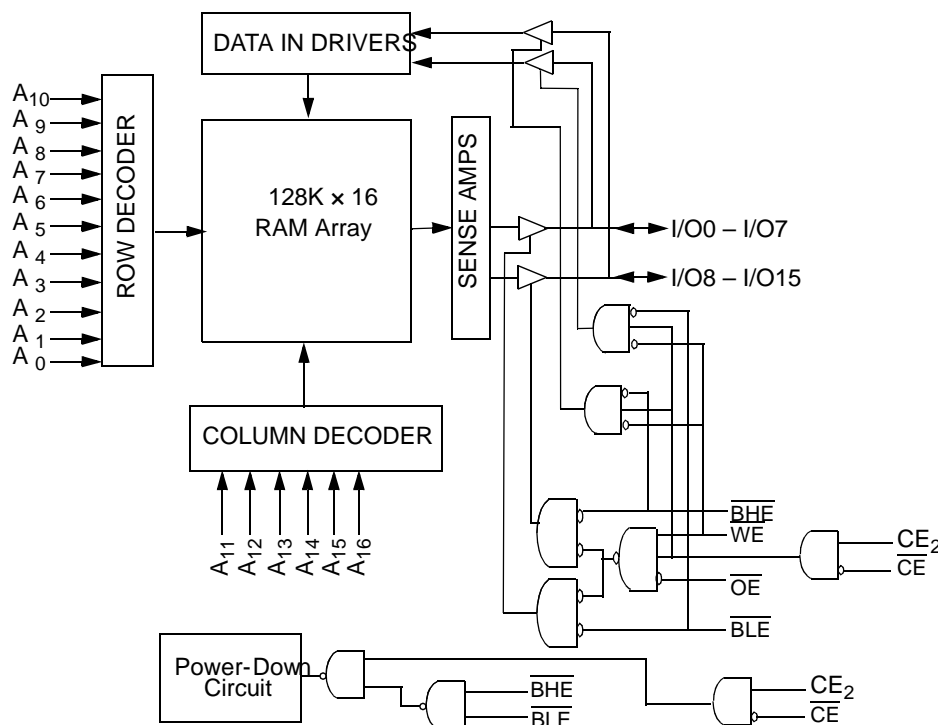
The CG6264AM is a high-performance CMOS Pseudo static RAM organized as 128K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life[®] (MoBL) in portable applications such as cellular telephones. The device can be put into standby mode reducing power consumption by

more than 99%. The device can also be put into standby mode when deselected (\overline{CE} HIGH or CE₂ LOW or both \overline{BHE} and \overline{BLE} are HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected (\overline{CE} HIGH or CE₂ LOW), outputs are disabled (\overline{OE} HIGH), both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, CE₂ HIGH and WE LOW). **The addresses must not be toggled once the read is started on the device.**

Writing to the device is accomplished by taking Chip Enables (\overline{CE} LOW and CE₂ HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

Reading from the device is accomplished by taking Chip Enables (\overline{CE} LOW and CE₂ HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this datasheet for a complete description of read and write modes

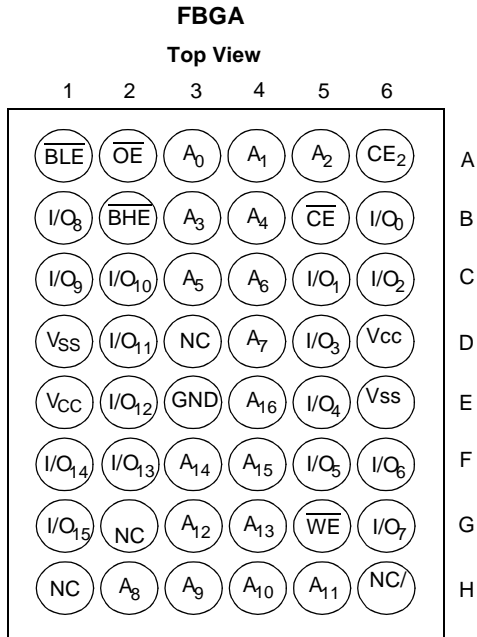
Logic Block Diagram



Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration^[2, 3, 4]



Note:

2. NC "no connect" - not connected internally to the die.
3. DNU pins are to be left floating or tied to V_{SS}.
4. Ball D3, H1, G2 and H6 are the expansion pins for the 4Mb, 8Mb, 16Mb and 32Mb density respectively.



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to + 150°C
 Ambient Temperature with Power Applied..... -55°C to + 85°C
 Supply Voltage to Ground Potential -0.4V to 4.6V

DC Voltage Applied to Outputs in High Z State^[5, 6, 7] -0.2V to 3.3V
 DC Input Voltage^[5, 6, 7] -0.2V to 3.3V
 Output Current into Outputs (LOW) 20 mA
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)
 Latch-Up Current >200 mA

Operating Range^[9]

Device	Range	Ambient Temperature	V _{CC}
CG6264AM	Industrial	-25°C to +85°C	2.70V to 3.30V

Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
					f = 1MHz		f = f _{max}			
Min.	Typ. ^[8]	Max.	Typ. ^[8]	Max.	Typ. ^[8]	Max.	Typ. ^[8]	Max.		
CG6264AM	2.70	3.0	3.30	70	2	4	13	17	55	80

Notes:

5. V_{IH(MAX)} = V_{CC} + 0.5V for pulse durations less than 20ns.
6. V_{IL(MIN)} = -0.5V for pulse durations less than 20ns.
7. Overshoot and undershoot specifications are characterized and are not 100% tested.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (typ) and T_A = 25C
9. V_{CC} must be at minimal operational levels before inputs are turned ON.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CG6264AM-70			Unit
			Min.	Typ. ^[8]	Max.	
V _{CC}	Supply Voltage		2.7		3.3	V
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA V _{CC} = 2.70V	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.0mA V _{CC} = 2.70V			0.4	V
V _{IH}	Input HIGH Voltage	V _{CC} = 2.7V to 3.3V	0.8*V _{CC}		V _{CC} +0.3V	V
V _{IL}	Input LOW Voltage	V _{CC} = 2.7V to 3.3V (F = 0)	-0.3		0.4	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}		13	17	mA
		f = 1 MHz	V _{CC} = V _{CCmax} I _{OUT} = 0 mA CMOS levels	2.0	4	mA
I _{SB1}	Automatic \overline{CE} Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$ f = f _{MAX} (Address and Data Only), f = 0 (\overline{OE} , \overline{WE} , \overline{BHE} and \overline{BLE}), V _{CC} = 3.30V	V _{CC} = 3.3V		350	μA
I _{SB2}	Automatic \overline{CE} Power-Down Current — CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0, V _{CC} = 3.30V	V _{CC} = 3.3V	55	80	μA

Capacitance^[10]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ)}	6	pF
C _{OUT}	Output Capacitance		8	pF

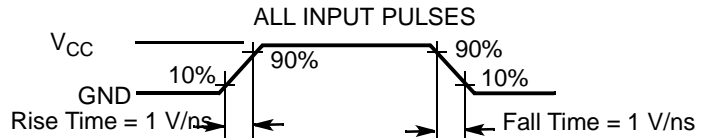
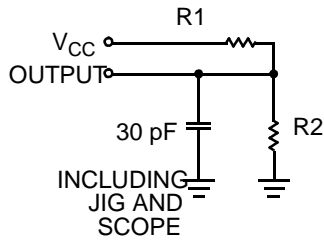
Thermal Resistance^[10]

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	θ _{JA}	55	°C/W
Thermal Resistance (Junction to Case)		θ _{JC}	16	°C/W

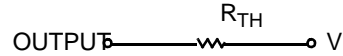
Note:

10. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENINEQUIVALENT



Parameters	3.0V V _{CC}	Unit
R1	1179	Ω
R2	1941	Ω
R _{TH}	733	Ω
V _{TH}	1.87	V

Switching Characteristics Over the Operating Range^[11]

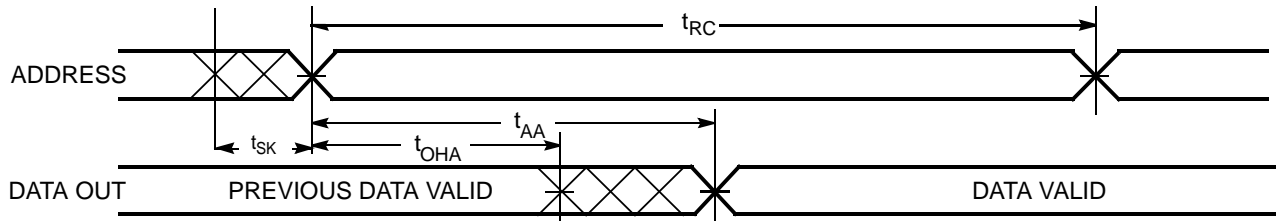
Parameter	Description	70 ns		Unit
		Min.	Max.	
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	\overline{CE} LOW and CE_2 HIGH to Data Valid		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		35	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[12, 14]	5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[12, 14]		25	ns
t_{LZCE}	\overline{CE} LOW and CE_2 HIGH to Low Z ^[12, 14]	5		ns
t_{HZCE}	\overline{CE} HIGH and CE_2 LOW to High Z ^[12, 14]		25	ns
t_{DBE}	BLE / BHE LOW to Data Valid		70	ns
t_{LZBE}	\overline{BLE} / \overline{BHE} LOW to Low Z ^[12, 14]	5		ns
t_{HZBE}	\overline{BLE} / \overline{BHE} HIGH to HIGH Z ^[12, 14]		25	ns
t_{sk}	Address Skew		0	ns
WRITE CYCLE^[13]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	\overline{CE} LOW and CE_2 HIGH to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	\overline{WE} Pulse Width	45		ns
t_{BW}	\overline{BLE} / \overline{BHE} LOW to Write End	60		ns
t_{SD}	Data Set-Up to Write End	45		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[12, 14]		25	ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[12, 14]	5		ns

Notes:

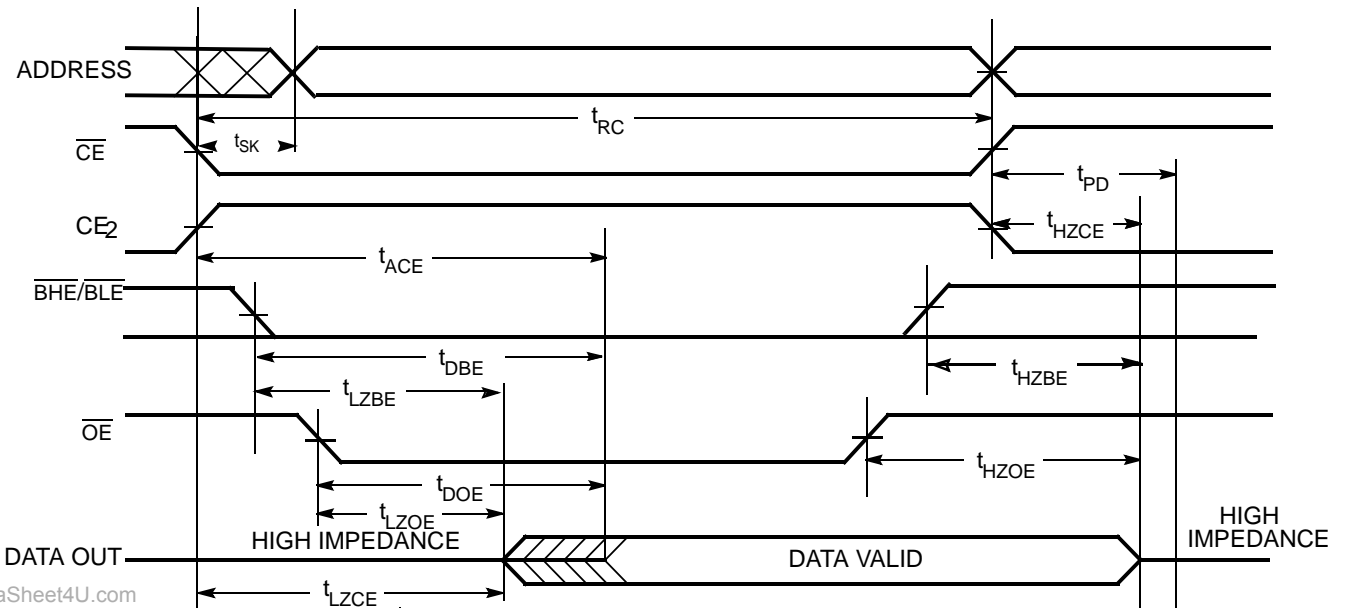
11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
12. t_{LZOE} , t_{HZOE} , t_{LZBE} , and t_{HZBE} transitions are measured when the outputs enter a high impedance state.
13. The internal Write time of the memory is defined by the overlap of \overline{WE} , $CE = V_{IL}$, BHE and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
14. High-Z and Low-Z parameters are characterized and are not 100% tested.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)^[15, 16]



Read Cycle 2 (\overline{OE} Controlled)^[15, 16]



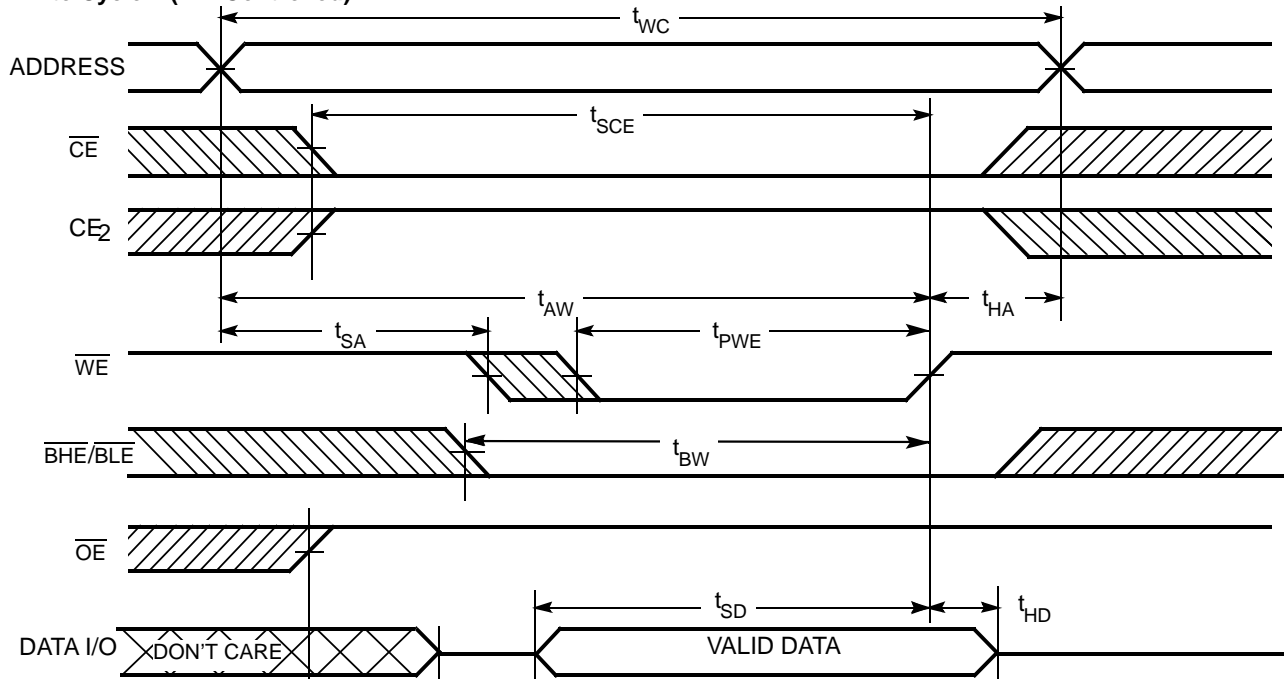
www.DataSheet4U.com

Note:

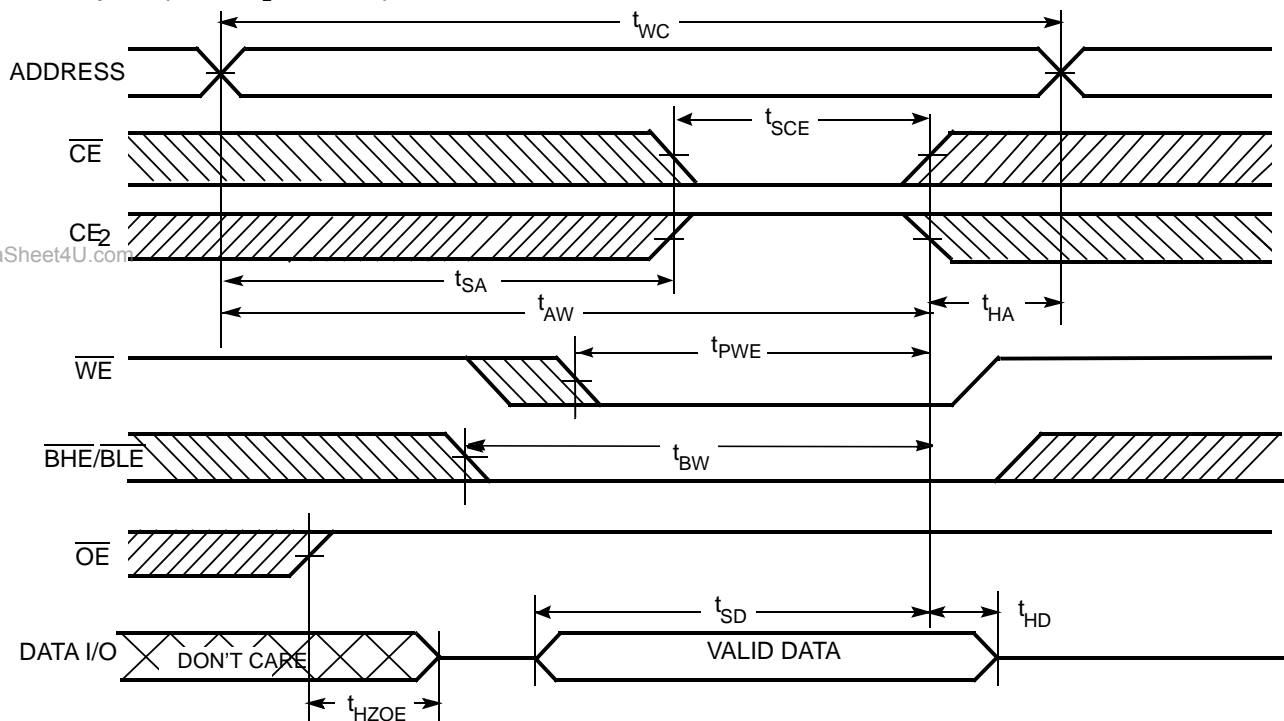
- 15. \overline{WE} is HIGH for read cycle.
- 16. Addresses should not be toggled after the start of a read cycle

Switching Waveforms (continued)

Write Cycle 1 (\overline{WE} Controlled) [13, 14, 17, 18, 19]



Write Cycle 2 (\overline{CE} or CE_2 Controlled) [13, 14, 17, 18, 19]

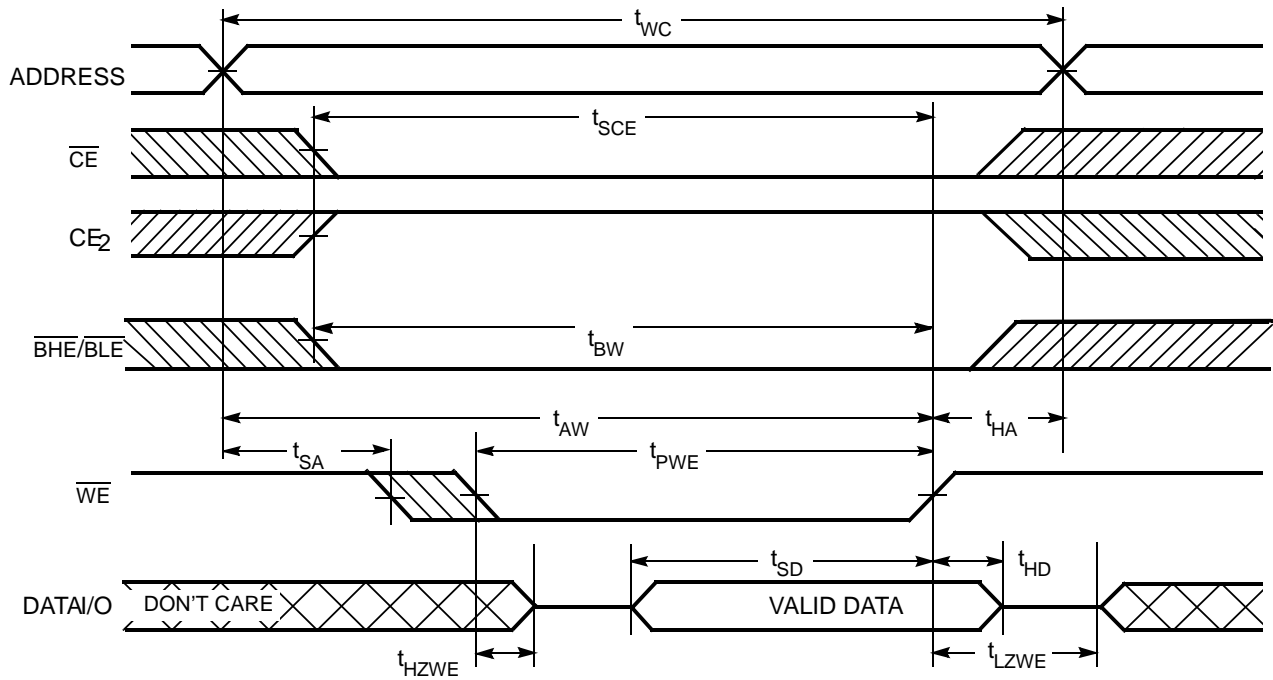


Notes:

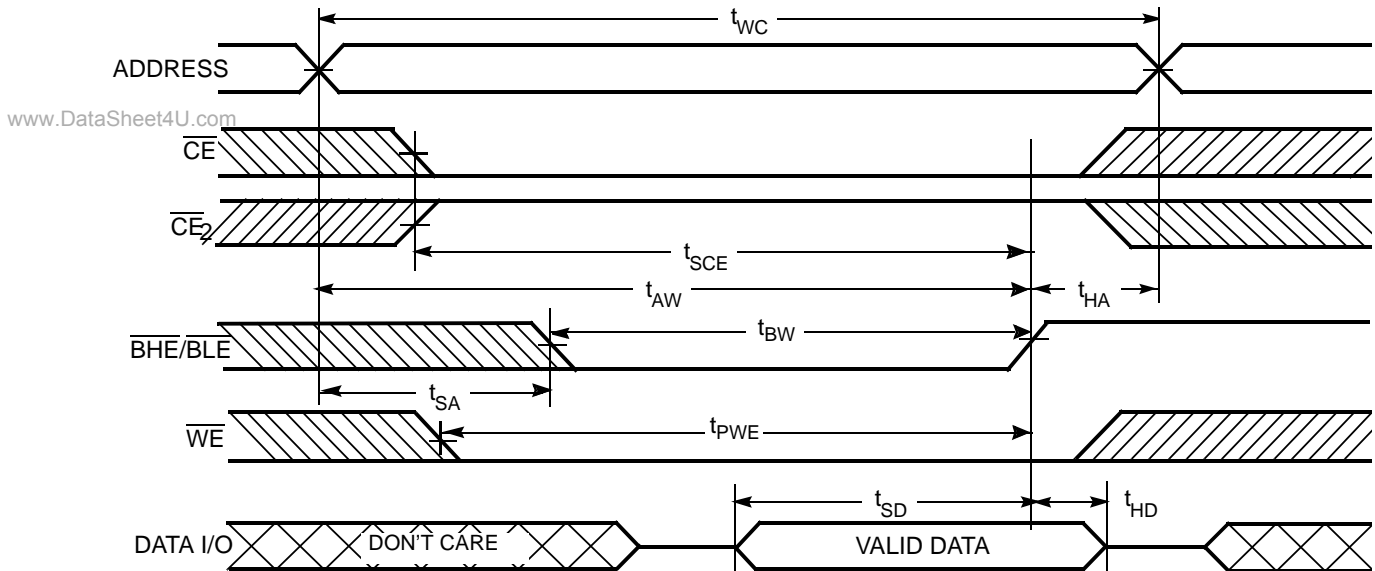
- 17. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 18. If Chip Enable goes INACTIVE and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
- 19. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 (WE Controlled, OE LOW)^[18, 19]



Write Cycle 4 (BHE/BLE Controlled, OE LOW)^[18, 19]



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Truth Table^[20]

CE	CE ₂	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby (I _{SB})
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby (I _{SB})
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I _{SB})
L	H	H	L	L	L	Data Out (I/O0 – I/O15)	Read	Active (I _{CC})
L	H	H	L	H	L	Data Out (I/O0 – I/O7); High Z (I/O8 – I/O15)	Read	Active (I _{CC})
L	H	H	L	L	H	High Z (I/O0 – I/O7); Data Out (I/O8 – I/O15)	Read	Active (I _{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I _{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I _{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I _{CC})
L	H	L	X	L	L	Data In (I/O0 – I/O15)	Write	Active (I _{CC})
L	H	L	X	H	L	Data In (I/O0 – I/O7); High Z (I/O8 – I/O15)	Write	Active (I _{CC})
L	H	L	X	L	H	High Z (I/O0 – I/O7); Data In (I/O8 – I/O15)	Write	Active (I _{CC})

Note:

20. H = V_{IH}, L = V_{IL}, X = Don't Care

Ordering Information

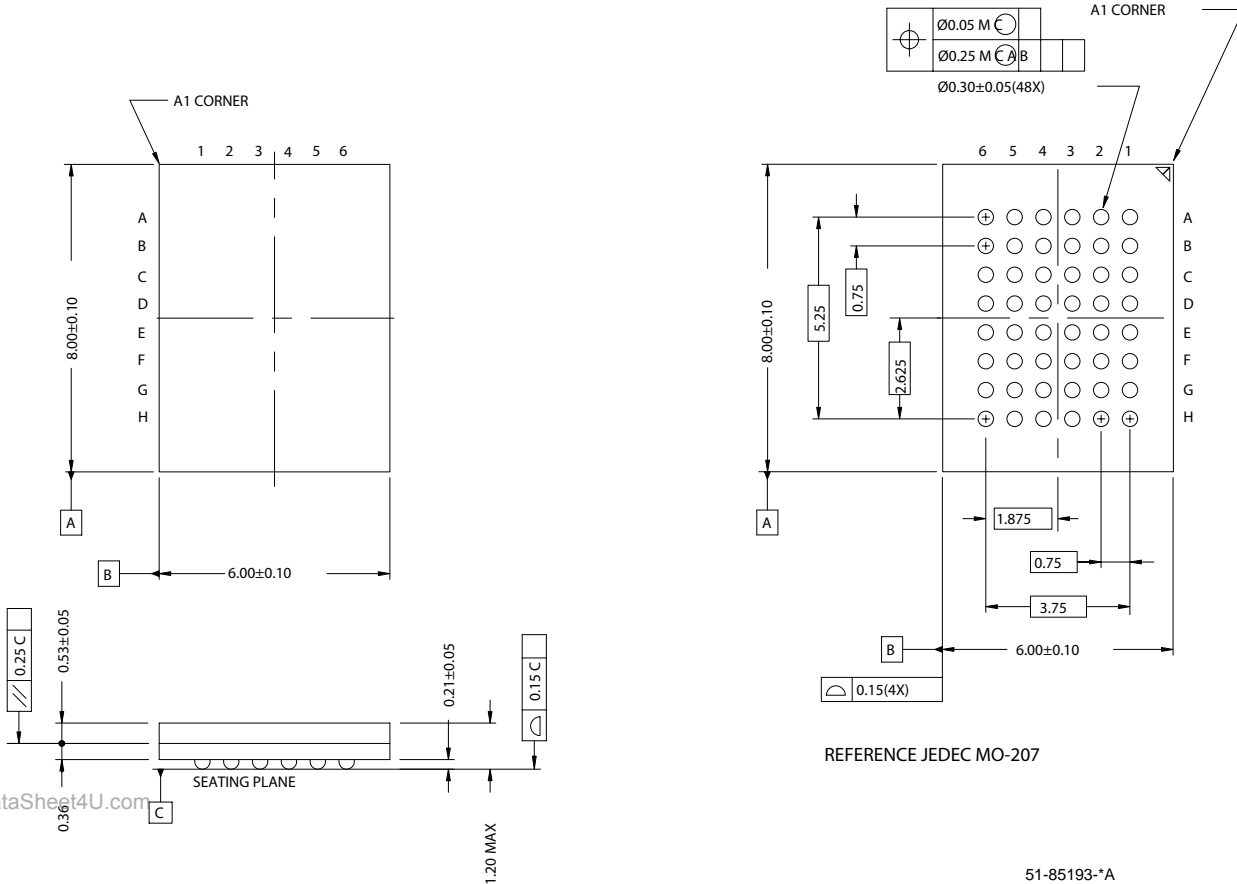
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CG6264AM	BA48K	48-ball Fine Pitch BGA (6 mm × 8mm × 1.2 mm)	Industrial

Package

48-Ball (6 mm x 8mm x 1.2 mm) FBGA BA48K

TOP VIEW

BOTTOM VIEW



51-85193-*A

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CG6264AM

Document Title: CG6264AM MoBL3[®] 2Mb (128K x 16) Pseudo Static RAM Document Number: 38-XXXXX				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**		10/16/03	MPR	New Datasheet