

# CGHV27200

## 200 W, 2500-2700 MHz, GaN HEMT for LTE

Cree's CGHV27200 is a gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically for high efficiency, high gain and wide bandwidth capabilities, which makes the CGHV27200 ideal for 2.5-2.7 GHz LTE and BWA amplifier applications. The transistor is supplied in a ceramic/metal flange package.



Package Type: 440162 and 440161  
PN: CGHV27200F and CGHV27200P

### Typical Performance Over 2.5 - 2.7 GHz ( $T_c = 25^\circ\text{C}$ ) of Demonstration Amplifier

Parameter	2.5 GHz	2.6 GHz	2.7 GHz	Units
Gain @ 47 dBm	15.0	16.0	16.0	dB
ACLR @ 47 dBm	-36.5	-37.5	-37.0	dBc
Drain Efficiency @ 47 dBm	29.0	28.5	29.0	%

**Note:**

Measured in the CGHV27200-TB amplifier circuit, under WCDMA 3GPP test model 1, 64 DPCH, 45% clipping, PAR = 7.5 dB @ 0.01% Probability on CCDF.

### Features

- 2.5 - 2.7 GHz Operation
- 16 dB Gain
- -37 dBc ACLR at 50 W  $P_{AVE}$
- 29 % Efficiency at 50 W  $P_{AVE}$
- High Degree of DPD Correction Can be Applied





## Absolute Maximum Ratings (not simultaneous) at 25 °C Case Temperature

Parameter	Symbol	Rating	Units	Units
Drain-Source Voltage	$V_{DSS}$	125	Volts	25 °C
Gate-to-Source Voltage	$V_{GS}$	-10, +2	Volts	25 °C
Storage Temperature	$T_{STG}$	-65, +150	°C	
Operating Junction Temperature	$T_J$	225	°C	
Maximum Forward Gate Current	$I_{GMAX}$	32	mA	25 °C
Maximum Drain Current <sup>1</sup>	$I_{DMAX}$	12	A	25 °C
Soldering Temperature <sup>2</sup>	$T_S$	245	°C	
Screw Torque	$\tau$	80	in-oz	
Thermal Resistance, Junction to Case <sup>3</sup>	$R_{\theta JC}$	1.22	°C/W	85 °C, $P_{DISS} = 96$ W
Thermal Resistance, Junction to Case <sup>4</sup>	$R_{\theta JC}$	1.54	°C/W	85 °C, $P_{DISS} = 96$ W
Case Operating Temperature <sup>5</sup>	$T_C$	-40, +150	°C	30 seconds

Note:

<sup>1</sup> Current limit for long term, reliable operation.

<sup>2</sup> Refer to the Application Note on soldering at <http://www.cree.com/rf/document-library>

<sup>3</sup> Measured for the CGHV27200P

<sup>4</sup> Measured for the CGHV27200F

<sup>5</sup> See also, the Power Dissipation De-rating Curve on Page 6

## Electrical Characteristics ( $T_C = 25$ °C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>DC Characteristics<sup>1</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.0	-2.3	$V_{DC}$	$V_{DS} = 10$ V, $I_D = 32$ mA
Gate Quiescent Voltage	$V_{GS(Q)}$	-	-2.7	-	$V_{DC}$	$V_{DS} = 50$ V, $I_D = 1.0$ A
Saturated Drain Current <sup>2</sup>	$I_{DS}$	24	28.8	-	A	$V_{DS} = 6.0$ V, $V_{GS} = 2.0$ V
Drain-Source Breakdown Voltage	$V_{BR}$	125	-	-	$V_{DC}$	$V_{GS} = -8$ V, $I_D = 32$ mA
<b>RF Characteristics<sup>5</sup> (<math>T_C = 25</math> °C, <math>F_0 = 2.7</math> GHz unless otherwise noted)</b>						
Saturated Output Power <sup>3,4</sup>	$P_{SAT}$	-	300	-	W	$V_{DD} = 50$ V, $I_{DQ} = 1.0$ A
Pulsed Drain Efficiency <sup>3</sup>	$\eta$	-	62	-	%	$V_{DD} = 50$ V, $I_{DQ} = 1.0$ A, $P_{OUT} = P_{SAT}$
Gain <sup>6</sup>	G	-	15.25	-	dB	$V_{DD} = 50$ V, $I_{DQ} = 1.0$ A, $P_{OUT} = 47$ dBm
WCDMA Linearity <sup>6</sup>	ACLR	-	-37	-	dBc	$V_{DD} = 50$ V, $I_{DQ} = 1.0$ A, $P_{OUT} = 47$ dBm
Drain Efficiency <sup>6</sup>	$\eta$	-	30.5	-	%	$V_{DD} = 50$ V, $I_{DQ} = 1.0$ A, $P_{OUT} = 47$ dBm
Output Mismatch Stress <sup>3</sup>	VSWR	-	-	10 : 1	$\Psi$	No damage at all phase angles, $V_{DD} = 50$ V, $I_{DQ} = 1.0$ A, $P_{OUT} = 200$ W Pulsed
<b>Dynamic Characteristics</b>						
Input Capacitance <sup>7</sup>	$C_{GS}$	-	97	-	pF	$V_{DS} = 50$ V, $V_{GS} = -8$ V, $f = 1$ MHz
Output Capacitance <sup>7</sup>	$C_{DS}$	-	13.4	-	pF	$V_{DS} = 50$ V, $V_{GS} = -8$ V, $f = 1$ MHz
Feedback Capacitance	$C_{GD}$	-	0.94	-	pF	$V_{DS} = 50$ V, $V_{GS} = -8$ V, $f = 1$ MHz

Notes:

<sup>1</sup> Measured on wafer prior to packaging.

<sup>2</sup> Scaled from PCM data.

<sup>3</sup> Pulse Width = 100  $\mu$ s, Duty Cycle = 10%

<sup>4</sup>  $P_{SAT}$  is defined as  $I_G = 3$  mA peak.

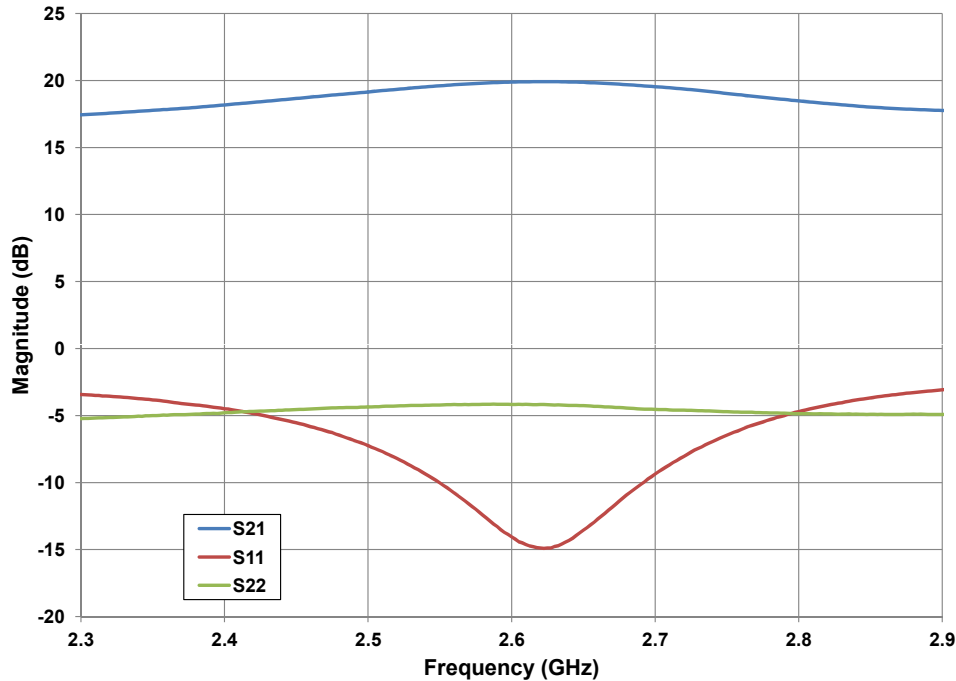
<sup>5</sup> Measured in CGHV27200-TB.

<sup>6</sup> Single Carrier WCDMA, 3GPP Test Model 1, 64 DPCH, 45% Clipping, PAR = 7.5 dB @ 0.01% Probability on CCDF.

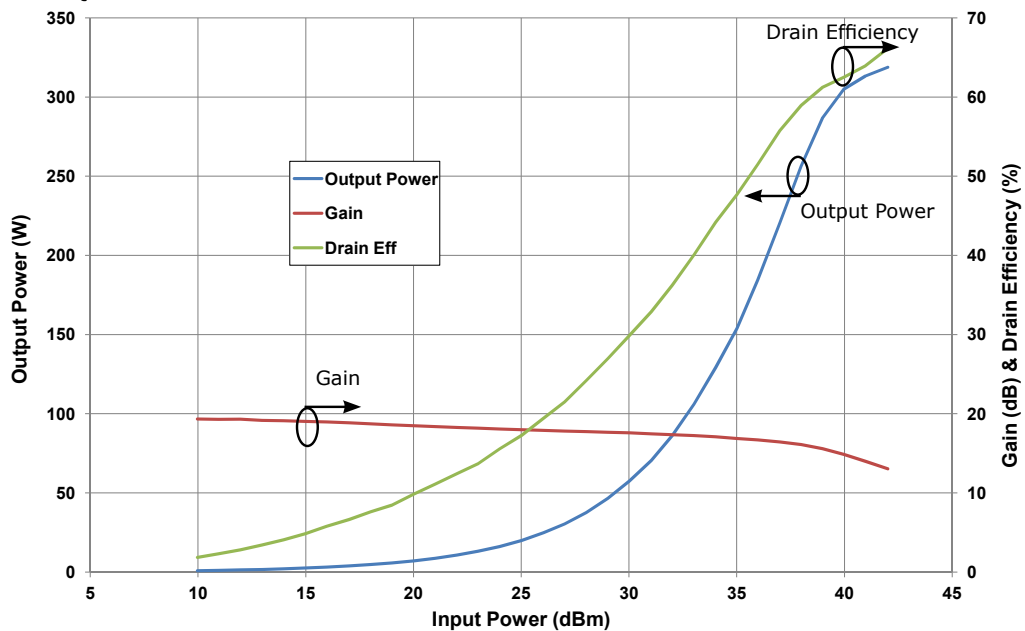
<sup>7</sup> Includes package and internal matching components.

## Typical Performance

**Figure 1. - Small Signal Gain and Return Losses vs Frequency for the CGHV27200 measured in CGHV27200-TB Amplifier Circuit**  
 $V_{DD} = 50\text{ V}, I_{DQ} = 1.0\text{ A}$

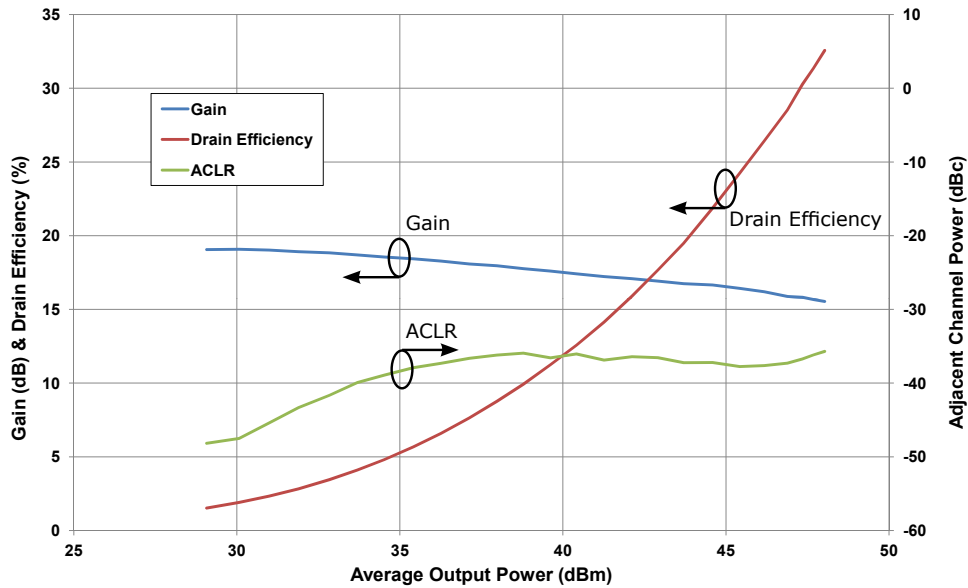


**Figure 2. - Typical Pulsed Measurements vs Input Power of the CGHV27200 measured in CGHV27200-TB Amplifier Circuit.**  
 $V_{DS} = 50\text{ V}, I_{DQ} = 1.0\text{ A}, \text{Freq} = 2.6\text{ GHz}, \text{Pulse Width} = 100\ \mu\text{s}, \text{Duty Cycle} = 10\%$

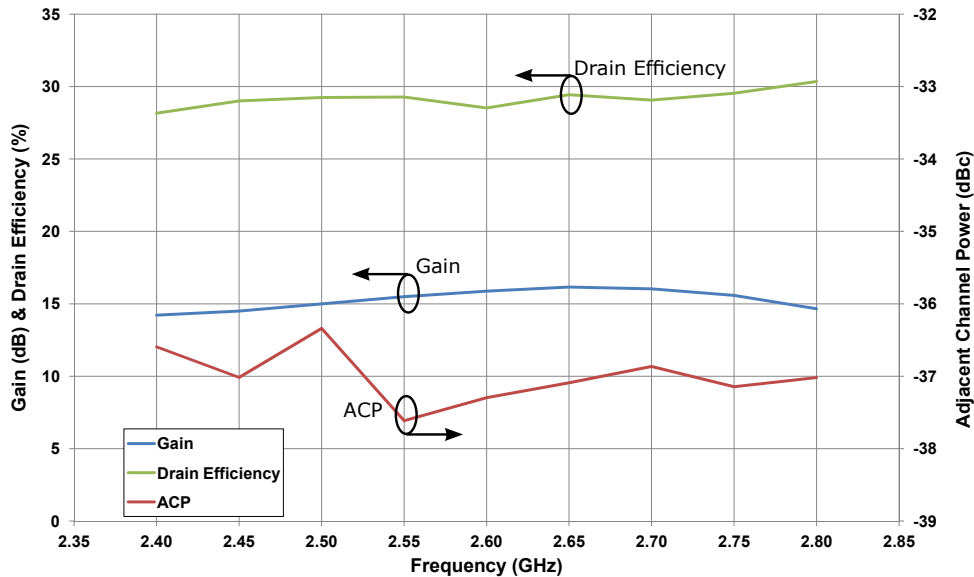


## Typical Performance

**Figure 3. - Typical Linearity vs Output Power for the CGHV27200 measured in CGHV27200-TB Amplifier Circuit**  
 $V_{DD} = 50\text{ V}$ ,  $I_{DQ} = 1.0\text{ A}$ , Freq = 2.6 GHz, 1c WCDMA 7.5 dB PAR

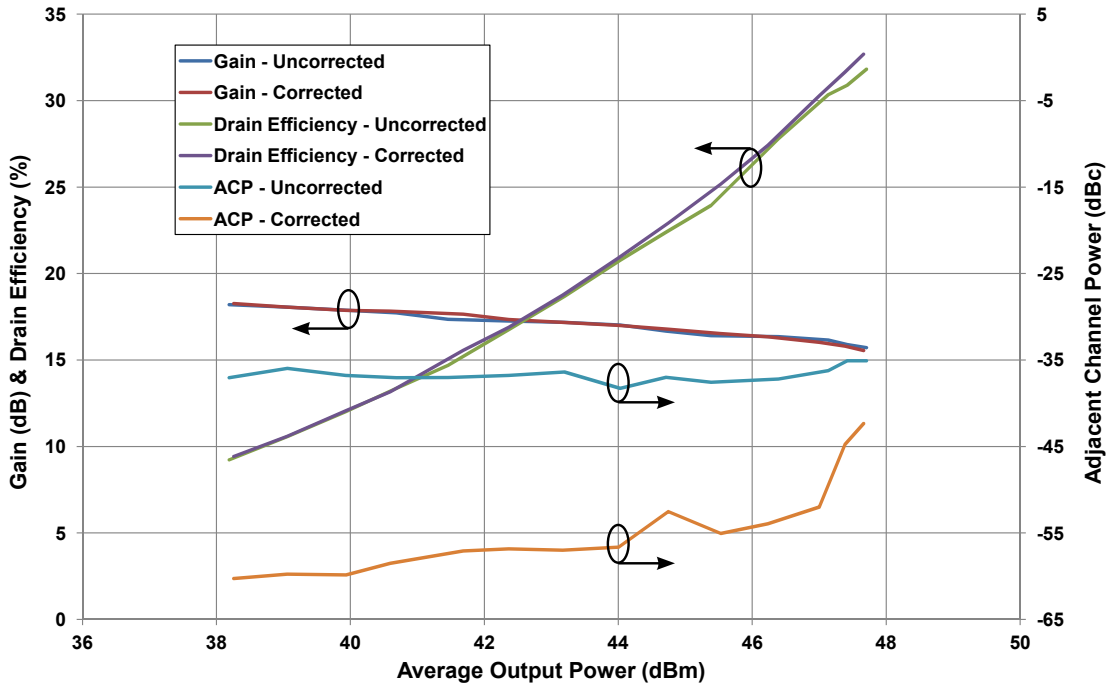


**Figure 4. - Typical Linearity at  $P_{AVE} = 47\text{ dBm}$  over Frequency of the CGHV27200 measured in CGHV27200-TB Amplifier Circuit.**  
 $V_{DD} = 50\text{ V}$ ,  $I_{DQ} = 1.0\text{ A}$ , 1c WCDMA 7.5 dB PAR

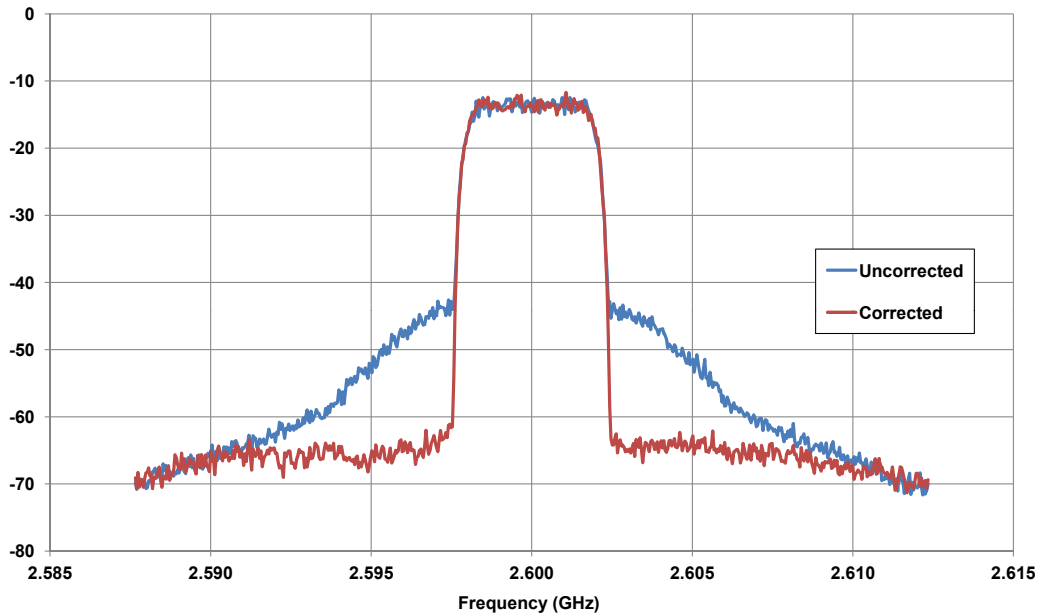


## Typical Performance

**Figure 5. - Typical Linearity under DPD vs Output Power**  
 $V_{DD} = 50\text{ V}$ ,  $I_{DQ} = 1.0\text{ A}$ , Freq = 2.6 GHz, 1c WCDMA 7.5 dB PAR

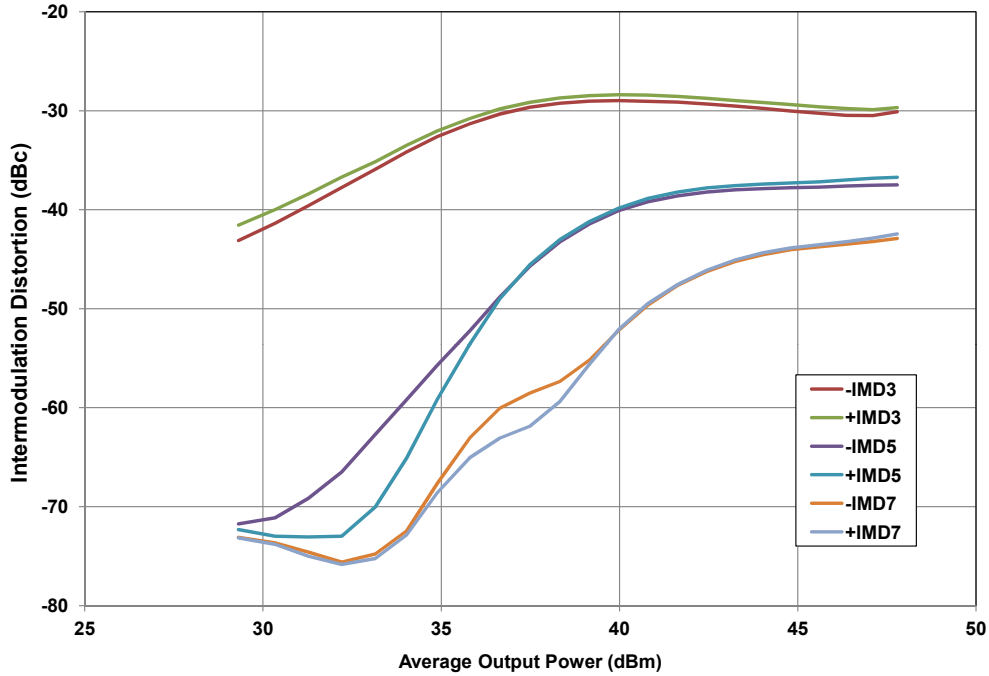


**Figure 6. - Spectral Mask at  $P_{AVE} = 47\text{ dBm}$  with and without DPD**  
 $V_{DD} = 50\text{ V}$ ,  $I_{DQ} = 1.0\text{ A}$ , 1c WCDMA 7.5 dB PAR

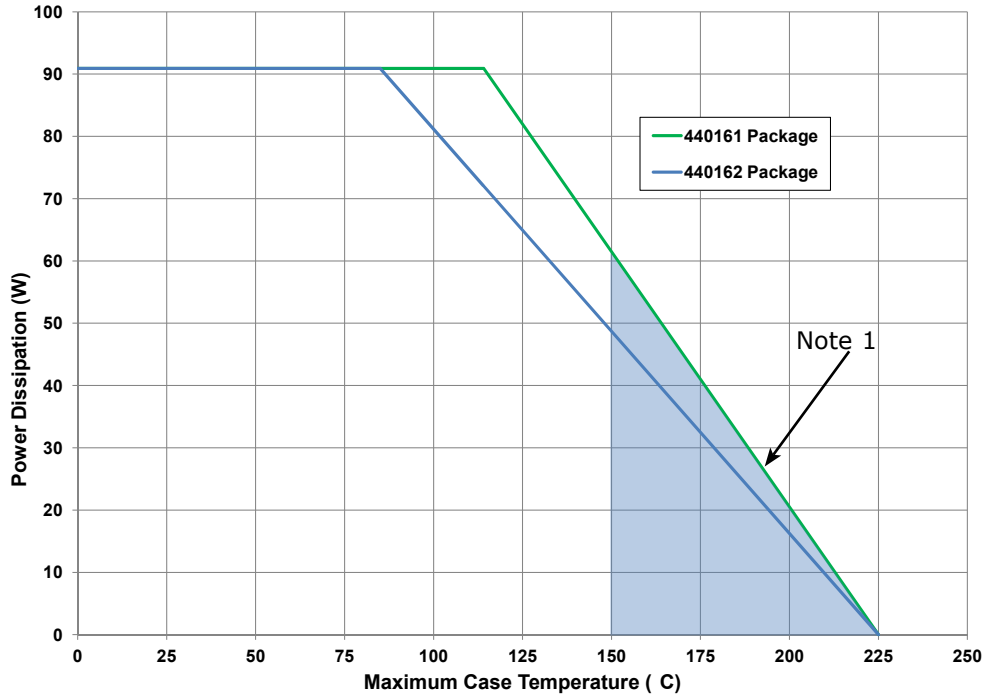


## Typical Performance

**Figure 7. - Intermodulation Distortion Products vs Output Power**  
 $V_{DD} = 50\text{ V}$ ,  $I_{DQ} = 1.0\text{ A}$ , Tone Spacing = 100 kHz

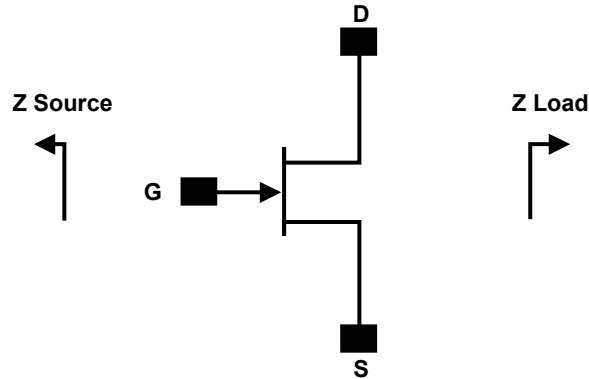


**Figure 8. - Power Dissipation Derating Curve**



Note 1. Area exceeds Maximum Case Operating Temperature (See Page 2).

## Source and Load Impedances

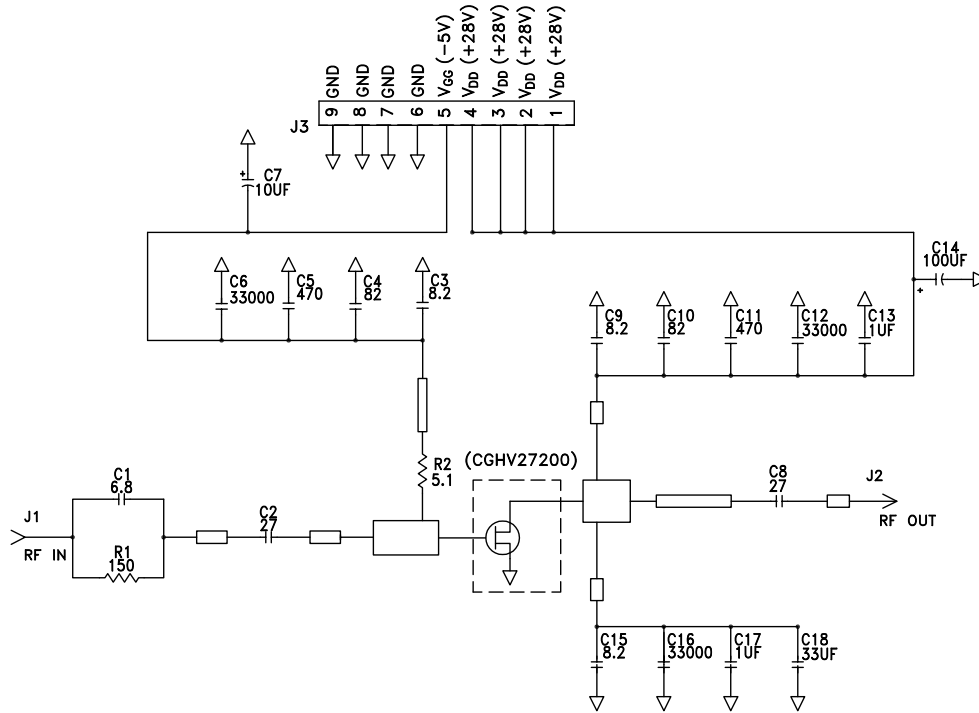


Frequency (MHz)	Z Source	Z Load
2500	7.12 - j10.19	2.23 - j0.03
2550	6.93 - j10.38	2.27 + j0.08
2600	6.61 - j10.59	2.32 + j0.18
2650	6.17 - j10.77	2.37 + j0.27
2700	5.61 - j10.87	2.41 + j0.33

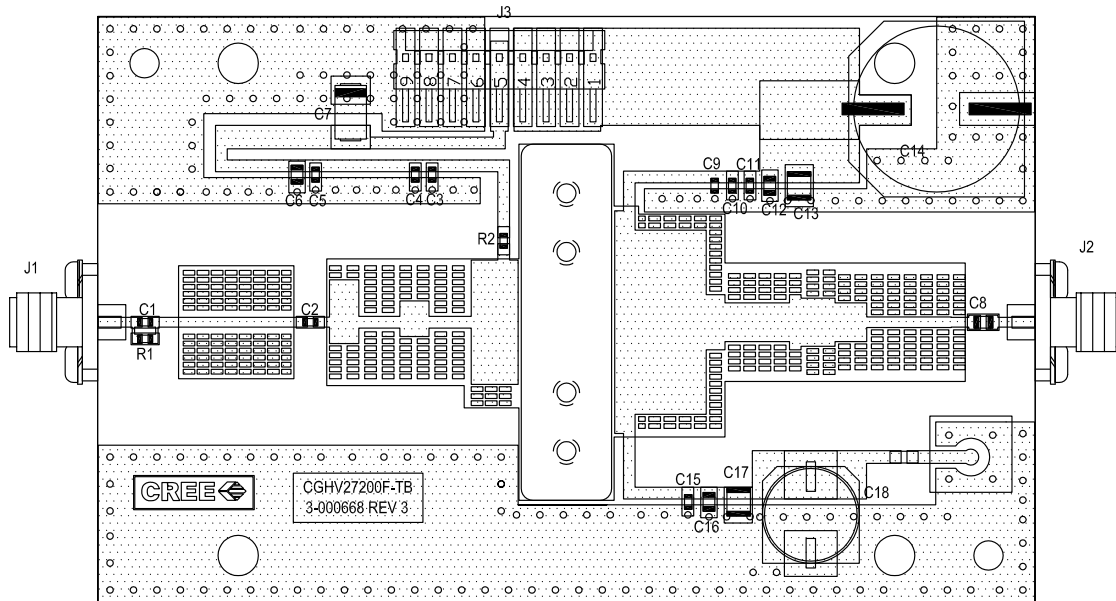
Note<sup>1</sup>:  $V_{DD} = 50\text{ V}$ ,  $I_{DQ} = 1.0\text{ A}$ . In the 440162 package.

Note<sup>2</sup>: Impedances are extracted from CGHV27200-TB demonstration circuit and are not source and load pull data derived from transistor.

## CGHV27200-TB Demonstration Amplifier Circuit Schematic



## CGHV27200-TB Demonstration Amplifier Circuit Outline

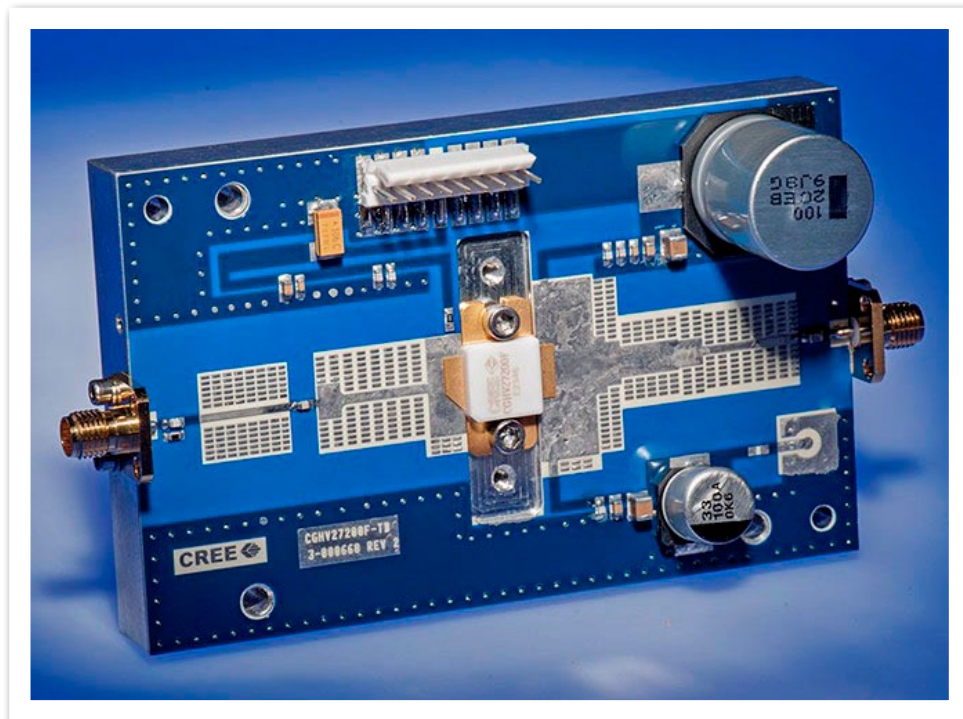




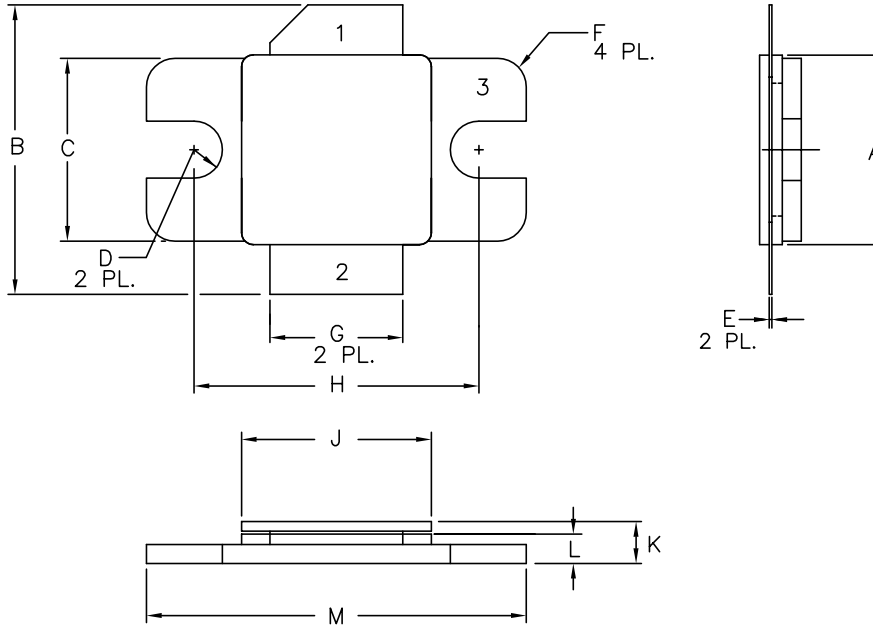
## CGHV27200-TB Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
R1	RES, 1/16 W, 0603, 1%, 150 OHMS	1
R2	RES, 1/16 W, 0603, 1%, 5.1 OHMS	1
C1	CAP, 6.2 pF, +/-0.25 pF, 0603, ATC600S	1
C2	CAP, 27 pF, +/-5%, 0603, ATC600S	1
C3,C9,C15	CAP, 8.2 pF, +/-0.25 pF, 0603, ATC600S	3
C4,C10	CAP, 82.0 pF, +/-5%, 0603, ATC600S	2
C5,C11	CAP, 470 pF, 5%, 100 V, 0603, X7R	2
C6,C12,C16	CAP, 33000 pF, 0805, 100 V, X7R	3
C7	CAP, 10 UF, 16V, TANTALUM	1
C8	CAP, 27 pF, +/-5%, 250 V, 0603, ATC600S	1
C13,C17	CAP, 1.0 UF, 100 V, 10%, X7R, 1210	2
C14	CAP, 100 UF, +/-20%, 160V, ELECTROLYTIC	2
C18	CAP, 33 UF, 20%, G CASE	1
J1,J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST	2
J3	CONN, Header, RT> PLZ, 0.1 CEN, LK, 9 POS	1
	PCB, RO4350, 0.020" THK, CGHV27200	1
	2-56 SOC HD SCREW 1/4 SS	4
	#2 SPLIT LOCKWASHER SS	4
	CGHV27200	1

## CGHV27200-TB Demonstration Amplifier Circuit



## Product Dimensions CGHV27200F (Package Type — 440162)



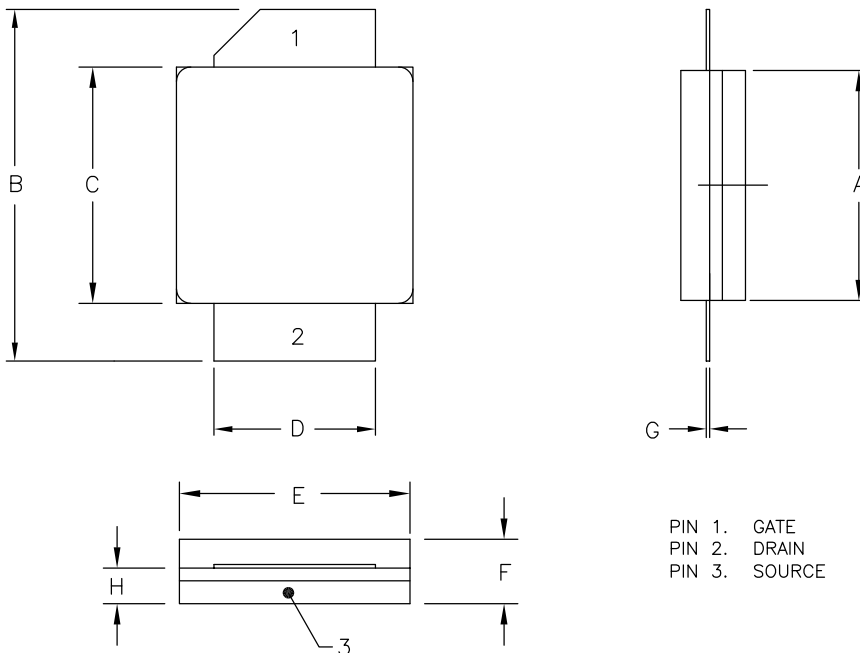
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.580	.620	14.73	15.75
C	.380	.390	9.65	9.91
D	.055	.065	1.40	1.65
E	.004	.006	0.10	0.15
F	.055	.065	1.40	1.65
G	.275	.285	6.99	7.24
H	.595	.605	15.11	15.37
J	.395	.405	10.03	10.29
K	.129	.149	3.28	3.78
L	.053	.067	1.35	1.70
M	.795	.805	20.19	20.45

PIN 1. GATE  
 PIN 2. DRAIN  
 PIN 3. SOURCE

## Product Dimensions CGHV27200P (Package Type — 440161)



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.395	.407	10.03	10.34
B	.594	.634	15.09	16.10
C	.395	.407	10.03	10.34
D	.275	.285	6.99	7.24
E	.395	.407	10.03	10.34
F	.129	.149	3.28	3.78
G	.004	.006	0.10	0.15
H	.057	.067	1.45	1.70

PIN 1. GATE  
 PIN 2. DRAIN  
 PIN 3. SOURCE



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