National Semiconductor

CGS100P2530
PECL-TTL 1 to 10 Minimum Skew Clock Driver
CGS100P2531
PECL-TTL 2 to 10 Minimum Skew Clock Driver

General Description

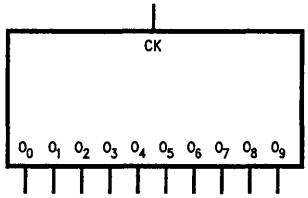
These minimum skew clock drivers are designed for Clock Generation & Support (CGS) applications, particularly for ECL to TTL clock tree distribution schemes. The '2530 and '2531 are single supply devices with guaranteed minimum output skew across the outputs of a given device. Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The '2530 is a minimum skew clock driver with one input driving ten outputs and the '2531 is a selectable two input to 10 outputs, specifically designed for signal generation and clock distribution applications.

Features

- PECL-TTL version of National's CGS74B2528 TTL clock drivers
- Clock Generation & Support (CGS) devices ideal for ECL and TTL clock trees with CGS 100311
- 1-to-10 or 2-to-10 low skew clock distribution
- 550 ps pin-to-pin output skew
- Specification for transition skew to meet duty cycle requirements
- 28-pin PCC to minimize high speed switching noise and for low dynamic power consumption
- Current sourcing 48 mA and current sinking of 64 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Logic Symbols

'2530



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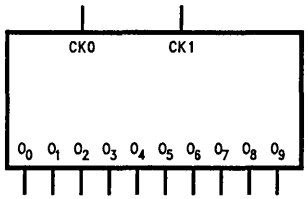
'2531



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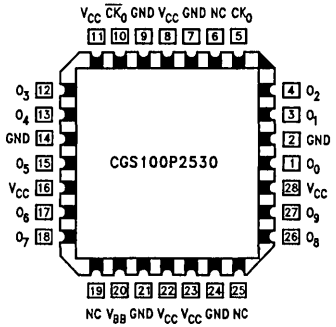
Connection Diagrams

Pin Assignment for LCC



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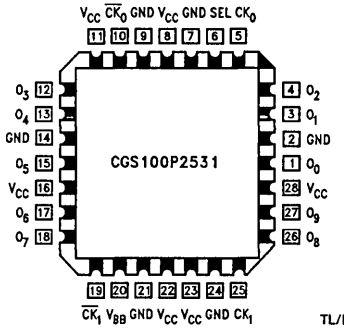

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Functional Description

On the multiplexed clock device, the SEL pin is used to determine which CKn will have an active effect on the outputs of the circuit. When SEL = 1, the CK1 input is selected and when SEL = 0, the CK0 input is selected. The non-selected CKn input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CK, CK1/CK0 pins when either the multiplexed ('2531) or the straight ('2530) clock distribution chip is selected.

Pin Description

Pin Names	Description
CK	PECL Differential Clock Input ('2530)
CK0, CK1	PECL Differential Clock Input ('2531)
O_0–O_9	TTL Outputs
SEL	PECL Clock Select ('2531)

Truth Tables

'2530

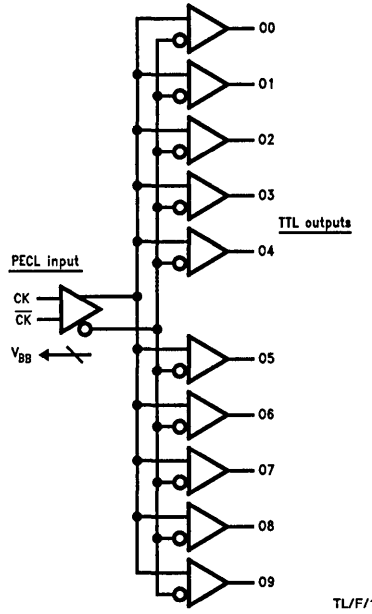
Inputs		Outputs
CK	$\overline{CK}$	O_0–O_9
L	H	L
H	L	H
L	L	U
H	H	U
L	V_{BB}	L*
H	V_{BB}	H*
V_{BB}	X	V_{BB}

L = Low Logic Level
H = High Logic Level
X = Don't Care
U = Undefined
* = Single Ended Operation

'2531

Inputs					Outputs
CK0	$\overline{CK0}$	CK1	$\overline{CK1}$	SEL	O_0–O_9
L	H	X	X	L	L
H	L	X	X	L	H
L	L	X	X	L	U
H	H	X	X	L	U
L	V_{BB}	X	X	L	L*
H	V_{BB}	X	X	L	H*
X	X	L	H	H	L
X	X	H	L	H	H
X	X	L	L	H	U
X	X	H	H	H	U
X	X	L	V_{BB}	H	L*
X	X	H	V_{BB}	H	H*

'2530



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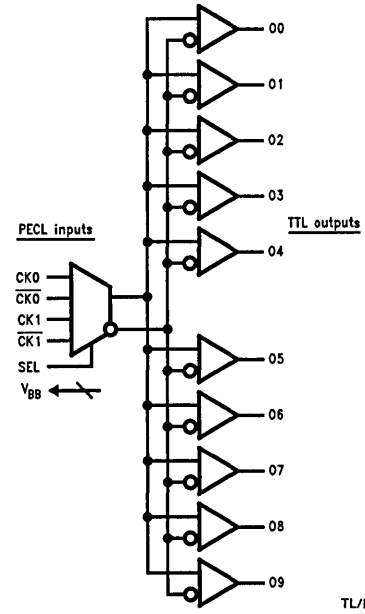
'2531



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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature Plastic	150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
TTL Input Voltage (Note 2)	−0.5V to +7.0V
TTL Input Current (Note 2)	−30 mA to +5.0 mA
V_{BB} Output Current	−5.0 mA to +1.0 mA
ECL Input Potential to GND Pin	−0.5V to V_{CC} +0.5V
Typical θ_{JA}	V Package
0 LFM Airflow	69
225 LFM	53
500 LFM	45
Voltage Applied to Output (with V_{CC} = 0V)	−0.5V to V_{CC}
Current Applied to Output in Low State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	2000V

Recommended Operating Conditions

Operating Free Air Temperature Range	−40°C to +85°C
Supply Voltage	4.5V to 5.5V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage		I_{OH} = −3 mA, V_{CC} = 4.5V	2.4			V
			I_{OH} = 48 mA, V_{CC} = 4.5V	2.0			
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V, I_{OL} = 64 mA		0.375	0.55	V
V_{BB}	Output Reference Voltage		$I_{V_{BB}}$ = −1 mA	V_{CC} − 1.38		V_{CC} − 1.26	V
V_{DIFF}	Input Voltage Differential		Required for Full Output Swing	150			mV
V_{CM}	Common Mode Voltage		High Level	V_{CC} − 1.6		V_{CC} − 0.4	V
V_{IH}	Input High Voltage		Guarantee HIGH Signal for All Inputs	V_{CC} − 1.165		V_{CC} − 0.87	V
V_{IL}	Input Low Voltage		Guarantee HIGH Signal for All Inputs	V_{CC} − 1.83		V_{CC} − 1.475	V
I_{IL}	Low Level Input Current		V_{IN} = V_{IL} (min)	0.50			μA
I_{IH}	High Level Input Current		V_{IN} = V_{IH} (max)			50	μA
I_{CBO}	Input Leakage Current		V_{IN} = 0	−10			μA
I_{CCH}	Supply Current	'2530	V_{CC} = 5.5V			30	mA
		'2531				33	
I_{OS}	Output Current Drive		V_{CC} = 5.5V, V_O = 2.25V	−50		−150	mA
I_{CCL}	Supply Current	'2530	V_{CC} = 5.5V			72	mA
		'2531				75	

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	CGS100P V_{CC} = 4.5V to 5.5V T_A = −40°C to +85°C C_L = 50 pF R_L = 500Ω			Units
		Min	Typ	Max	
f_{MAX}	Frequency Maximum	70			MHz
t_{PLH}	Low-to-High Propagation Delay CK to O_n ('2530)	3.4	5.0	7.0	ns
t_{PHL}	High-to-Low Propagation Delay CK to O_n ('2530)	3.4	5.0	7.0	ns
t_{PLH}, t_{PHL}	Propagation Delay CKn to O_n ('2531)	4.0 4.0	5.0 5.0	8.0 8.0	ns
t_{PLH}, t_{PHL}	Propagation Delay SEL to O_n ('2531)	5.0 5.0	5.0 5.0	10.0 10.0	ns

Extended AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

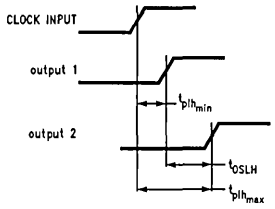
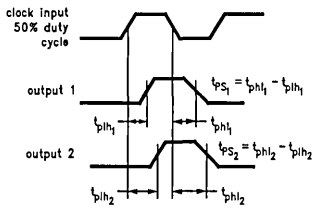
Symbol	Parameter	V_{CC} (V)*	CGS100P T_A = −40°C to +85°C C_L = 50 pF R_L = 500Ω			Units
			Min	Typ	Max	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.0		150	550	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	5.5		150	550	ps
t_{PS}	Maximum Skew Pin (Signal) Transition Variation (Note 1)	5.0		0.6	1.1	ns
t_{rise}, t_{fall}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)	5.0		1.0	1.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design. See Figures A and B of Parameter Measurement Information.

Minimum Skew Parameters

Parameter Measurement Information (Preliminary)

Definition	Example	Significance
t_{OSHL}, t_{OSLH} **Common Edge Skew:** Output Skew for HIGH-to-LOW Transitions: $t_{OSHL} = \lvert t_{PHL_{max}} - t_{PHL_{min}} \rvert$ Output Skew for LOW-to-HIGH Transitions: $t_{OSLH} = \lvert t_{PLH_{max}} - t_{PLH_{min}} \rvert$ Propagation delays are measured across the outputs of any given device.	 **FIGURE A**	• t_{OS}, Output Skew or Common Edge Skew • Skew parameter to observe propagation delay differences in applications requiring synchronous data/ clock operations.
t_{PS} **Pin Skew or Transition Skew:** $t_{PS} = \lvert t_{PHL_i} - t_{PLH_i} \rvert$ Both HIGH-to-LOW and LOW-to-HIGH propagation delays are measured at each output pin across the given device. t_{PS} is the maximum difference for outputs i = 1 to 8 within a device package.	 **FIGURE B**	• t_{PS}, Pin Skew or Transition Skew • Skew parameter to observe duty cycle degradation of any output signal (pin).