National Semiconductor

PRELIMINARY

# CGS2537V
# Commercial Quad Memory Array Clock Drivers
# CGS2537TV
# Industrial Quad Memory Array Clock Drivers

## General Description

These Clock Generation and Support clock drivers are specifically designed for driving memory arrays requiring large fanouts while operating at high speeds.

CGS2537 is a 4 to 16 inverting driver with TTL compatible I/Os. This device features the same characteristics of CGS2534 with an added series resistor on the output for ease of termination while reducing the undershoot.

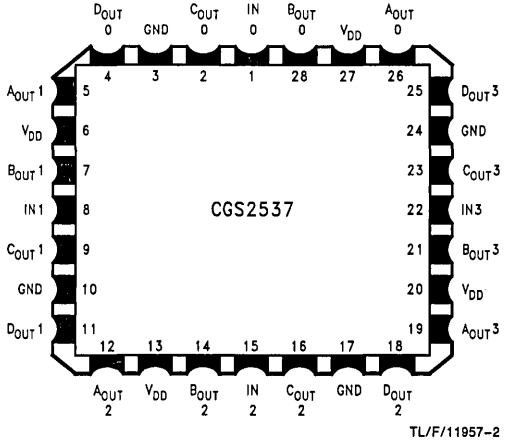
This device has minimum skew specifications of 500 ps pin-to-pin as well as a 1 ns specification for part-to-part propagation delay variation.

## Features

- Nominal 8Ω output series resistor
- Guaranteed and tested:
  — 500 ps pin-to-pin skew ($T_{OSHL}$ and $T_{OHLH}$)
- Implemented on National's ABT family process
- Output current drive:
  — −36 mA/+20 mA $I_{OH}/I_{OL}$
- Industrial temperature of −40°C to +85°C
- 28-pin PLCC for optimum skew performance
- Symmetric package orientation
- Large fanout for memory driving applications
- Guaranteed 2 kV ESD protection

## Connection Diagram

**Pin Assignment for 28-Pin PLCC**

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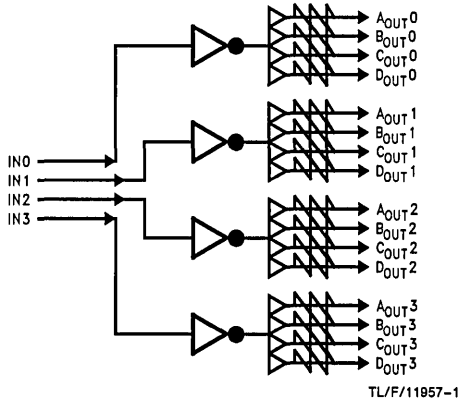
**See NS Package Number V28A**

## Logic Diagram

**CGS2537**

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## Truth Table

| Device | Input | Output |
|---|---|---|
| CGS2537 | In (0–3) | $\overline{ABCD}$ Out (0–3) |

## Absolute Maximum Ratings (Note)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 7.0V |
| Input Voltage ($V_I$) | 7.0V |
| Storage Temperature Range ($T_{stg}$) | −65°C to +150°C |
| Typical $\theta_{JA}$ Airflow | V Pack |
| 0 LFM | 62°C/W |
| 225 LFM | 43°C/W |
| 500 LFM | 34°C/W |
| 900 LFM | 27°C/W |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 4.75V to 5.25V |
| High Level Input Voltage ($V_{IH}$) | 2V |
| Low Level Input Voltage ($V_{IL}$) | 0.8V |
| High Level Output Current ($I_{OH}$) | −36 mA |
| Low Level Output Current ($I_{OL}$) | 20 mA |
| Free Air Operating Temperature | |
| Industrial | −40°C to +85°C |
| Commercial | 0°C to +70°C |

**Note:** The Absolute Maximum Rating are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

## DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at $V_{CC}$ = 5V, $T_A$ = 25°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Level Voltage | | | | 0.8 | V |
| $V_{IH}$ | Input High Level Voltage | | 2.0 | | | V |
| $V_{IK}$ | Input Clamp Voltage | $V_{CC}$ = 4.75V, $I_I$ = −18 mA | | | −1.2 | V |
| $V_{OH}$ | High Level Output Voltage | $I_{OH}$ = −3 mA, $V_{CC}$ = 4.75V | 2.4 | | | V |
| | | $I_{OH}$ = −36 mA, $V_{CC}$ = 4.75V | 2.0 | | | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = 4.75V, $I_{OL}$ = 20 mA | | 0.35 | 0.5 | V |
| | | $V_{CC}$ = 4.75V, $I_{OL}$ = 50 μA | | 0.1 | 0.1 | |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = 5.25V, $V_{IH}$ = 7V | | | 7 | μA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = 5.25V, $V_{IH}$ = 2.7V | | | 5 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = 5.25V, $V_{IL}$ = 0.4V | −5 | | | μA |
| $I_{OS}$ | Output Drive Current | $V_{CC}$ = 5.25V, $V_O$ = 0V | −100 | | 275 | mA |
| $I_{OLD}$ | Minimum Dynamic Output Current* | $V_{CC}$ = 5.25V, $V_{OLD}$ = 1.65V (max) | | 50 | 75 | mA |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | $V_{CC}$ = 5.25V | | | 3 | mA |
| $I_{CC}$ | Supply Current '2537 (Quiescent) | $V_{CC}$ = 5.25V | | | 80 | μA |
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = 5V | | 5 | | pF |

*Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at $V_{CC}$ = 5V, $T_A$ = 25°C.

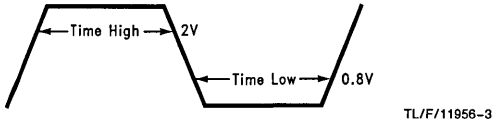
| Symbol | Parameter | $V_{CC}$* (V) | CGS2537 | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = +25°C, $C_L$ = 50 pF, $R_L$ = 500Ω | | | $T_A$ = −40 to +85°C, $C_L$ = 50 pF, $R_L$ = 500Ω | | | |
| | | | Min | Typ | Max | Min | Typ | Max | |
| $f_{max}$ | Frequency Maximum | 5.0 | | | | | 100 | | MHz |
| $t_{PLH}$ | Low-to-High Propagation Delay CK to $O_n$ | 5.0 | | | 4.0 | | | 4.0 | ns |
| $t_{PHL}$ | High-to-Low Propagation Delay CK to $O_n$ | 5.0 | | | 4.5 | | | 4.5 | ns |
| $t_{OSHL}$ | Maximum Skew Common Edge Output-to-Output Variation (Note 1) | 5.0 | | | 500 | | | 500 | ps |
| $t_{OSLH}$ | Maximum Skew Common Edge Output-to-Output Variation (Note 1) | 5.0 | | 150 | 500 | | | 500 | ps |
| $t_{rise}$, $t_{fall}$ | Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V) | | | | 1.5 | | | 1.5 | ns |
| $t_{HIGH}$ | Pulse Width Duration High | | 4 | | | 4 | | | ns |
| $t_{LOW}$ | Pulse Width Duration Low | | 4 | | | 4 | | | |
| $t_{PVLH}$ | Part-to-Part Variation of Low-to-High Transitions | 5.0 | | | 750 | | | 750 | ps |
| $t_{PVHL}$ | Part-to-Part Variation of High-to-Low Transitions | 5.0 | | | 750 | | | 750 | ps |

*Voltage Range 5.0 is 5.0V ±0.5V

**Note 1:** Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW ($t_{OSHL}$) or LOW to HIGH ($t_{OSLH}$).

Time high is measured with outputs are at 2.0V or above.
Time low is measured with outputs are at 0.8V or below.

**Timing Information**

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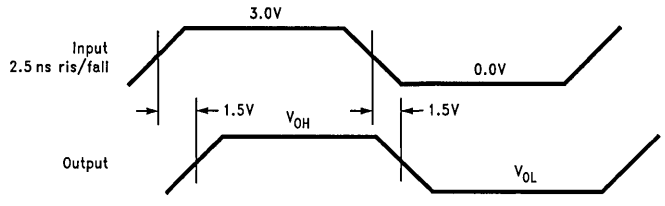


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## Memory Array Driving

In order to minimize the total load on the address bus, quite often memory arrays are being driven by buffers while having the inputs of the buffers tied together. Although this practice was feasible in the conventional memory designs, in today's high speed, large buswidth designs which require address fetching at higher speeds, this technique produces many undesired results such as cross-talk and over/undershoot.

CGS2534/35/36/37 Memory Array Drivers were designed specifically to address these application issues on high speed, large memory arrays systems.

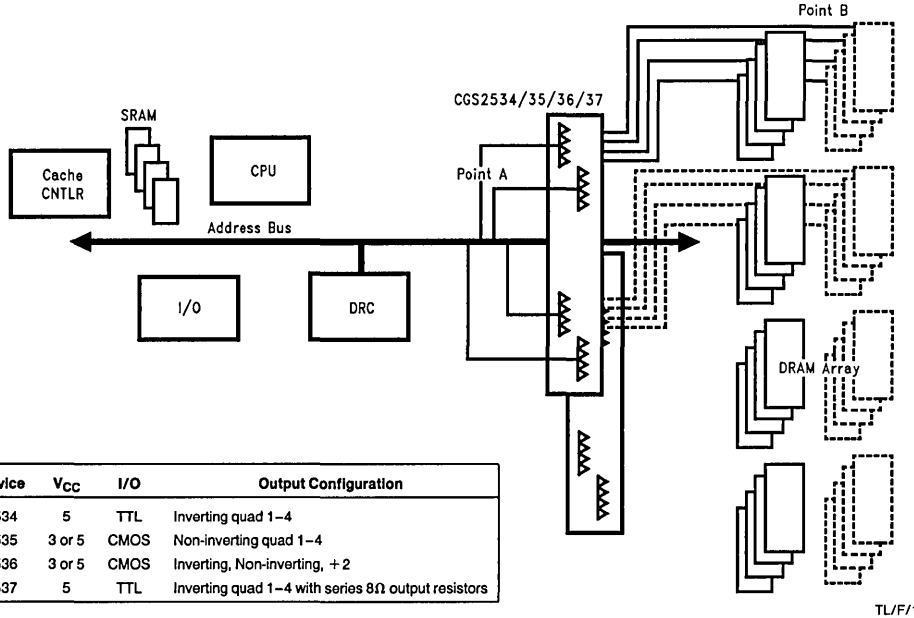
These drivers are optimized to driver large loads, with sub 3 ns propagation delays. These drivers produce less noise while reducing the total capacitive loading on the address bus by having only four inputs tied together (see the diagram below, point A). This helps to minimize the overshoot and undershoot by having only four outputs being switched simultaneously.

Also this larger fan-out helps to save board space since for every one of these MAD drivers, two conventional buffers were typically being used.

Another feature associated with these clock drivers is a 250 ps–500 ps pin-to-pin skew specification. The minimum skew specification allows high speed memory system designers to optimize the performance of their memory subsystem by operating at higher frequencies without having concerns about output-to-output (bank-to-bank) synchronization problem which are associated with driving high capacitive loads (Point B).

The diagram below depicts a "2534/35/36/37" a memory subsystem operating at high speed with large memory capacity. The address bus is common to both the memory and the CPU and I/Os.

These MAD drivers can operate beyond 150 MHz, and are also available in 3V–5V TTL/CMOS versions with symmetric 24 mA $I_{OH}/I_{OL}$ current drive.




| Device | $V_{CC}$ | I/O | Output Configuration |
|---|---|---|---|
| 2534 | 5 | TTL | Inverting quad 1–4 |
| 2535 | 3 or 5 | CMOS | Non-inverting quad 1–4 |
| 2536 | 3 or 5 | CMOS | Inverting, Non-inverting, +2 |
| 2537 | 5 | TTL | Inverting quad 1–4 with series 8Ω output resistors |

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