National Semiconductor

PRELIMINARY

CGS700V
Commercial Low Skew PLL 1 to 9 CMOS Clock Driver

General Description

CGS700 is an off the shelf clock driver specifically designed around the PowerPc™ architecture. It provides low skew outputs which are produced at different frequencies from three fixed input references. The XTALIN input pin is designed to be driven from three distinct crystal oscillators running at 25 MHz, 33 MHz or 40 MHz.

The PLL, using a charge pump and an internal loop filter, multiplies this input frequency to create a maximum output frequency of four times the input.

The device includes a TRI-STATE® control pin to disable the outputs while the PLL is still in lock. This function allows for testing the board without having to wait to acquire the lock once the testing is complete.

Also included, are two EXTSEL and EXTCLK pins to allow testing the chip via an external source. The EXTSEL pin, once set to high, causes the External-Clock_Mux to change its input from the output of the VCO and Counter to the external clock signal provided via EXTCLK input pin. CLK1SEL pin changes the output frequency of the CLK1_0, CLK1_6 outputs. During normal operation, when CLK1SEL pin is high, these outputs are at the same frequency as the input crystal oscillator, while CLK2 and CLK4 outputs are at twice and four times the input frequency respectively.
Once CLK1SEL pin is set to a low logic level, the CLK1 outputs will be at twice the input frequency, the same as the CLK2 output, with CLK4 output still being at four times the input frequency.

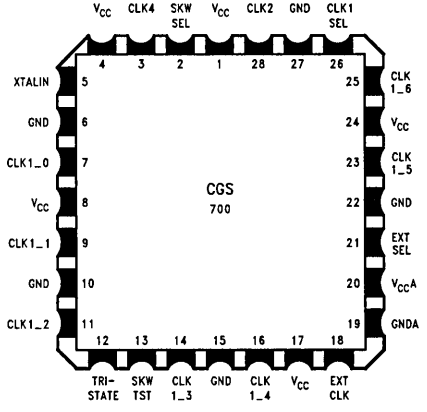
In addition two other pins are added for increasing the test capability. SKWSEL and SKWTST pins allow testing of the counter's output and skew of the output drivers by bypassing the VCO. In this test mode CLK4 frequency is the same as SKWTST input frequency, while CLK2 is ½ and CLK1 frequencies are ¼ respectively (refer to the truth table). In addition CLK1SEL functionality is also true under this test condition

Features

- Guaranteed and tested:
  - 500 ps pin-to-pin skew (t_{OSHL} and t_{OSLH}) on 1X outputs
- Output buffer of nine drivers for large fanout
- 25 MHz–160 MHz output frequency range
- Outputs operating at 4X, 2X, 1X of the reference frequency for multi-frequency bus applications
- Selectable output frequency
- TRI-STATE output control with the PLL is in the lock state
- Internal loop filter to reduce noise and jitter
- Separate analog and digital V_{CC} and Ground pins
- Low frequency test mode by disabling the PLL
- Implemented on National's Core CMOS process
- Symmetric output current drive :
  - +30 mA/−30 mA I_{OL}/I_{OH}
- 28-pin PLCC for optimum skew performance
- Guaranteed 2 kV ESD protection

Connection Diagram

Pin Assignment for PLCC



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See NS Package Number V28A

Pin Description

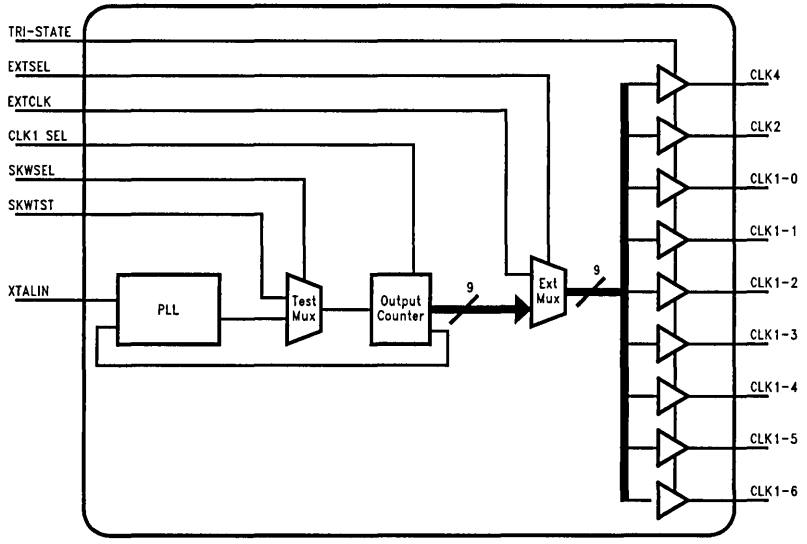
PLCC Package

Pin	Name	Description
1	V_{CC}	Digital V_{CC}
2	SKWSEL	Skew Test Selector Pin
3	CLK4	4X Clock Output
4	V_{CC}	Digital V_{CC}
5	XTALIN	Crystal Oscillator Input
6	GND	Digital Ground
7	CLK1_0	1X Clock Output
8	V_{CC}	Digital V_{CC}
9	CLK1_1	1X Clock Output
10	GND	Digital Ground
11	CLK1_2	1X Clock Output
12	TRI-STATE	Output TRI-STATE Control
13	SKWTST	Skew Testing Pin
14	CLK1_3	1X Clock Output

Pin	Name	Description
15	GND	Digital Ground
16	CLK1_4	1X Clock Output
17	V_{CC}	Digital V_{CC}
18	EXTCLK	External Test Clock
19	GNDA	Analog Ground
20	V_{CC}A	Analog V_{CC}
21	EXTSEL	External Clock Mux Selector
22	GND	Digital Ground
23	CLK1_5	1X Clock Output
24	V_{CC}	Digital V_{CC}
25	CLK1_6	1X Clock Output
26	CLK1SEL	CLK1 Multiplier Selector
27	GND	Digital Ground
28	CLK2	2X Clock Output

Block Diagram

CGS700



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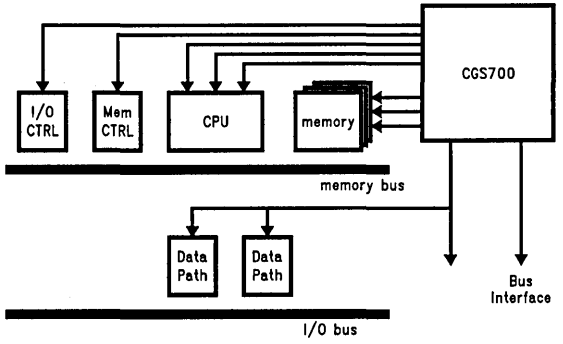
Truth Table

Input						Output		
CLK1 SEL	EXT SEL	EXT CLK	SKW SEL	SKW TST	TRI-STATE	CLK4	CLK2	CLK1
H	L	X	L	X	H	$4\times f_{IN}$	$2\times f_{IN}$	f_{IN}
L	L	X	L	X	H	$4\times f_{IN}$	$2\times f_{IN}$	$2\times f_{IN}$
X	H	⎍	X	X	H	⎍	⎍	⎍
H	L	X	H	⎍	H	$1\times f_{tst}$	$\frac{1}{2}\times f_{tst}$	$\frac{1}{4}\times f_{tst}$
L	L	X	H	⎍	H	$1\times f_{tst}$	$\frac{1}{2}\times f_{tst}$	$\frac{1}{2}\times f_{tst}$
X	X	X	X	X	L	Z	Z	Z

Typical Application



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CGS700

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage Diode Current (I_{IK})	
V = −0.5V	−20 mA
V = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_O)	
V = −0.5V	−20 mA
V = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±60 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±60 mA
Storage Temperature (T_{stg})	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Static and Dynamic) (Note 2)	1400 mW

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.

Note 2: Power dissipation is calculated using 49°/W as the thermal coefficient for the PCC package at 225 LFM airflow. The input frequency is assumed @ 33 MHz with CLK4 at 132 MHz and CLK2 and CLK1's being at 66 MHz. In addition the ambient temperature is assumed 70°C.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Input Crystal Frequency	25 MHz to 40 MHz
Operating Temperature (T_A)	0°C to +70°C
External Clock Frequency (EXTCLK Pin)	1 MHz to 10 MHz
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Crystal Input V_{in} from 0.8V to 2.0V	5 ns
All Other Inputs	50 ns

DC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	V_{CC} (V)	V_{CC} = 4.5V to 5.5V, T_A = 0°C to 70°C			Units
				Min	Typ	Max	
V_{IH}	Minimum Input High Level Voltage		4.5 5.5	2.0 2.0			V
V_{IL}	Maximum Input Low Level Voltage		4.5 5.5			0.8 0.8	V
V_{OH}	Minimum Output High Level Voltage	I_{OUT} = −50 μA	4.5 5.5	4.4 5.4	4.4 5.4		V
		I_{OH} = −30 mA	4.5 5.5	V_{CC} − 0.6 V_{CC} − 0.6			
V_{OL}	Maximum Output High Level Voltage	I_{OUT} = −50 μA	4.5 5.5			0.1 0.1	V
		I_{OL} = 30 mA	4.5 5.5			0.6 0.6	
I_{OH}	High Level Output Current	V_{OH} = V_{CC} − 1.0V	4.5	50	110	170	mA
I_{OL}	Low Level Output Current	V_{OL} = 1.0V	5.5	50	110	170	mA
I_{IN}	Leakage Current	V_{IN} = 0.4V or 4.6V	4.5 5.5	−50		50	μA
C_{IN}	Input Capacitance		4.5 5.5			10	pF
I_{CC}	Quiescent Current (No Load)	V_{IN} = V_{CC}, GND	5.5		15	100	mA
I_{CCT}	I_{CC} per TTL Input	V_{IN} = V_{CC} − 2.1, GND	5.5			2.5	mA

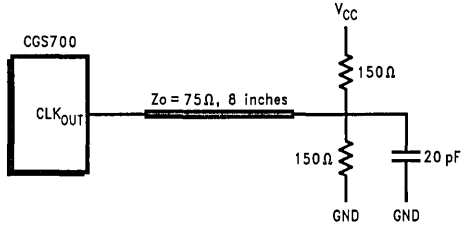
CGS700 (Continued)

AC Electrical Characteristics

Over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter			V_{CC} = 4.5V to 5.5V T_A = 0°C to 70°C C_L = Circuit 1 R_L = Circuit 1			Units
				Min	Typ	Max	
t_{rise}	Output Rise (Note 1)	CLK4 CLK2 CLK1	0.8V to 2.6V 1.0V to V_{CC} − 1.0V 1.0V to V_{CC} − 1.0V			2.0	ns
t_{fall}	Output Fall (Note 1)	CLK4 CLK2 CLK1	2.6V to 0.8V V_{CC} − 1.0V to 1.0V V_{CC} − 1.0V to 1.0V			2.0	ns
t_{skew}	Maximum Edge- to-Edge Output Skew (Note 2)	+ to + Edges + to + Edges + to + Edges	CLK1 Outputs CLK1 and CLK4 CLK2 and CLK4			500 1000 1000	ps
t_{lock}	Time to Lock the Output to the Synch Input					10.0	ms
t_{cycle}	Output Duty Cycle (Note 3)		CLK1 Outputs CLK2 Output CLK4 Output	40 40 30		60 60 70	%
Jitter	Output Jitter (Note 4)					0.4	ns

Circuit 1. Test Circuit



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Note 1: t_{rise} and t_{fall} are measured at the pin of the device.

Note 2: Skew is measured at 50% of V_{CC}.

Note 3: Output duty cycle is measured at $V_{DD}/2$.

Note 4: Jitter parameter is characterized and is guaranteed by design only. It measures the uncertainty of either the positive or the negative edge compared to its previous cycle. It is also measured at output levels of $V_{CC}/2$. Refer to *Figure 2* for further explanation.

Note 5: The GNDA pins of the 700 must be as free of noise as possible for minimum jitter. Separate analog ground plane is recommended for the PCB. Also the $V_{CC}A$ pin requires extra filtering to further reduce noise. Ferrite beads for filtering and bypass capacitors are suggested for $V_{CC}A$ pin.

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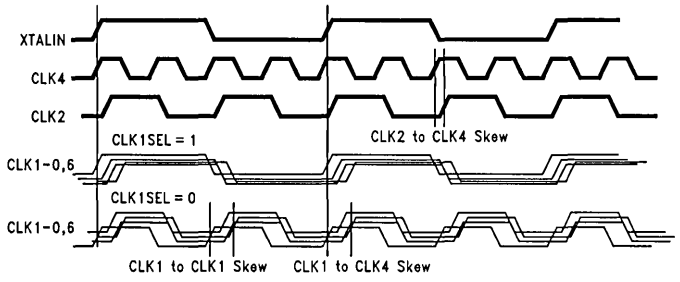

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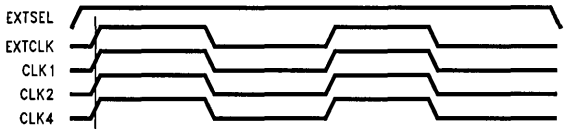

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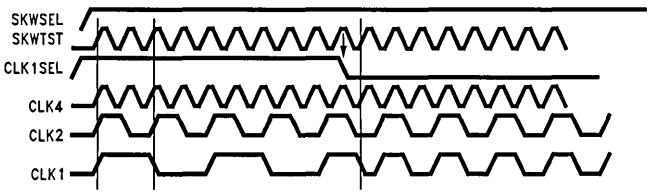

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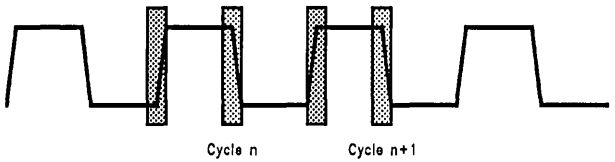
FIGURE 1. Waveforms



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P(n) − P(n+1) = ±250 ps for either the rising or falling edge.

FIGURE 2. Jitter