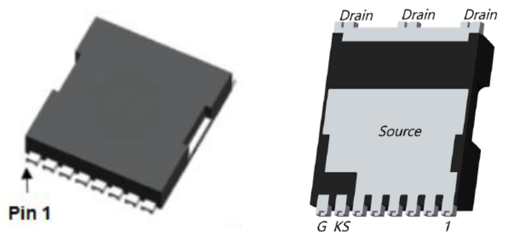
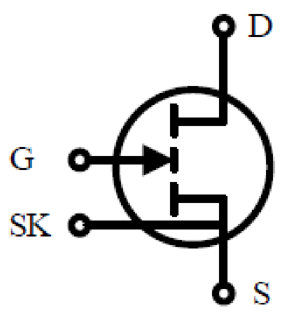
E-mode 650V, 25mΩ typ.,
GaN HEMT T1 in TOLL

Datasheet - production data

Descriptions

TOLL

GaN-on-Silcon E-mode Transistor


Key Performance Parameters

Parameters	Value	Unit
BV_{DSS}	650	V
$R_{DS(on),max}$	32	mΩ
$Q_{g,typ}$	14	nC
$I_{DS,max}$	60	A
$I_{DS,pulse}$	120	A

Features

- 650 V enhancement mode power transistor
- Ultra-low FOM
- Simple gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 / +10 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Reverse conduction capability
- Zero reverse recovery loss

Applications

- On Board Chargers
- Traction Drive
- DC-DC Converters
- Industrial Motor Drives
- Solar Inverters
- Bridgeless Totem Pole PFC

Type/Ordering Code	Package	Marking	Related Links
CGT65R032T1	**TOLL**	**65R032T1**	**See Appendix A**

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Transient Drain-to-Source Voltage (Note 1)	$V_{DS(transient)}$	900	V
Gate-to-Source Voltage	V_{GS}	-10 to + 7	V
Gate-to-Source Voltage - transient (Note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case}= 25 °C)	I_{DS}	60	A
Continuous Drain Current (T_{case}= 100 °C)	I_{DS}	41	A
Pulse Drain Current (Pulse width 10 μs, V_{GS} = 6 V) (Note 2)	$I_{DS\ Pulse}$	120	A

(1) For ≤1 μs

(2) Defined by product design and characterization. Value is not tested to full current in production.

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	0.35	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

Electrical Characteristics (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	650			V	V_{GS} = 0 V, I_{DSS} ≤ 120 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		25	32	mΩ	V_{GS} = 6 V, T_J = 25 °C I_{DS} = 18 A
Drain-to-Source On Resistance	$R_{DS(on)}$		65		mΩ	V_{GS} = 6 V, T_J = 150 °C I_{DS} = 18 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_{DS} = 16.4 mA
Gate-to-Source Current	I_{GS}		320		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 400 V, I_{DS} = 60 A
Drain-to-Source Leakage Current	I_{DSS}		4	120	µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		160		µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		1		Ω	f = 5 MHz, open drain
Input Capacitance	C_{ISS}		516		pF	V_{DS} = 400 V V_{GS} = 0 V f = 100 kHz
Output Capacitance	C_{OSS}		127		pF	
Reverse Transfer Capacitance	C_{RSS}		2.4		pF	
Effective Output Capacitance Energy Related (Note 3)	$C_{O(ER)}$		212		pF	V_{GS} = 0 V V_{DS} = 0 to 400 V
Effective Output Capacitance Time Related (Note 4)	$C_{O(TR)}$		338		pF	
Total Gate Charge	Q_G		14		nC	V_{GS} = 0 to 6 V V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		3.8		nC	
Gate-to-Drain Charge	Q_{GD}		4.1		nC	
Output Charge	Q_{OSS}		135		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(3) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

(4) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Electrical Characteristics cont'd (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		8.1		ns	V_{DD} = 400 V, V_{GS} = +6 V/-3 V I_{DS} = 20 A, $R_{G(on)}$ = 10 Ω, $R_{G(off)}$ = 2 Ω, L = 65 µH, L_P = 4 nH (Notes 5,6,7)
Rise Time	t_R		8.5		ns	
Turn-Off Delay	$t_{D(off)}$		9.8		ns	
Fall Time	t_F		7.7		ns	
Switching Energy during turn-on	E_{on}		117		µJ	
Switching Energy during turn-off	E_{off}		17.2		µJ	
Output Capacitance Stored Energy	E_{OSS}		17		µJ	V_{DS} = 400 V V_{GS} = 0 V, f = 100 kHz

(5) See Figure 16 for switching test circuit diagram.

(6) See Figure 17 for switching time definition waveforms.

(7) L_P = parasitic inductance.

Electrical Performance Graphs

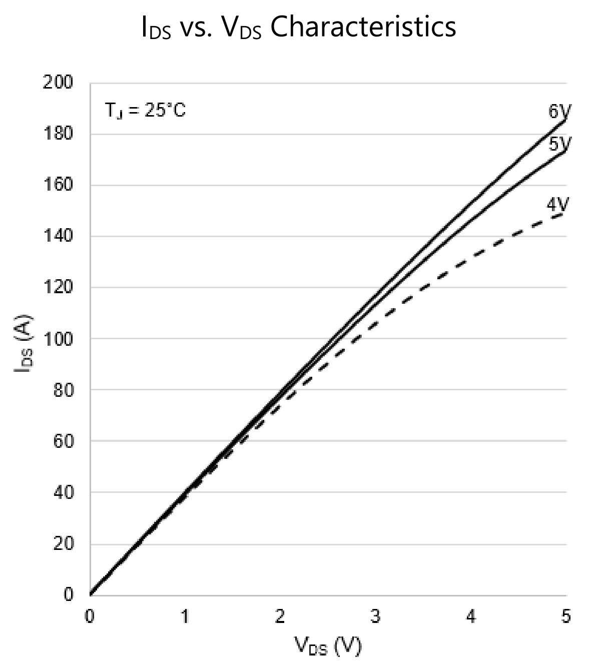


Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 ^{0}C

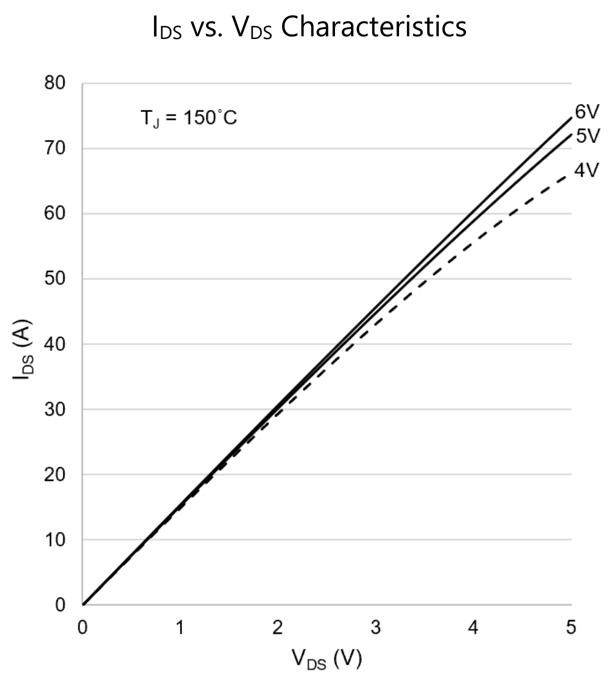


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 ^{0}C

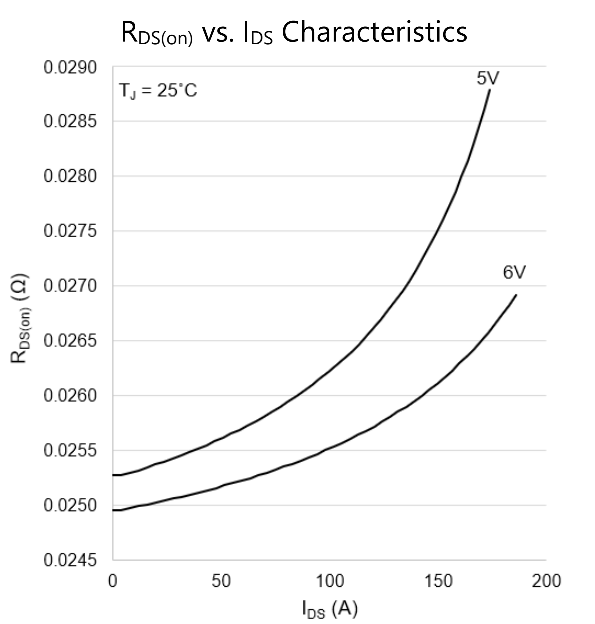


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 ^{0}C

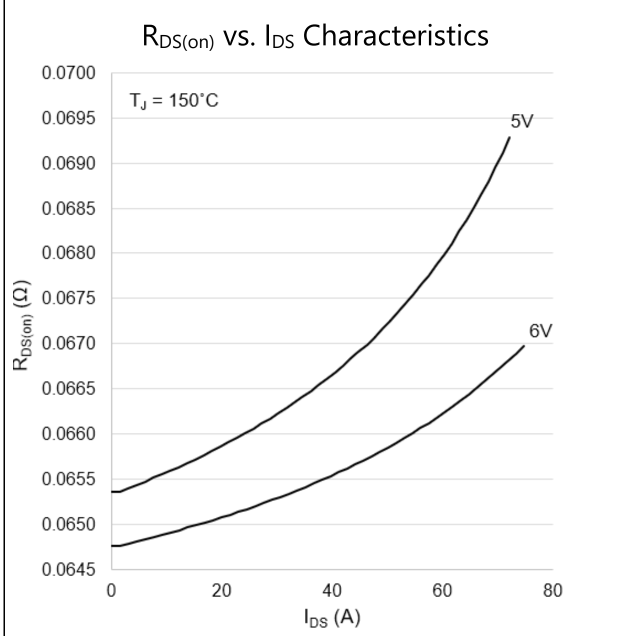


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 ^{0}C

Electrical Performance Graphs

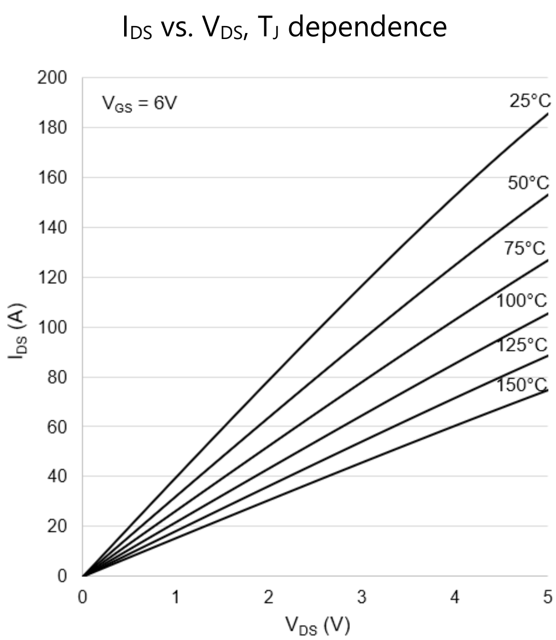


Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

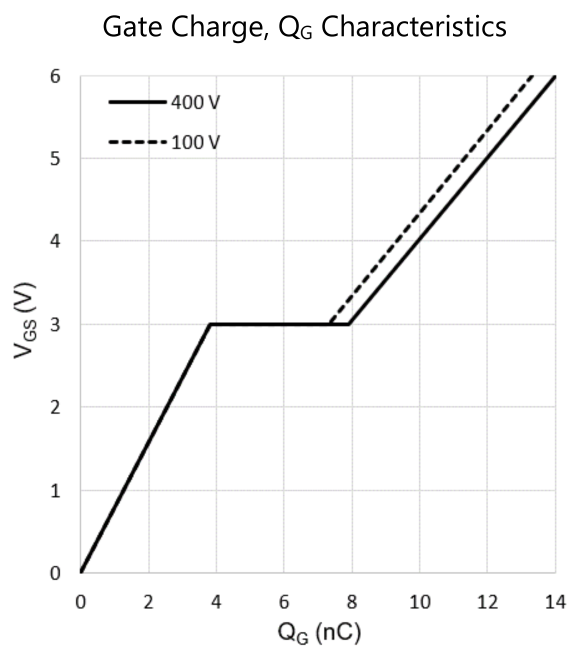


Figure 6: Typical V_{GS} vs. Q_G @ V_{DS}=100, 400V

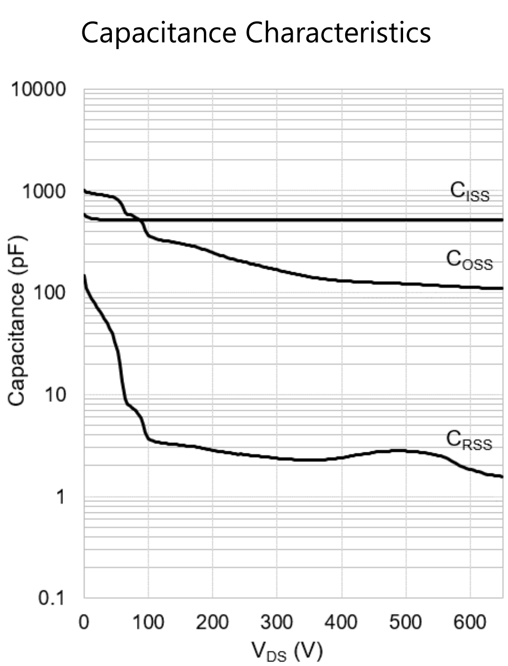


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

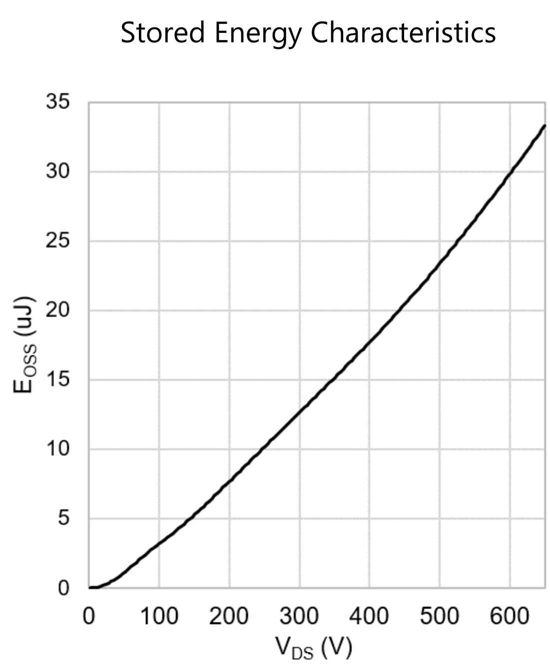


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

Reverse Conduction Characteristics

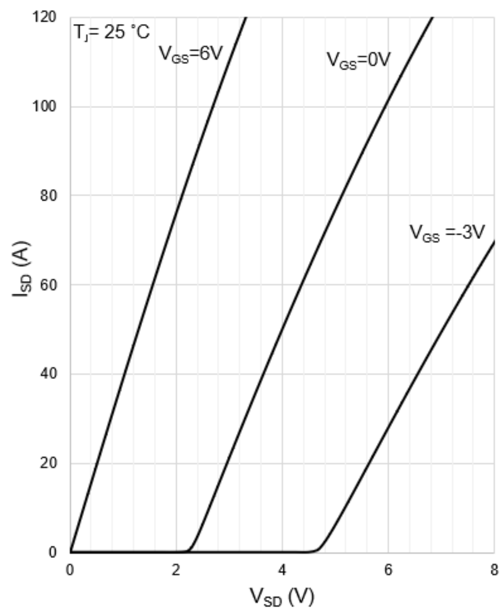


Figure 9: Typical I_{SD} vs. V_{SD} @ T_J = 25 °C

Reverse Conduction Characteristics

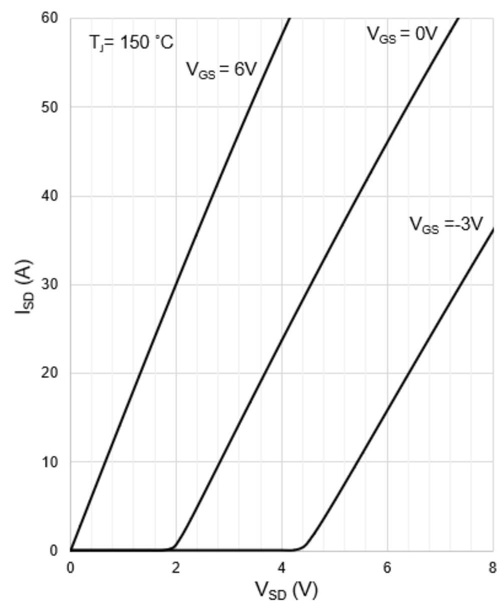


Figure 10: Typical I_{SD} vs. V_{SD} @ T_J = 150 °C

I_{DS} vs. V_{GS} Characteristics

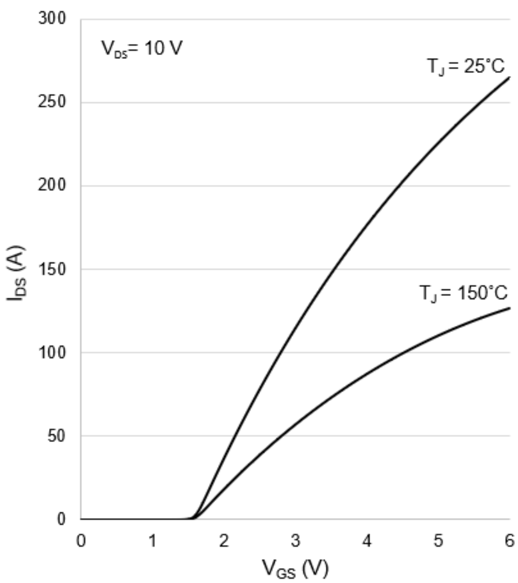


Figure 11: Typical I_{DS} vs. V_{GS}

$R_{DS(on)}$ Temperature Dependence

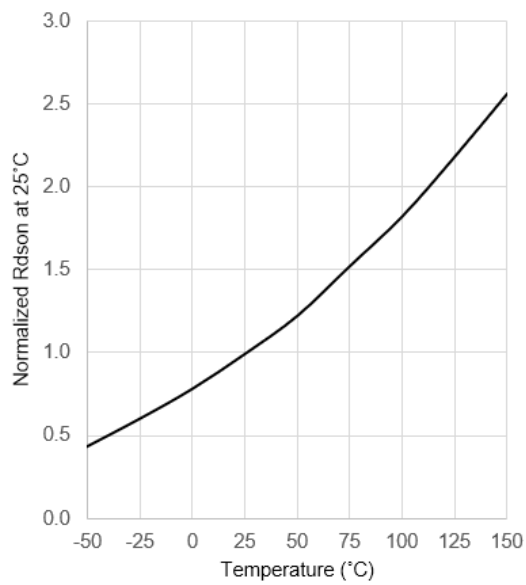


Figure12: Normalized $R_{DS(on)}$ as function of T_J

Thermal Performance Graphs

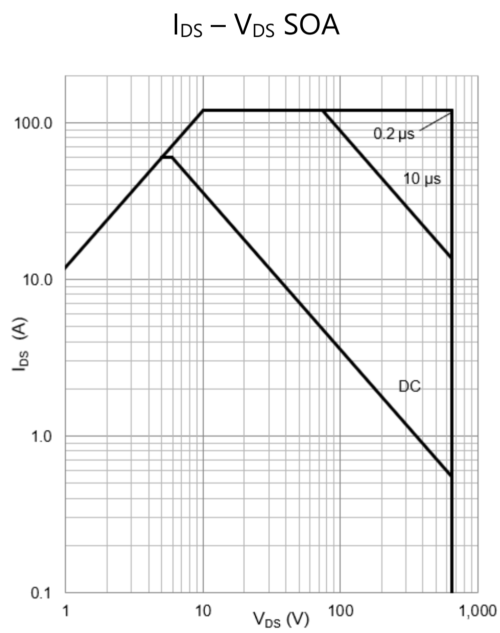


Figure 13: Safe Operating Area @ T_{case}=25°C

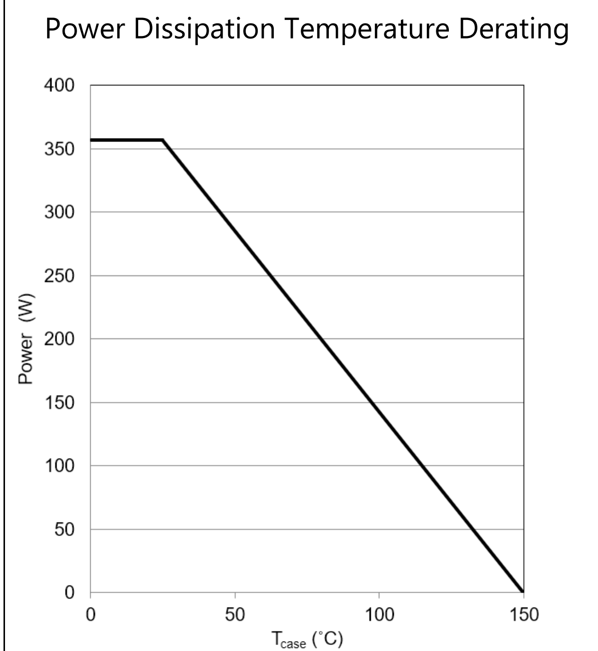


Figure 14: Power Derating vs. T_{case}

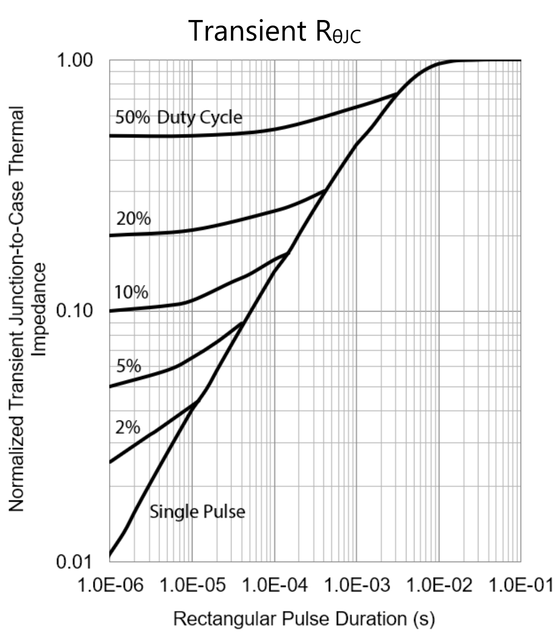


Figure 15: Transient Thermal Impedance
(1.00 = Nominal DC thermal impedance)

Test Circuits

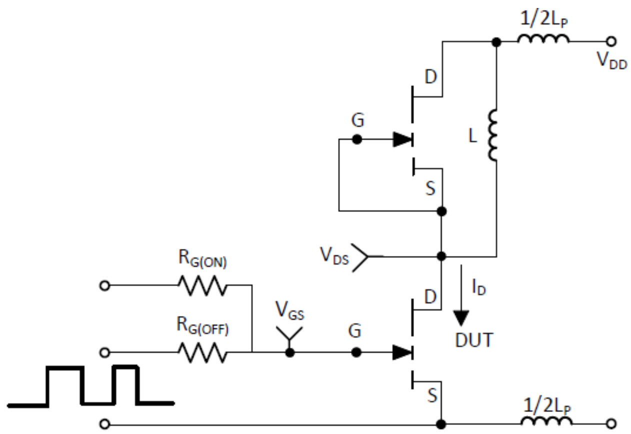


Figure 16: Switching Test Circuit

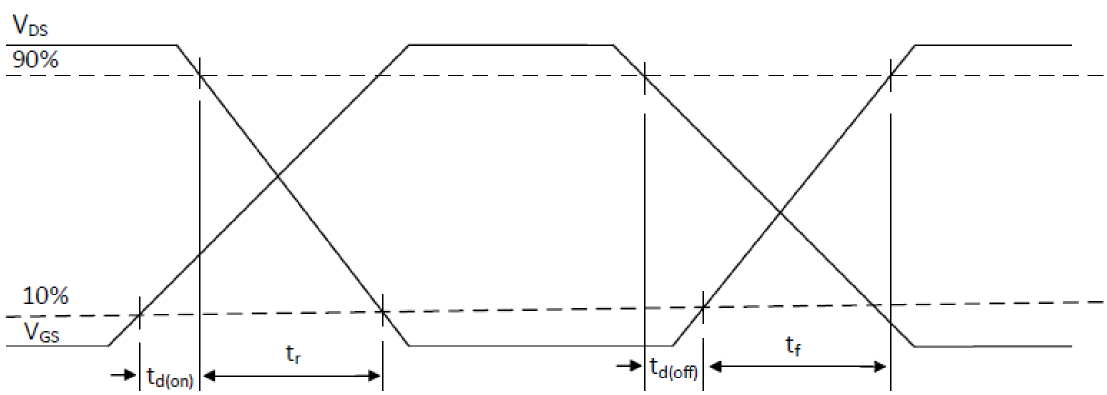


Figure 17: Switching Time Waveforms

Appendix

CoolSemi Webpage: www.coolsemi.com.