USB bus interface chip CH374

English DataSheet
Version: 2
http://wch.cn
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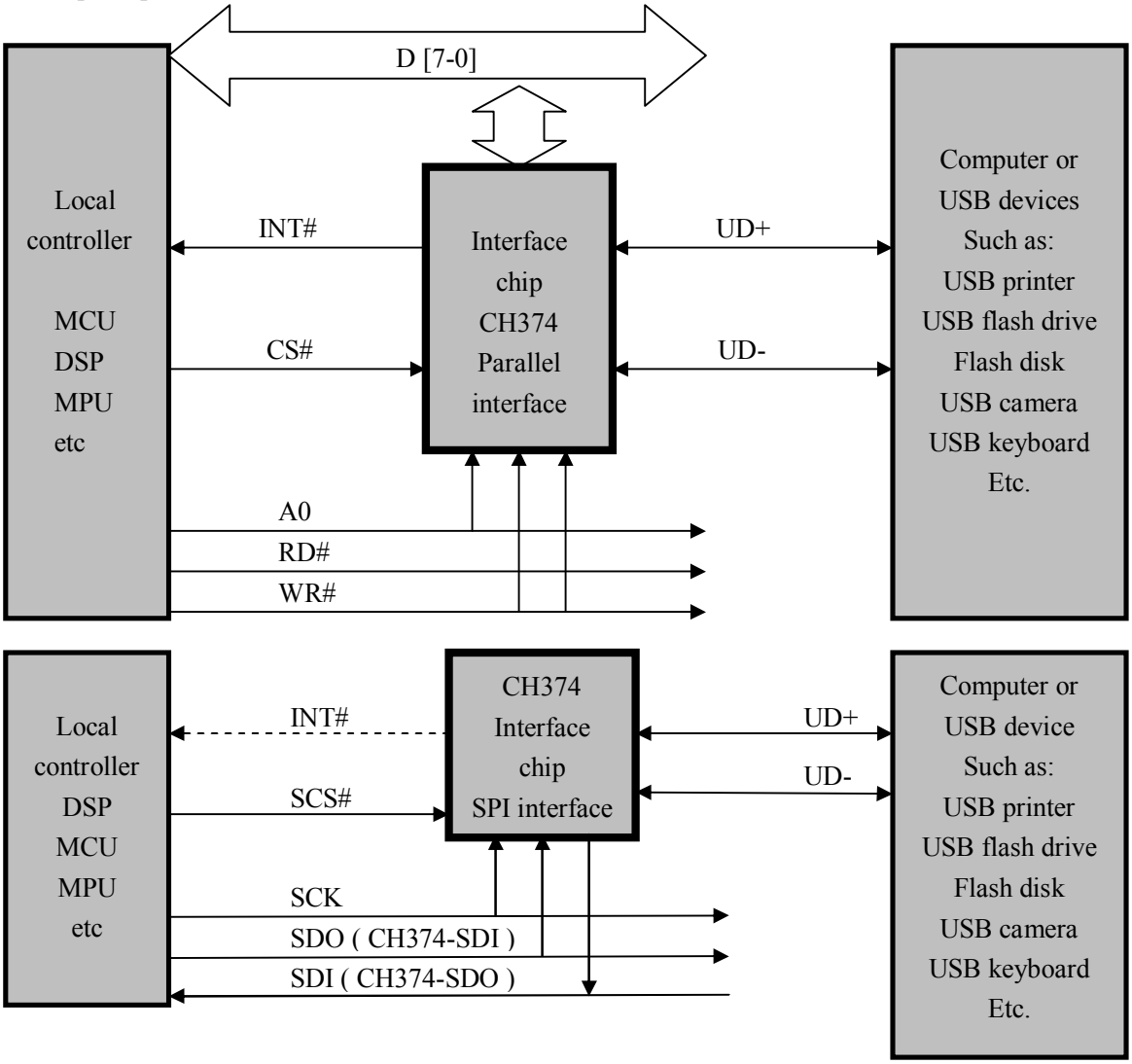
1. Introduction

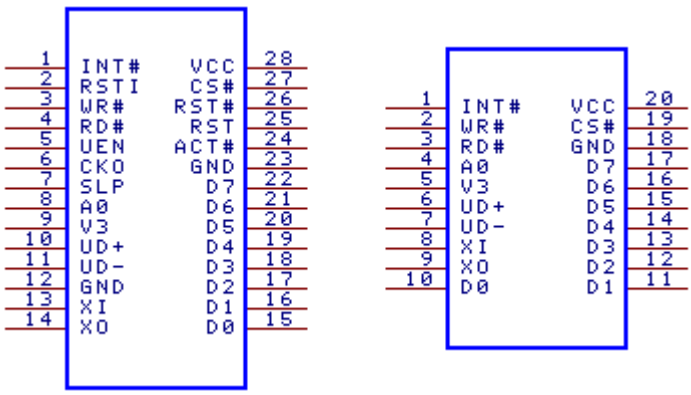
CH374 is a USB bus universal interface chip, supports both USB-HOST and USB-DEVICE/SLAVE mode. There are three ports of HUB internal. It supports low-speed and full-speed control transfer, bulk transfer, interrupt transfer and synchronous/isochronous transfer. At local, there are 8-bit data bus and read, write, chip select control wire and interrupt output in CH374.It is convenient to link CH374 to controller system bus of DSP/MCU/MPU/microprocessors (uPs). Besides, CH374 supplies SPI serial communication mode to save pins. CH374 connects to MCU/DSP/MPU through 3-wire or 4-wire SPI serial interface and interrupt output.



2. Features

● Supports low-speed of 1.5Mbps and full-speed of 12Mbps, conforms to USB Specification Version 2.0, only needs crystal and capacitor as peripherals.
● Supports USB host interface and USB device interface, and supports exchanging USB-HOST and USB-DEVICE mode dynamically.
● CH374U has 3 ports of ROOT-HUB internal, and supports 3 USB devices.
● Supports control transfer, bulk transfer, interrupt transfer and synchronous/isochronous transfer of USB device with common low-speed and full-speed.
● Automatically detects connection and disconnection of either low-speed or full-speed device, and gives out interrupt information.
● Sets impedance matching serial resistor of USB signal wire, pull-up resistor of USB device endpoint and pull-down resistor of USB host endpoint internal.
● Two kinds MCU interface are optional: 8-bit passive parallel interface with 6MB and SPI serial interface with 2.7MB/22MHz.
● Parallel interface contains 8-bit data bus, 1-bit address wire and 3-wire to control. The control wires are chip select input wire, write strobe wire and read strobe wire which is optional.
● Parallel interface only occupies 2-bit address: index address port and data port. After reading and writing data port, internal index address increases automatically.
● SPI serial interface contains SPI chip select, serial clock, serial input/output, and supports parallel connecting input to output of SPI.
● Interrupt output pin is optional connection, and active with low-level. Detection of interrupt flag in register can replace of interrupt output pin.
● Supplies assistant function: programmable clock output, power on reset output and optional watchdog reset.
● Supplies USB flash driver file layer subprogram congregation that supports FAT12/FAT16/FAT32 to realize MCU reads and writes file in USB flash drive.
● Supports source voltage of 5V and 3.3V.
● Supplies SOP-28, SSOP-20, SSOP-24 and SOP-16 lead free package which are compatible with RoHS, and DIP28 swap board is also supplied. The pins basically compatible with CH375 and CH372.

3. Package



Package shape	Width of plastic		Pitch of Pin		Instruction of package	Ordering type
SOP-28	7.62mm	300mil	1.27mm	50mil	Small outline package of 28-pin	CH374S
SSOP-20	5.30mm	209mil	0.65mm	25mil	Shrink small outline package of 20-pin	CH374T

The packages, HUB pins and HUB registers of CH374U and CH374G can consult the second DataSheet.

4. Pins

SOP28 Pin NO. (SSOP20 Pin)	Name	Type	Pin Description
28 (20)	VCC	POWER	Positive power input port, requires an external 0.1uF power decoupling capacitance
12, 23 (18)	GND	POWER	Public ground, ground connection for USB
9 (5)	V3	POWER	Attachment of VCC input external power while 3.3V;connects of 0.01uF decoupling capacitance outside while 5V
13 (8)	XI	IN	Input of crystal oscillator, attachment of crystal and crystal oscillator capacitance outside
14 (9)	XO	OUT	Opposite output of crystal oscillator, attachment of crystal and crystal oscillator capacitance outside
10 (6)	UD+	USB signal	USB Data Signal plus
11 (7)	UD-	USB signal	USB Data Signal minus
22~15 (17~10)	D7~D0	Bi-directional tri-state	8-bit bi-directional data bus, set up pull-up resistor internal, D3 also is SCS# of SPI interface, D5 also is SCK, D6 also is SDI, D7 also is SD0
4 (3)	RD#	IN	Read Strobe Input, LOW active, with pull-up resistor
3 (2)	WR#	IN	Write Strobe Input, LOW active, with pull-up resistor
27 (19)	CS#	IN	LOW active CH374 chip select, with pull-up resistor
1 (1)	INT#	Open drain OUT	Interrupter request output, low-level active, with pull-up resistor
8 (4)	A0	IN	Address wire input to identify index port and data port, with feeble pull-up resistance, A0=1,write index address; A0=0,read/write data
24 (no)	ACT#	Open drain OUT	Output USB transfer or active state in USB-DEVICE, output USB device connection state in USB-HOST, low-level active, with pull-up resistor
5 (no)	UEN	IN	USB signal UD+/UD- enable output, with pull-down resistor
6 (no)	CKO	OUT	Programmable clock output, must be left suspend when not using and cut down the connection wire as short as possible
2 (no)	RSTI	IN	External reset input, high level active, with pull-down resistor
25 (no)	RST	OUT	Output when power on reset and external reset, high level active
26 (no)	RST#	OUT	Output when power on reset and external reset, low level active
7 (no)	SLP	OUT	Output sleeping state, high level active

5. Register

The MCU appears in this manual basically apply to DSP or SCM/MCU/MPU/CPU etc.

The internal register and buffer configuration in CH374 is from address 00H to 0FFH, and they can be access to after MCU searching address. Binary system numbers can express the default data after reset, and many character symbols can explain their characteristics. The character symbols are as following:

0: after reset is always 0;

1: after reset is always 1;

X: The bit is automatically set by internal hardware or effects by external pin state;

=: reset has no effect on data, and the initial value is uncertain.

?: reserved bit, the read data have no meaning, must be write as 1 or keep former value.

Note: effect by interpretation custom, some professional terms come from English USB specification may have many similar Chinese terms.

Address scope Hexadecimal system	Register name (gray) Bit name of register	Register note (gray) Bit note of register	Default value after software and hardware reset
00H-03H	Reserved	Forbid read and write	????????
04H	REG_SYS_INFO	System information register, read only	XXX?XX01
04H bit 7	BIT_INFO_POWER_RST	Complete state of hardware power-up reset: 0=reset; 1= finish reset	0/X
04H bit 6	BIT_INFO_WAKE_UP	Chip wake up state, no effect by software reset: 0=sleep or during wake up; 1= has woke up	X
04H bit 5	BIT_INFO_SOF_PRES	Hardware 1mS timing cycle state, in HOST mode, 1= will generate SOF	=/X
04H bit 4	Reserved	Read data has no meaning and uncertain	?
04H bit 3	BIT_INFO_USB_DP	Logical level state of USB bus UD+	X
04H bit 2	BIT_INFO_USB_DM	Logical level state of USB bus UD-	X
04H bit 1 04H bit 0	Hardware identification bit	Immobility value, usually as constant 01, used to detect hardware connection is right and read operation successful	01
05H	REG_SYS_CTRL	System control register, no effected by software reset	00000000
05H bit 7	Reserved	Read data has no meaning and must be written as 0	0/?
05H bit 6	BIT_CTRL_OE_POLAR	USB output enable polarity of UEN: 0=high level enable, UEN is low forbids UD+/- output; 1=low level enable, UEN is high forbids UD+/- output	0
05H bit 5	BIT_CTRL_INT_PULSE	INT# interrupt output manner:0=low level interrupt until clear relevant interrupt flag; 1=low level pulse interrupt	0
05H bit 4	BIT_CTRL_WATCH_DOG	Watchdog reset enable of RST and RST#:0=forbid, supplies power-up reset only,	0

		no watchdog reset; 1=start, can not be forbidden after start unless hardware reset	
05H bit 3	BIT_CTRL_RESET_NOW	Control chip software reset: 1=no reset; 1=reset	0
05H bit 2	BIT_CTRL_USB_POWER	USB power adjustor control for V3: 0=start, generate USB power from 5V power of VCC; 1=forbid, external input power from V3	0
05H bit 1	Reserved	Read data has no meaning and must be written as 0	0/?
05H bit 0	BIT_CTRL_OSCIL_OFF	Control clock oscillator :0=allow oscillate; 1=stop oscillate	0
06H	REG_USB_SETUP	USB configuration register	00000000
06H bit 7	BIT_SETP_HOST_MODE	USB mode: 0=device mode; 1= host mode	0
06H bit 6	BIT_SETP_LED_ACT	Active event of ACT# LOW in device mode: 0=receive and transfer process; 1=USB host activity	0
06H bit 6	BIT_SETP_AUTO_SOF	In host mode, automatically generate SOF enable: 0=forbid; 1=allow, automatically timing send SOF	0
06H bit5 06H bit 4	BIT_SETP_USB_SPEED	USB bus speed:00=full speed mode 12Mbps; 11=low speed mode 1.5Mbps; other value is forbidden	00
06H bit 3 06H bit 2	BIT_SETP_RAM_MODE	Apply manner of spare buffer:00= forbid using spare buffer; 01= connect to receive buffer to receive 128 bytes successively and the start address is RAM_ENDP2_EXCH/RAM_HOST_EXCH; 10=successively transfer the second buffer, and the synchronous flag is 1 indicates pitch on; 11=successively receive the second buffer and the synchronous flag is 1 indicates pitch on	00
06H bit 1	BIT_SETP_PULLUP_EN	In device mode control the USB pull-up resistor: 0=forbid using pull-up resistor; 1=using pull-up resistor/connection	0
06H bit 0	BIT_SETP_TRANS_EN	USB device transfer enable in device mode: 0=forbid; 1=allow, use USB device/allow receive and transfer	0
06H bit 1 06H bit 0	BIT_SETP_BUS_CTRL	Control USB bus state in host mode;00=normal/idle;01= low UD+ low UD-(bus reset); 10=forbid; 11=low UD+ high UD-(bus resume)	00
07H	REG_INTER_EN	Interrupt enable register contain programmable clock set	11110000
07H bit 7 to bit	BIT_IE_CLK_OUT_DIV	Programmable clock detach frequency	1111

4		devisor: output frequency =(48MHz/(the data +1)), e.g. 0001=24MHz; 0010=16MHz; 1111=3MHz	
07H bit 3	BIT_IE_USB_RESUME	USB bus resume/wake up interrupt enable:0= enable chip wake up complete interrupt BIT_IF_WAKE_UP; 1= enable USB bus resume interrupt BIT_IF_USB_RESUME	0
07H bit 2	BIT_IE_USB_SUSPEND	USB bus suspend interrupt enable: 0=forbid; 1=allow, output from INT#	0
07H bit 1	BIT_IE_BUS_RESET	USB bus reset interrupt enable in device mode: 0=forbid; 1= allow, output from INT#	0
07H bit 1	BIT_IE_DEV_DETECT	USB device detect interrupt enable in device mode:0=forbid; 1=allow, output from INT#	0
07H bit 0	BIT_IE_TRANSFER	USB transfer finish interrupt enable: 0=forbid; 1= allow, output from INT#	0
08H	REG_USB_ADDR	USB device address register	00000000
08H bit 7	Reserved	Read data has no meaning and must be written as 0	0/?
08H bit 6 to bit 0	BIT_ADDR_USB_DEV	In device mode, as USB device address, in host mode, as current working USB device address	0000000
09H	REG_INTER_FLAG	Interrupt flag register, read only	XXX00000
09H bit 7	BIT_IF_USB_DX_IN	Sampling state of full speed UD+/low speed UD-:0=low level/speed lose match; 1=high level/speed match	X
09H bit 6	BIT_IF_USB_OE	USB output enable state input from UEN:0=UEN is low level; 1= UEN is high level	X
09H bit 5	BIT_IF_DEV_ATTACH	Current connection state of USB device: 0= disconnect any USB device/cut/pull out; 1=has connected one USB device at least/insert	=/X
09H bit 4	BIT_IF_USB_PAUSE	USB transfer pause flag, active with 1, write 1 to the bit can clear flag, after USB transfer automatically set as 1	0/X
09H bit 3	BIT_IF_WAKE_UP	Chip wake-up finish interrupt flag, active with 1, write 1 to the bit can clear the flag, after chip waking up automatically set as 1	0/X
09H bit 3	BIT_IF_USB_RESUME	USB bus resume/wake-up interrupt flag, active with 1, write 1 to the bit can clear the flag, after detecting USB bus resume automatically set as 1	0/X
09H bit 2	BIT_IF_USB_SUSPEND	USB bus suspend interrupt flag, active with 1, write 1 to the bit can clear flag, after detecting USB bus suspend automatically set as 1	0/X

09H bit 1	BIT_IF_BUS_RESET	USB bus reset interrupt flag in device mode, active with 1, write 1 to the bit can clear flag, after detecting USB bus reset automatically set as 1	0/X
09H bit 1	BIT_IF_DEV_DETECT	Detection of USB device insert state in host mode, active with 1, write 1 to the bit can clear flag, after detecting USB device insert or draw automatically set as 1	0/X
09H bit 0	BIT_IF_TRANSFER	USB transfer finish interrupt flag, active with 1, write 1 to the bit can clear flag, after finishing each USB transfer automatically set as 1	0/X
0AH	REG_USB_STATUS	USB state register, read only, usually query after detecting relative interrupt only	1XXXXXXX
0AH bit 7	BIT_STAT_SIE_FREE	Current SIE state: 0=busy/transferring;1=idle /wait	1/X
0AH bit 6	BIT_STAT_SUSPEND	Current USB bus suspend state:0= activity on bus;1= bus suspend	X
0AH bit 5	BIT_STAT_BUS_RESET	On device mode, current USB bus reset state:0= USB bus is idle/normal/no reset; 1=USB bus is reset	X
0AH bit 4	BIT_STAT_TOG_MATCH	Inform current receive data package whether synchronous or not:0= asynchronous; 1=synchronous	X
0AH bit 3 0AH bit 2	BIT_STAT_THIS_PID	USB transfer transaction/token PID in device mode: 00= OUT transaction; 01=reserve/accident; 10= IN transaction; 11=SETUP transaction	XX
0AH bit 1 0AH bit 0	BIT_STAT_THIS_ENDP	Aim endpoint number of USB transfer in device mode: 00= endpoint 0; 01= endpoint 1; 10= endpoint 2; 11= reserved/accident	XX
0AH bit 3 to bit 0	BIT_STAT_DEV_RESP	Response PID of USB device in host mode:0010=device response to OUT/SETUP with ACK;1010=device response to IN/OUT/SETUP with NAK; 1110=device response to IN/OUT/SETUP with STALL; 0011=device response to IN with DATA0; 1011=device response to IN with DATA1; XX00=device acknowledge is error or time over without acknowledge; other value=illegal acknowledge/accident	XXXX
0BH	REG_USB_LENGTH	USB size register, read only/write only, read receive size of current USB transfer, in device mode, write endpoint 2 transfer size of USB, in host mode, write host transfer size of USB	XXXXXXXX

0CH	REG_USB_ENDP0	In device mode, control register of USB endpoint 0	00000000
0CH bit 7	BIT_EP0_RECV_TOG	Endpoint 0 receive synchronous flag: 0=DATA0; 1=DATA1	0
0CH bit 6	BIT_EP0_TRAN_TOG	Endpoint 0 transfer synchronous flag: 0=DATA0; 1=DATA1	0
0CH bit 5 0CH bit 4	BIT_EP0_RECV_RESP	Endpoint 0 receive respond to OUT transaction: 00=acknowledge ACK; 01=forbid; 10=acknowledge NAK; 11=acknowledge STALL	00
0CH bit 3 to bit 0	BIT_EP0_TRAN_RESP	Endpoint 0 transfer respond to IN: 0000 to 1000=acknowledge data length from 0 to 8; 1110=acknowledge NAK; 1111=acknowledge STALL; other value=forbid	0000
0DH	REG_USB_ENDP1	USB endpoint 1 control register in device mode	========
0DH bit 7	BIT_EP1_RECV_TOG	Endpoint 1 receive synchronous flag: 0=DATA0; 1=DATA1	=
0DH bit 6	BIT_EP1_TRAN_TOG	Endpoint 1 transfer synchronous flag: 0=DATA0; 1=DATA1	=
0DH bit 5 0DH bit 4	BIT_EP1_RECV_RESP	Endpoint 1 receive respond to OUT transaction: 00=acknowledge ACK; 01=forbid; 10=acknowledge NAK; 11=acknowledge STALL	=
0DH bit 3 to bit 0	BIT_EP1_TRAN_RESP	Endpoint 1 transfer respond to IN: 0000 to 1000=acknowledge data length from 0 to 8; 1110=acknowledge NAK; 1111=acknowledge STALL; other value=forbid	====
0EH	REG_USB_ENDP2	USB endpoint 2 control register in device mode	00000000
0EH bit 7	BIT_EP2_RECV_TOG	Endpoint 2 receive synchronous flag: 0=DATA0; 1=DATA1	0
0EH bit 6	BIT_EP2_TRAN_TOG	Endpoint 2 transfer synchronous flag: 0=DATA0; 1=DATA1	0
0EH bit 5 0EH bit 4	BIT_EP2_RECV_RESP	Endpoint 2 receive respond to OUT transaction: 00=acknowledge ACK; 01=synchronous/isochronous transfer; 10=acknowledge NAK; 11=acknowledge STALL	00
0EH bit 3	Reserved	Read data has no meaning and must be written as 0	0/?
0EH bit 2	Reserved	Read data has no meaning and must be written as 0	0/?
0EH bit 1 0EH bit 0	BIT_EP2_TRAN_RESP	Endpoint 2 transfer respond to IN: 00=acknowledge	00

		DATA0/DATA1;01=synchronous/ isochronous transfer; 10=acknowledge NAK; 11= acknowledge STALL	
0DH	REG_USB_H_TOKEN	In host mode, USB host token register	========
0DH bit 7 to bit 4	BIT_HOST_PID_TOKEN	Appoint transaction/token PID: 1101=SETUP;0001=OUT; 1001=IN; 0101=SOF; other value=forbid. Note: no interrupt after finishing SOF, detects SIE state	====
0DH bit 3 to bit 0	BIT_HOST_PID_ENDP	Appoint be operated aim endpoint number: 0000 to 1111= endpoint from 0 to 15	====
0EH	REG_USB_H_CTRL	In USB host mode, USB host control register	00000000
0EH bit 7	BIT_HOST_RECV_TOG	Host receive synchronous flag:0=DATA0; 1=DATA1	0
0EH bit 6	BIT_HOST_TRAN_TOG	Host transfer synchronous flag: 0=DATA0; 1=DATA1	0
0EH bit 5	Reserved	Read data has no meaning and must be written as 0	0/?
0EH bit 4	BIT_HOST_RECV_ISO	Transfer type of host receive: 0=control/bulk /interrupt transfer; 1=synchronous/isochronous transfer	0
0EH bit 3	BIT_HOST_START	Control host transfer start: 0=pause; 1=start transfer, after finishing clear as 0	0
0EH bit 2	Reserved	Read data has no meaning and must be written as 0	0/?
0EH bit 1	Reserved	Read data has no meaning and must be written as 0	0/?
0EH bit 0	BIT_HOST_TRAN_ISO	Transfer type of host transfer: 0=control/bulk /interrupt transfer; 1=synchronous/isochronous transfer	0
0FH-1FH	Reserved	Forbid read and write	????????
20H-27H	RAM_ENDP0_TRAN	Endpoint 0 transfer buffer in USB device mode	========
28H-2FH	RAM_ENDP0_RECV	Endpoint 0 receive buffer in USB device mode	========
30H-37H	RAM_ENDP1_TRAN	Endpoint 1 transfer buffer in USB device mode	========
38H-3FH	RAM_ENDP1_RECV	Endpoint 1 receive buffer in USB device mode	========
40H-7FH	RAM_ENDP2_TRAN	Endpoint 2 transfer buffer in USB device mode	========
C0H-FFH	RAM_ENDP2_RECV	Endpoint 2 receive buffer in USB device mode	========
80H-BFH	RAM_ENDP2_EXCH	Endpoint 2 spare buffer in USB device mode	========
40-7FH	RAM_HOST_TRAN	Transfer buffer in USB host mode	========

C0-FFH	RAM_HOST_RECV	Receive buffer in USB host mode	========
80H-BFH	RAM_HOST_EXCH	Spare buffer in USB host mode	========

6. Function explanation

6.1. MCU interface

CH374 supplies universal 8-bit passive parallel interface and SPI synchronous serial interface at location (CH374G only support SPI interface). CH374 will sample state of CS#, WR# and RD# during power-up reset period. If WR# and RD# are low-level or connect to ground besides CS# is high-level or connect to positive power, then chooses SPI serial interface, otherwise chooses parallel interface.

The output interrupt request of INT# in CH374 active with low-level in default, and INT# can connect to interrupt input pin of MCU or common input pin. The MCU may use interrupt manner or detection manner to obtain interrupt request of CH374. To save pins, the MCU can not connect to INT# of CH374 but query interrupt flag register REG_INTER_FLAG in CH374 to obtain interrupt.

6.2. Parallel interface

Parallel interface signal wires contain: 8-bit bi-directional data bus D7 to D0, read strobe input pin RD#, write strobe input pin WR#, chip select input pin CS# and address input pin A0. CH374 is convenient to connect to various 8-bit CPU, DSP and MCU system bus besides coexists with many peripheral equipments through passive parallel interface.

CS# in CH374 is driven by address decoding circuit, be used to select peripheral equipments.

For MCU which are similar to Intel parallel time sequence, the RD# and WR# of CH374 can respectively connect to read strobe output pin and write strobe output pin in MCU. For MCU which are similar to Motorola parallel time sequence, the RD# must connect to low-level and WR# must connect to read /write direction output pin R/-W in MCU.

The following is true value table of parallel interface I/O (pay no attention to X bit, Z indicates CH374 tri-state is forbidden).

CS#	WR#	RD#	A0	D7-D0	Practical operation for CH374
1	0	0	X	X/Z	Sample when CH374 power-up reset, used to select SPI interface mode
1	X	X	X	X/Z	Not select CH374, carry out no operation
0	1	1	X	X/Z	Select but no operation, carry out no operation
0	0	1/X	1	IN	Write index address to CH374, i.e. the start address of read/write operation
0	0	1/X	0	IN	Write data to specified address, after finishing it increase index address to successive write
0	1	0	0	OUT	Read data from specified address, after finishing it increase index address to successive read
0	1	0	1	OUT	Read data from specified address, no change to index address, easily to write return after modifying

CH374 occupies 2-bit of address. When A0 is high-level selects index address endpoint to write new index address or read data but keep index address no change. When A0 is low-level selects data endpoint to read and write data corresponding to index address. After reading and writing increases index address automatically to write next data easily. The process of reading from and writing to CH374 through 8-bit

parallel interface is as following: write index address to index address endpoint and read or write several data successively.

6.3. SPI Serial interface

SPI synchronous serial interface signal wires contain: SPI chip select pin SCS#, serial clock input pin SCK, serial data input pin SDI and serial data output pin SDO. Through SPI serial interface, CH374 is convenient to connect to SPI serial bus of various MPU, DSP and MCU while using lesser connections. It can also links point-to-point for further distance.

The SCS# is driven by SPI chip select pin or common output pin of MCU. SCK in CH374 is driven by SPI clock output pin SCK of MCU. SDI is driven by SPI data output pin SDO. SDO pin connects to SPI data input pin SDI of MCU. The recommend to set hardware SPI interface is CPOL=CPHA=0 or CPOL=CPHA=1.

The SPI interface in CH374 supports MCU to use common I/O pin to simulate SPI interface to communicate. SDO in CH374 is tri-state output pin, and only to output after receiving read operation. The SDO and SDI in CH374 can parallel connect to link to bi-direction I/O pin of MCU to save pins. One recommendation is serial connecting several hundreds ohmic resistor to SDO in CH374 then parallel connects to SDI pin.

SPI in CH374 supports SPI mode 0 and mode 3. CH374 is always input data in rising edge of the SPI clock SCK, and output data in falling edge of SCK when allowing output. The list of data is high bit is before and count 8 bit as one byte.

The operation process of SPI is following:

① MCU generates SPI chip select signal of CH374, active with low;

② MCU sends one byte address code according to SPI output mode to appoint the initiative address of read and write operation.

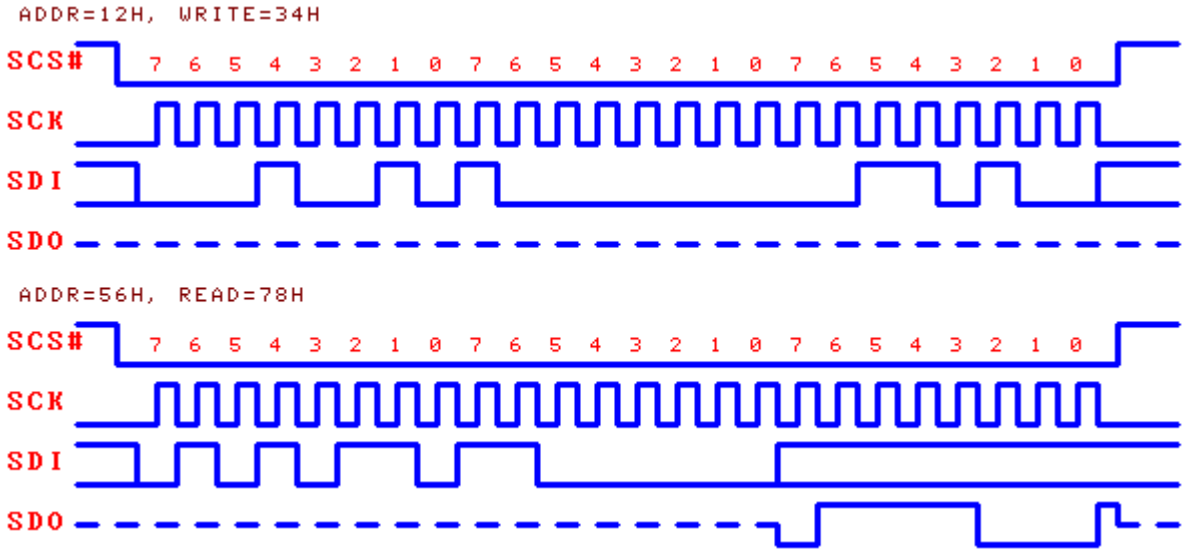
③ MCU sends one byte command code to appoint operation direction. The read command code is C0H and the write command code is 80H;

④ If the operation is Write, MCU sends one byte waited data, address automatically increase after CH374 receiving data and saving it to appointed address. Then MCU continues to send one byte waited data and CH374 to deal with until MCU forbidding SPI chip select;

⑤ If the operation is Read, CH374 read one byte data from appointed address and output then increases address automatically. MCU receives data and saves. CH374 continues to read data from next address and output until MCU forbidding SPI chip select.

⑥ MCU forbids SPI chip selects in CH374 to finish current SPI operation.

The following is SPI logic time sequence image. The former is writing 34H to address12H, and the later is reading 78H from address 56H.



6.4. Other hardware

The unused pin can be left suspend of CH374 in actual circuit.

ACT# in CH374 appoints state. In USB device mode, BIT_SETP_LED_ACT selects active ACT# pin output low-level. The USB transfer process is relevant to self is in default and also can select all transfer including SOF package of USB host. In USB host mode, the pin output high-level when USB device disconnects; the pin output low-level after USB device connecting. The ACT# can external connect LED which serial connects limited current resistor to appoint relevant state.

UD+ and UD- are USB signal wires. When works on USB device mode, they must connect to USB bus directly. When works on USB host mode, they can directly connect to USB device. In order to keep safe to serial connect secure resistor or inductance or ESD protective equipments, the AC/DC equivalent serial connect resistor is within 5Ω.

UEN pin in CH374 is used to control USB signal wire UD+ and UD- output enable. For without UEN pin of CH374T, must set BIT_CTRK-OE_POLAR as 1. For CH374S, UEN pin controls whether allow USB signal output or not. UEN pin can connect to USB device power wire after serial connecting resistor to avoid USB device to continue sending USB signal when losing work power. UEN can be used to woke up sleeping CH374.

CH374 internal set power-up reset circuit and no need external supply reset in generally. RSTI is used to external input asynchronous reset signal; CH374 is reset when RSTI is high-level; when RSTI resume low-level, CH374 internal will continue delay reset about 25mS to step into work state. In order to credibly reset and reduce external disturbing during power-up period, a 0.1uF capacitance can over connect between RSTI and VCC. RST and RST# are reset state output pins and active with high-level and low-level respectively. RST and RST# respectively output high-level and low-level when CH374 power-up reset, forced to reset by external or reset delay and watchdog time over. After CH374 finishes internal reset, RST and RST# will continue delay decades milliseconds then resume to low-level and high-level respectively. RST and RST# supply power-up reset signal for external MCU. Executing any write operation for CH374 can clear watchdog counter time.

The CH374 needs outside to supply 24MHz clock to work normally. In common, clock signal is generated by inverter in CH374 through oscillating of crystal keeping frequency. A crystal of 24MHz between XI and XO can compose the peripheral circuit and connects a high frequency oscillator capacitance to ground respectively. The 24MHz clock signal directly input to XI while suspending XO.

SLP is sleeping state output pin and output low-level in default. If set BIT_CTRL_OSCIL_OFF as 1 to close clock oscillator, then CH374 comes into sleeping state. SLP output high-level until arose to resume low-level.

CKO in CH374 is programmable clock output, and used to supply clock signal from 3MHz to 24MHz. It supports dynamically adjusts clock frequency and transition smoothness. The pin will stop output clock when CH374 come into sleeping state.

CH374 chip supports 5V source voltage or 3.3V source voltage (some types don't support 3.3V voltage). VCC pin input external 5V source when CH374 works with 5V power. And V3 pin must external connect to power-decoupling capacitance range from 4700pF to 0.02uF. When use 3.3V power, V3 in CH374 must be connected to VCC and input external 3.3V power. The other chip that connects to CH374 works voltage is not surpassing 3.3V. One suggestion is that set BIT_CTRL_USB_POWER as 1 to economize power.

6.4. Internal structure

In function, CH374 is a pure interface chip of CH375 removes command explanation device, protocol handing device and common firmware program. The external MCU program is more complex because of removing protocol handling device and firmware program. The interface speed with MCU is higher due to

reduce inner transact etc middle process.

CH374 has a compound USB host mode with USB device mode USB interface engineer SIE and ROOT-HUB to finish physical USB data transfer and receive, deal with bit tracking automatically and synchronous, NRZI code and decode, bit (be) stuffing, parallel/serial data conversion, CRC data checking, transaction handshake, retry error, USB bus state detection and so on.

There are seven endpoints in CH374 inner.

The port0 is a default endpoint, supports upstream and downstream. The buffer of upstream and downstream is 8-byte respectively.

The port1 includes upstream and downstream endpoint and buffer of each is 8-byte. The upstream endpoint number is 81H while the downstream endpoint number is 01H.

The port2 includes upstream and downstream endpoint and buffer of each is 64-byte. The upstream endpoint number is 82H while the downstream endpoint number is 02H.

The host endpoints include output and input endpoint, and each buffer is 64 bytes. The host endpoint is operable to port2 with one buffer. The transfer buffer of host is the upstream buffer of port2 as the receive buffer of host is downstream buffer of port2.

The port0、port1 and port2 of CH374 are used to USB-DEVICE mode while the host endpoint is used to USB-HOST. In USB-HOST mode, CH374 supports various common USB low-speed and full-speed devices. The endpoint number is from 0 to 15 in USB devices, and two directions can support up to 31 endpoints. The package size is from 0 to 64 bytes of USB device and receive maximum package size is 128 bytes.

7. Parameter

7.1. Absolute Maximum Rating (Stresses above those listed can cause permanent damage to the device. Exposure to maximum rated conditions can affect device operation and reliability.)

Name	Parameter note		Min.	Max.	Units
TA	Ambient operating temperature	VCC=5V	-40	85	℃
		VCC=V3=3.3V	-40	85	
TS	Storage temperature		-55	125	℃
VCC	Source voltage (VCC connects to power, GND to ground)		-0.5	6.0	V
VIO	The voltage of input or output pin		-0.5	VCC+0.5	V

7.2. Electrical parameter (test conditions: TA=25℃,VCC=5V,exclude pin connection of USB bus)

(The every current parameter must multiply the coefficient of 40% when the power is 3.3V)

Name	Note of parameter			Min.	Typical	Max.	Units
VCC	Source voltage	V3 doesn't connect to VCC		4.5	5	5.3	V
		V3 connects to VCC		3.3	3.3	3.6	
ICC	Total source current when working		VCC=5V		4	30	mA
			VCC=3.3V		2	15	

ISLP	Source current with low-power, I/O pin in suspend /internal pull up	VCC=5V		0.15	0.2	mA
		VCC=3.3V		0.05	0.08	
VIL	LOW-level Input Voltage		-0.5		0.7	V
VIH	HIGH-level Input Voltage		2.0		VCC+0.5	V
VOL	Output Voltage LOW (draw 4mA current)				0.5	V
VOH	Output Voltage HIGH (4mA output current)		VCC-0.5			V
IUINT	Output current HIGH pull-up in INT#		24	240	360	uA
IUACT	Output current HIGH pull-up in ACT#		53	530	800	uA
IUP	Input current in other input port with internal pull-up resistor		3	150	250	uA
IDUEN	UEN input current with internal pull-down resistor		-30	-60	-120	uA
IDRI	Input current in RSTI with internal pull-down resistor		-70	-140	-210	uA
VR	Edge power when power-up reset		2.4	2.7	3.0	V

7.3. Basic time sequence (test conditions: TA=25℃,VCC=5V or VCC=3.3V)

Name	Explanation of parameter	Min.	Typical	Max.	Units
FCLK	The clock freq of XI in mode of USB-HOST	23.99	24.00	24.01	MHz
TPR	Reset time of internal power-up	15	20	40	mS
TRI	Effective signal width of external reset	100			nS
TRD	Delay time of external reset	15	17	20	mS
TR0	RST and RST# output reset time when power-up	60		150	mS
TDGC	Watchdog count time cycle (overflow time)	950		1170	mS
TDGR	The reset time generated by watchdog count time overflow	60	64	140	mS
TWAK	Chip wake-up time	3	5	15	mS
TINT	INT# interrupt pulse width in low-level pulse mode	8		16	mS
TNAK	The overtime of NAK automatically retry	3900		4200	mS

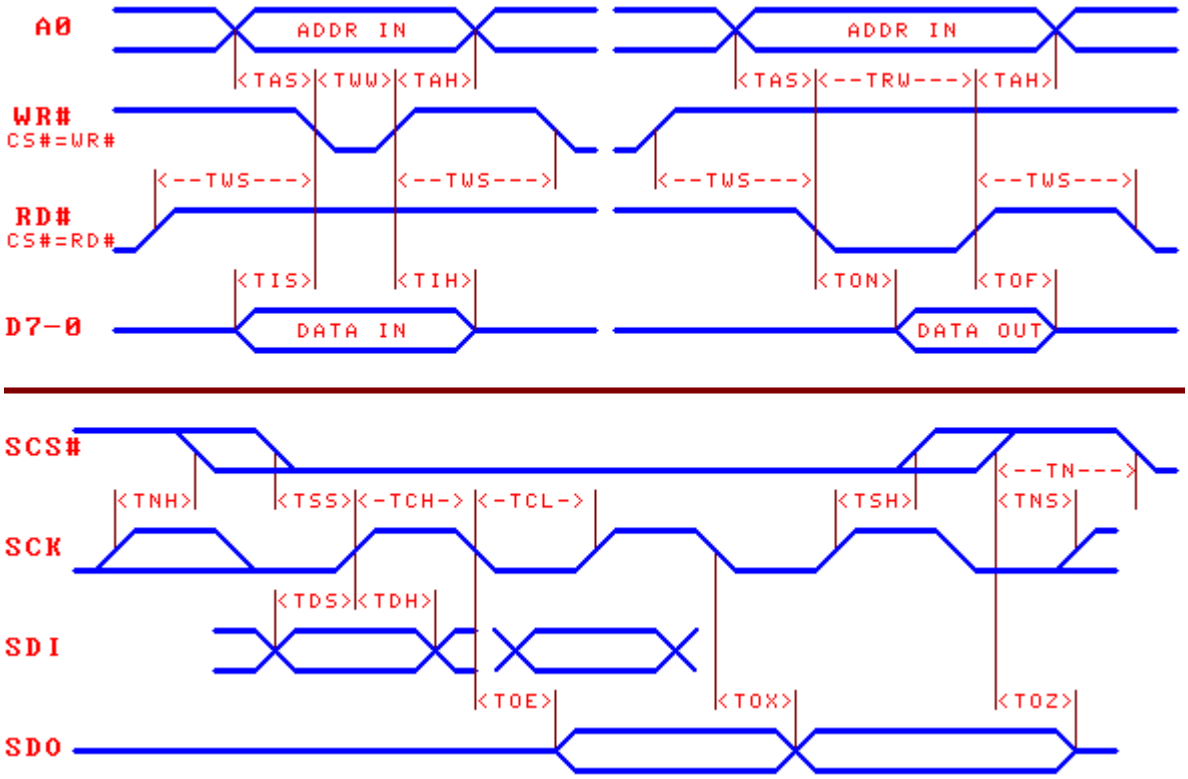
7.4. Parallel interface time sequence (test conditions: TA=25℃,VCC=5V, parameter VCC=3.3V in bracket, refer to the following picture)

(RD implies RD# and CS# are active, execute read operation when WR#=1 & RD#=CS#=0)

(WR implies WR# and CS# are active, execute write operation when WR#=CS#=0)

Name	Explanation of parameter	Min.	Typical	Max.	Units
TWW	Write pulse width	40 (65)			nS
TRW	Read pulse width	40 (65)			nS
TWS	The interval width of READ pulse or WRITE pulse	120 (135)			nS
TAS	Address to Read HIGH or Write HIGH SET-UP TIME	6			nS

TAH	Address hold time after Read HIGH or Write HIGH	3			nS
TIS	Data to Write HIGH set-up time	3			nS
TIH	Data hold time after Write HIGH	6			nS
TON	Data valid after Read LOW		30 (45)	30 (55)	nS
TOF	Data hold after Read HIGH			20 (35)	nS



7.5. Serial interface time sequence (test conditions: TA=25℃,VCC=5V, parameter VCC=3.3V in bracket, refer to the upper picture)

Name	Explanation of parameter	Min.	Typical	Max.	Units
TSS	SCS# LOW to SCK LOW set-up time	20 (30)			nS
TSH	SCK HIGH to SCS# HOLD TIME	20 (30)			nS
TNS	SCS# HIGH to SCK LOW set-up time	20 (30)			nS
TNH	SCKHIGH to SCS# HIGH hold time	20 (30)			nS
TN	SCS# invalid time	60 (100)			nS
TCH	High–level time of SCK	20 (30)			nS
TCL	Low-level time of SCK	20 (30)			nS
TDS	SDI input to SCK rising edge set-up time	8 (12)			nS
TDH	After SCK rising edge to SDI input hold time	5			nS
TOE	SCK falling edge to SDO output valid	2	12 (20)	20 (30)	nS
TOX	SCK falling edge to SDO output change		8 (12)	12 (20)	nS
TOZ	SCS# invalid to SDO output invalid			20 (30)	nS

8.Application

8.1. Parallel interface mode (the following image)

This is parallel connection circuit of CH374.

In the image, the VCC of CH374 is 5V in default. If VCC is 3.3V, connect V3 and VCC. The USB source power is 5V which is supplied to the USB port P1.

The capacitance C3 eliminates the coupling of inner power of CH375.The capacity of C3 is 4700pF to 0.02uF.It is made of monolithic or high frequency ceramic. The C4 is used to decoupling of external power. The C4 is 0.1uF and made of monolithic or high frequency ceramic.

The crystal X1, capacitance C1 and C2 are composed of clock oscillating circuit of CH374.The USB-HOST manner needs exact frequency. The frequency of X1 is 24MHz±0.4‰,C1 and C2 are monolithic or high frequency ceramic capacitors of 22pF. Capacitance C5 is optional and only be used to prolong reset time when CH374 power-up. In generally, the C5 can be taken out of the application circuit.

If the source power of CH374 is 3.3V, connect V3 and VCC, and input 3.3V voltage, take the C3 out of the circuit.

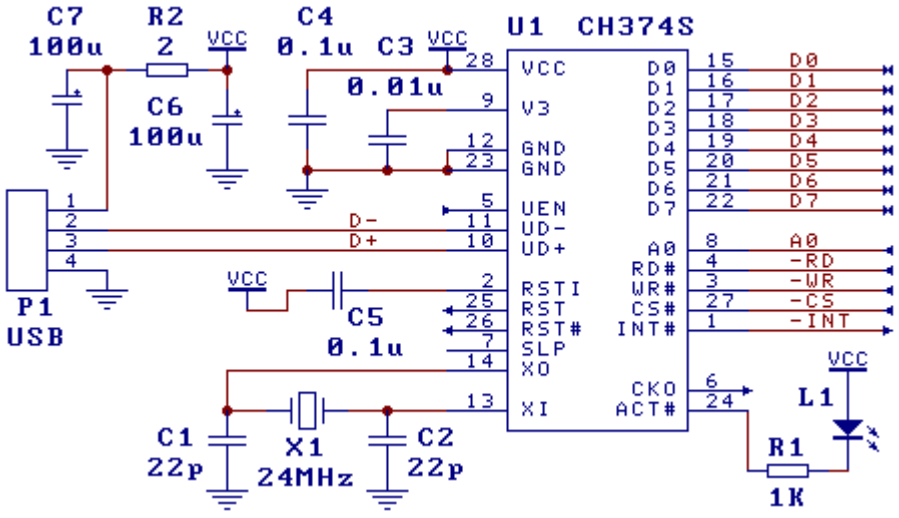
When designing the PCB, pay much attention to some notes: decoupling capacitance C3 and C4 must keep near to connection pin of CH374; makes sure D+ and D- are parallel and supply ground or cover copper besides to decrease the disturb from outside signal; the relevant signal leads between XI and XO must be kept as short as possible. In order to lessen the high frequency clock disturb outside, setting ground wire on the circle or covering copper to the relative equipment.

In USB-HOST application, resistor R2 and capacitance C7 are usually used to limit peak current when USB device connecting. UEN connects to USB power via 1KΩ resistor and be used to close USB output signal when lose sources. L1 and limited resistor R1 are optional to indicate state.

CH374 also supplies assistant signal as following: RST and RST# can be used to supply power reset and watch-dog reset signal for MCU; CKO can supply clock signal for MCU which can be automatically programmed; SLP can supply automatically awake control for MCU or other device.

The program of MCU can be substituted of detecting interrupt token register if the INT# doesn't connect.

CH374 has common passive parallel interface and can directly connect to various MPU, DSP, MCU and so on through D0-D7,A0,-RD,-CS and –INT signal.



8.2. Serial interface mode (the following picture)

CH374 works on the SPI serial interface mode when RD# and WR# connect to ground while CS# is high-level or suspended. On SPI serial interface mode, CH374 only connects five signal wires to

MPU/DSP/MCU and the five signal wires are SCS#, SCK, SDI, SDO and INT#. The other pins are left suspended.

In order to save pins, INT# can be left disconnected and replace detection of interrupt token register, but the detection efficient is low.

SDO can be serially connected to 330Ω resistor R4 then parallel connected to SDI, at last connected to SDI and SDO in MCU to economize pins. Certainly, the SDO in MCU must be three-state or can be close output.

The circuit of SPI serial interface mode is the same with parallel interface mode except the connect lines is less. In the soft program, the program is basically same with parallel interface mode except the interface sub-program of hardware abstract layer.

The SPI serial interface mode of CH374 supply USB communication and control USB device mode for MCU which has limited I/O pins and without parallel interface bus.