RGB-LED and USB Enhanced MCU CH557, USB MCU CH556

Datasheet

Version: 1F

http://wch.cn

1. Overview

The CH557 is a USB multi-host multi-device enhanced E8051 core MCU compatible with MCS51 instruction set. 79% of its instructions are single-byte single-cycle, and the average instruction speed is 8 to 15 times faster than that of the standard MCS51.

CH557 supports the maximum 32 MHz system clock frequency, built-in 64K program memory Flash-ROM and 256-byte internal iRAM and 8 Kbytes of internal xRAM. The xRAM supports direct memory access (DMA).

CH557 has a built-in USB host controller and receiver/transmitter, and 4-port USB root-hub, and supports full-speed and low-speed USB Host mode and USB Device mode.

CH557 has built-in 3*8-channel PWM, supports 384 monochromatic LEDs or 128 groups of RGB tri-color LEDs.

In addition, CH557 has a built-in 12-bit analog-to-digital converter (ADC), capacitive touch key detection module, built-in clock, 3 sets of timer and 2 channels of signal capture, 6 channels of PWM, 2 UARTs, 2 SPIs, I2C host and I2C slave and other functional modules.

CH556 is a simplified version of CH557, without PWM module of RGB tri-color LED. CH556 only provides 2-port USB root-hub, others are the same as that of CH557. Please directly refer to CH557 datasheet and information. The pins are basically compatible with CH549, CH548 and CH559.

<table>
<tr><th>Product No.</th><th>Program+boot loader ROM + EEPROM</th><th>xRAM iRAM</th><th>USB device</th><th>USB host root-hub</th><th>Timer</th><th>Signal capture</th><th>General PWM</th><th>RGB LED</th><th>UART</th><th>SPI host SPI slave</th><th>12-bit ADC</th><th>Capacitive touch key</th></tr>
<tr><td>CH557</td><td rowspan="2">60KB+3KB +1KB</td><td rowspan="2">8192 +256</td><td rowspan="2">full speed low speed</td><td>4-port</td><td rowspan="2">3</td><td rowspan="2">2 channels</td><td rowspan="2">6 channels</td><td>8*16</td><td rowspan="2">2</td><td rowspan="2">1 host slave
1 host</td><td rowspan="2">14 channels</td><td rowspan="2">14 channels</td></tr>
<tr><td>CH556</td><td>2-port</td><td>None</td></tr>
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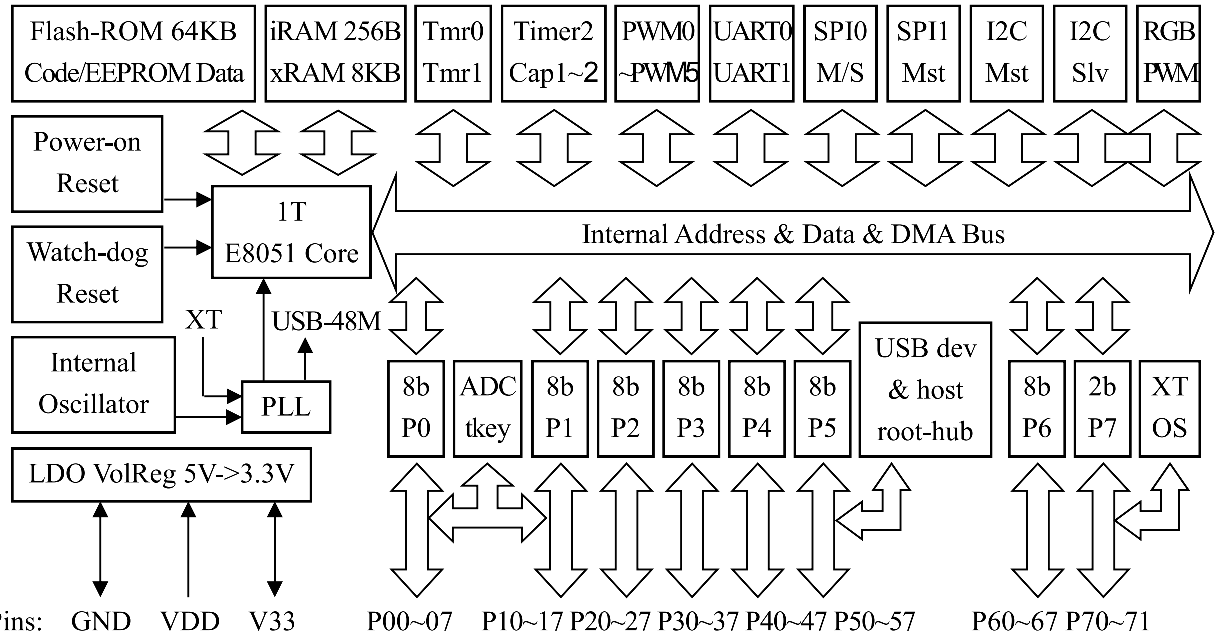
The following is the internal block diagram of CH557, for reference only.



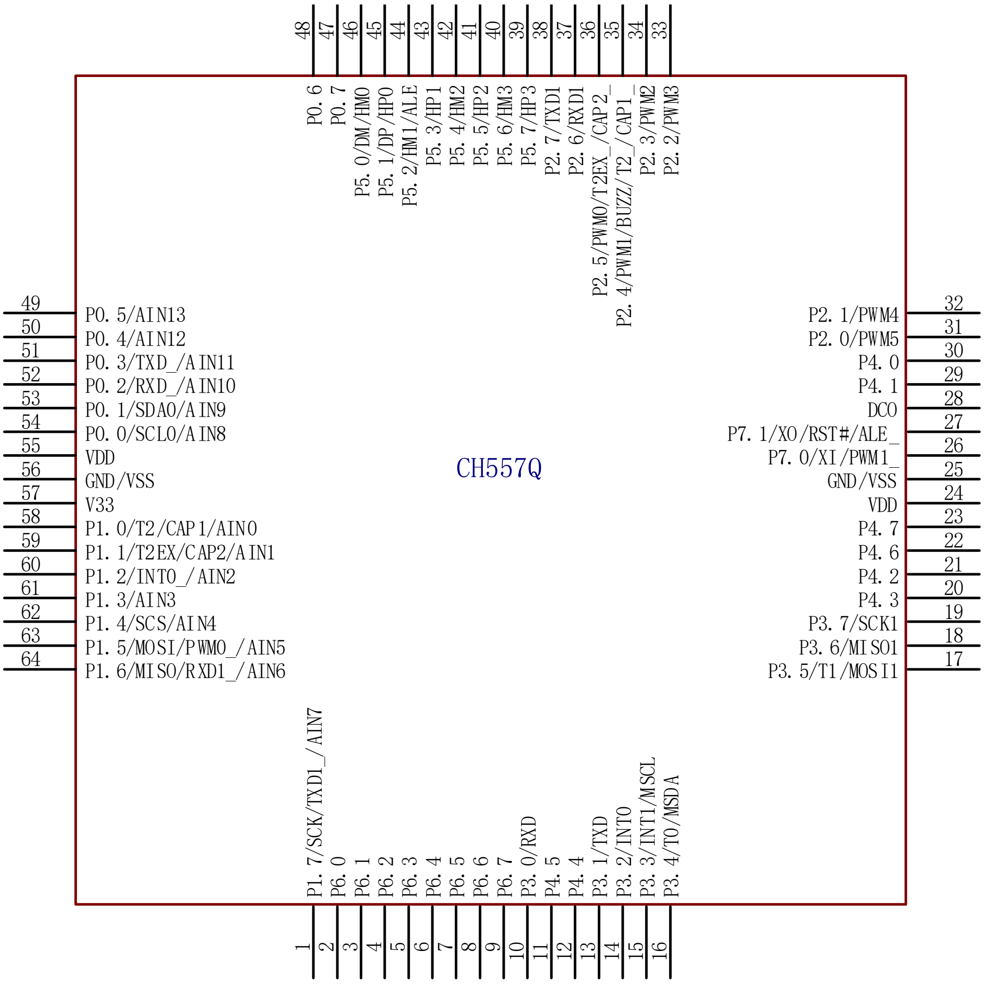
2. Features

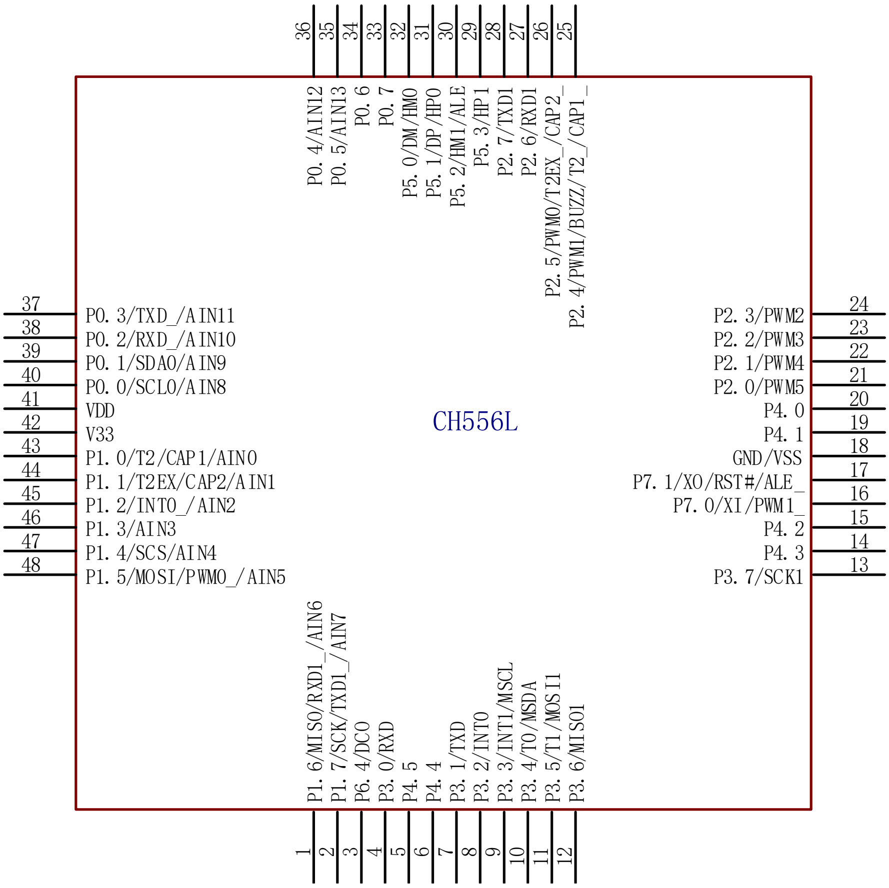
- Core: Enhanced E8051 core compatible with MCS51 instruction set, 79% of its instructions are single-byte single-cycle, and the average instruction speed is 8 to 15 times faster than that of the standard MCS51, with special XRAM data fast copy command, and double DPTR pointer.
- ROM: 64KB non-volatile memory Flash-ROM, which supports 10K times of erase/write operations and can all be used for the program storage area;or it can be divided into a 60 KB program storage area, a 1 KB data storage area EEPROM and a 3 KB BootLoader/ISP program area.
- EEPROM: 1 Kbyte of data storage area EEPROM, which is divided into 16 independent blocks, supporting single-byte read, single-byte write, block write (1 ~ 64 bytes), block erase (64 bytes) operations. In a typical environment, it generally supports 100K times of erase/write operations (not guaranteed).
- OTP: One time programmable data storage area. OTP has a total of 32 bytes, and supports double word read (4 bytes), single byte write.
- RAM: 256-byte internal iRAM, which can be used for fast temporary storage of data and stack. 8KB on-chip xRAM, which can be used for large amount of data temporary storage and DMA (direct memory access).
- USB: USB controller and USB transceiver, supports USB-Host mode and USB-Device mode, supports USB 2.0 full speed (12 Mbps) and low speed (1.5 Mbps). Built-in 4-port USB root-hub, USB host can manage 4 USB devices simultaneously via the root-hub. Data packet can be up to 64 bytes. Built-in FIFO. DMA capability.
- Timer: 3 sets of 16-bit timers, T0, T1 and T2, which are standard MCS51 timers.
- Capture: Timer T2 is extended to support 2-channel signal capture, support leading edge trigger, trailing edge trigger, periodic detection.
- PWM: 6-channel PWM output, support standard 8-bit data, fast 6-bit data or high-precision 12-bit data, support interleaved output.
- UART: 2 UARTs. UART0 is a standard MCS51 serial port. UART1 has a built-in communication baud rate setting register.

- SPI: 2 SPIs, built-in FIFO, clock frequency can be approximate to half of the system clock frequency (Fsys). It supports simplex multiplexing of serial data input and output. SPI0 controller supports master/Slave mode. SPI1 controller only supports Master mode.
- I2CM: I2C master controller, with adjustable clock frequency.
- I2CS: I2C slave controller, support DMA, which is used for EEPROM memory 24C.
- RGB LED: Support 384 monochromatic LEDs or 128 sets of RGB tri-color LEDs through 3*8-channel PWM and 1/16 dynamic scanning. The maximum 8-bit brightness PWM supports 256-level of grayscale and the maximum 3*8-bit color PWM supports 16777216 sets of combined colors. The dedicated DMA mode supports loading preset curing data from Flash-ROM or loading edited data from xRAM.
- BUZZ: Buzzer driver output, 3 frequencies are optional.
- ADC: 14-channel 12-bit A/D converter.
- Touch-key: 14-channel capacitive touch key detection. Each ADC channel supports touch key detection.
- GPIO: Up to 58 GPIO pins (including XI and USB pins), support MCS51 compatible quasi-bidirectional mode, newly add high-impedance input, push-pull output, open-drain output mode.
- Interrupt: 15 sets of interrupt signal sources, including 6 sets of interrupts compatible with the standard MCS51 (INT0, T0, INT1, T1, UART0, T2), and 9 sets of extended interrupts (SPI0, USB, ADC, UART1, PWMX/LED/I2C, GPIO, WDOG). GPIO interrupt can be selected from several pins.
- Watch-Dog: 8-bit presettable watchdog timer WDOG, support timing interrupt.
- Reset: 5 kinds of reset signal sources, built-in power on reset and multi-stage adjustable power supply low voltage detection reset module, supports software reset and watchdog overflow reset, optional pin external input reset.
- Clock: Built-in 24 MHz clock source, which can support external crystals by multiplexing GPIO pins, and the built-in PLL is used to generate the USB clock and the system clock frequency (Fsys) with the required frequency.
- Power: Built-in 5V to 3.3V low dropout voltage regulator for USB and other modules. It supports 5V or 3.3V or even 6V or 2.8V supply voltage. Built-in DC-DC controller, which can control the external MOS tube to achieve voltage boost.
- Sleep: Support low-power Sleep mode, and support USB, UART0, UART1, SPI0, and part of the GPIO external waking.
- Builtin unique ID, support ID number and calibration.

3. Package

Package	Body size		Lead pitch		Description	Part No.
LQFP-64	7*7mm		0.4mm	15.7mil	Standard LQFP 64-pin patch	CH557Q
LQFP-48	7*7mm		0.5mm	19.7mil	Standard LQFP 48-pin patch	CH556L


CH557Q
P0.6
P0.7
P5.0/DM/HM0
P5.1/DP/HP0
P5.2/HM1/ALE
P5.3/HP1
P5.4/HM2
P5.5/HP2
P5.6/HM3
P5.7/HP3
P2.7/TXD1
P2.6/RXD1
P2.5/PWM0/T2EX_/CAP2_
P2.4/PWM1/BUZZ/T2_/CAP1_
P2.3/PWM2
P2.2/PWM3
P0.5/AIN13
P0.4/AIN12
P0.3/TXD_/AIN11
P0.2/RXD_/AIN10
P0.1/SDA0/AIN9
P0.0/SCL0/AIN8
VDD
GND/VSS
V33
P1.0/T2/CAP1/AIN0
P1.1/T2EX/CAP2/AIN1
P1.2/INT0_/AIN2
P1.3/AIN3
P1.4/SCS/AIN4
P1.5/MOSI/PWM0_/AIN5
P1.6/MISO/RXD1_/AIN6
P2.1/PWM4
P2.0/PWM5
P4.0
P4.1
DCO
P7.1/XO/RST#/ALE_
P7.0/XI/PWM1_
GND/VSS
VDD
P4.7
P4.6
P4.2
P4.3
P3.7/SCK1
P3.6/MISO1
P3.5/T1/MOSI1
P1.7/SCK/TXD1_/AIN7
P6.0
P6.1
P6.2
P6.3
P6.4
P6.5
P6.6
P6.7
P3.0/RXD
P4.5
P4.4
P3.1/TXD
P3.2/INT0
P3.3/INT1/MSCL
P3.4/T0/MSDA


CH556L
P0.4/AIN12
P0.5/AIN13
P0.6
P0.7
P5.0/DM/HM0
P5.1/DP/HP0
P5.2/HM1/ALE
P5.3/HP1
P2.7/TXD1
P2.6/RXD1
P2.5/PWM0/T2EX_/CAP2_
P2.4/PWM1/BUZZ/T2_/CAP1_
P0.3/TXD_/AIN11
P0.2/RXD_/AIN10
P0.1/SDA0/AIN9
P0.0/SCL0/AIN8
VDD
V33
P1.0/T2/CAP1/AIN0
P1.1/T2EX/CAP2/AIN1
P1.2/INT0_/AIN2
P1.3/AIN3
P1.4/SCS/AIN4
P1.5/MOSI/PWM0_/AIN5
P2.3/PWM2
P2.2/PWM3
P2.1/PWM4
P2.0/PWM5
P4.0
P4.1
GND/VSS
P7.1/XO/RST#/ALE_
P7.0/XI/PWM1_
P4.2
P4.3
P3.7/SCK1
P1.6/MISO/RXD1_/AIN6
P1.7/SCK/TXD1_/AIN7
P6.4/DCO
P3.0/RXD
P4.5
P4.4
P3.1/TXD
P3.2/INT0
P3.3/INT1/MSCL
P3.4/T0/MSDA
P3.5/T1/MOSI1
P3.6/MISO1

4. Pin definitions

Pin No.		Pin Name	Alternate (Left function with highest priority)	Other function description
CH557Q	CH556L			
55,24	41	VDD	VCC	I/O power input and external power input of internal USB power regulator, an external 0.1uF decoupling capacitor is required.
57	42	V33	V3	Internal USB power regulator output and internal USB power input. When supply voltage is less than 3.6V, connect VDD to input the external power supply. when supply voltage is greater than 3.6V, an external 0.1uF decoupling capacitor is required.
56,25	18	GND	VSS	Ground
54	40	P0.0	SCL0/AIN8	AIN8 ~ AIN13: 6 channels of ADC analog signal/touch key input. RXD_, TXD_: RXD, TXD pin mapping. SCL0, SDA0: I2CS serial clock input, bidirectional serial data. Level change on any one of P0.0 to P0.7 pins supports interrupt and wakeup.
53	39	P0.1	SDA0/AIN9	
52	38	P0.2	RXD_/AIN10	
51	37	P0.3	TXD_/AIN11	
50	36	P0.4	AIN12	
49	35	P0.5	AIN13	
48	34	P0.6		
47	33	P0.7		
58	43	P1.0	T2/CAP1/AIN0	AIN0 ~ AIN7: 8 channels of ADC analog signal/touch key input. T2: External count input/clock output of timer/counter 2. T2EX: Reload/capture input of timer/counter 2. CAP1, CAP2: Capture input 1, 2 of timer/counter 2. SCS, MOSI, MISO, SCK: SPI0 interfaces. SCS is chip select input. MOSI is master output/slave input. MISO is master input/slave output. SCK is serial clock master output/slave input. INT0_, PWM0_, RXD1_, TXD1_: INT0/PWM0/RXD1/TXD1 pin mapping. Level change on any one of P1.0 to P1.3 pins supports interrupt and wakeup.
59	44	P1.1	T2EX/CAP2/AIN1	
60	45	P1.2	INT0_/AIN2	
61	46	P1.3	AIN3	
62	47	P1.4	SCS/AIN4	
63	48	P1.5	MOSI/PWM0_/AIN5	
64	1	P1.6	MISO/RXD1_/AIN6	
1	2	P1.7	SCK/TXD1_/AIN7	
31	21	P2.0	PWM5	PWM0～PWM5: 6 channels of PWM output. BUZZ: Buzzer driver output. T2_/CAP1_: T2/CAP1 pin mapping. T2EX_/CAP2_: T2EX/CAP2 pin mapping. RXD1, TXD1: UART1 serial data input, serial data output. P2.0 to P2.3 pins provide independent controllable pull-down resistors. Level change on any one of P2.0 to P2.3 pins supports interrupt and wakeup.
32	22	P2.1	PWM4	
33	23	P2.2	PWM3	
34	24	P2.3	PWM2	
35	25	P2.4	PWM1/BUZZ/T2_/CAP1_	
36	26	P2.5	PWM0/T2EX_/CAP2_	
37	27	P2.6	RXD1	
38	28	P2.7	TXD1	

10	4	P3.0	RXD	RXD, TXD: UART0 serial data input, serial data output. MSCL, MSDA: I2CM serial clock output, bidirectional serial data. INT0, INT1: External interrupt 0, external interrupt 1 input. T0, T1: timer 0, timer 1 external input. MOSI1, MISO1, SCK1: SPI1 interfaces. MOSI1 is master output. MISO is master input. SCK is serial clock output.
13	7	P3.1	TXD	
14	8	P3.2	INT0	
15	9	P3.3	MSCL/INT1	
16	10	P3.4	MSDA/T0	
17	11	P3.5	MOSI1/T1	
18	12	P3.6	MISO1	
19	13	P3.7	SCK1	
30	20	P4.0		Level change on any one of P4.0 to P4.7 pins supports interrupt and wakeup. If the corresponding bit of P4_LED_KEY is 1, it has the following characteristics: Support current keyboard signal input when pins are input or bidirectional. When the pin is output, no series current limiting resistor is needed, and the LED can be driven directly.
29	19	P4.1		
21	15	P4.2		
20	14	P4.3		
12	6	P4.4		
11	5	P4.5		
22	None	P4.6		
23	None	P4.7		
46	32	P5.0	DM/HM0	DM, DP: D- and D+ signals of USB host or USB device. HM0, HP0: D- and D+ signals of USB host root hub0. HM1, HP1: D- and D+ signals of USB host root hub1. HM2, HP2: D- and D+ signals of USB host root hub2. HM3, HP3: D- and D+ signals of USB host root hub3. ALE: Dummy address lock enable signal output or clock output. The transceiver is designed built-in based on USB2.0. and the pins are not connected to resistors in series.
45	31	P5.1	DP/HP0	
44	30	P5.2	HM1/ALE	
43	29	P5.3	HP1	
42	None	P5.4	HM2	
41	None	P5.5	HP2	
40	None	P5.6	HM3	
39	None	P5.7	HP3	
2	None	P6.0		DCO: DC-DC drive output. The I/O power supply of P6.0～P6.7 is V33, and the input voltage does not exceed V33. And separate controllable 7.5K pull-up resistors to VDD are provided by P6.0 ~ P6.7.
3	None	P6.1		
4	None	P6.2		
5	None	P6.3		
6	3	P6.4	DCO	
7	None	P6.5		
8	None	P6.6		
9	None	P6.7		
26	16	P7.0	XI/PWM1_	XI, XO: Input and inverted output of external crystal oscillation. PWM1_, ALE_: PWM1/ALE pin mapping. RST#: External reset input, active low, with built-in pull-up resistor.
27	17	P7.1	XO/RST#/ALE_	
28	None	DCO		DC-DC drive output.

After RGB LED of CH557 is enabled, some pins are optionally alternate for PWM driver or dynamic scanning driver.

Pin Name	Function Name	Function Description
P4.0～P4.7	RED0～RED7	RGB LED red PWM drive output, each bit can be independently enabled and disabled.
P2.0～P2.7	GRE0～GRE7	RGB LED green PWM drive output, each bit can be independently enabled and disabled.
P1.0～P1.7	BLU0～BLU7	RGB LED blue PWM drive output, each bit can be independently enabled and disabled.
P7.0～P7.1	COM14～COM15	RGB LED dynamic scanning public drive output, each bit can be independently enabled and disabled.
P0.0～P0.7	COM16～COM23	RGB LED dynamic scanning public drive output, each bit can be independently enabled and disabled.
P3.0～P3.7	COM24～COM31	RGB LED dynamic scanning public drive output, each bit can be independently enabled and disabled.

5. Special function register (SFR)

The following abbreviations may be used in this manual to describe the registers:

Abbreviation	Description
RO	Software can only read these bits.
WO	Software can only write to this bit. The read value is invalid.
RW	Software can read and write to these bits.
H	End with it to indicate a hexadecimal number
B	End with it to indicate a binary number

5.1 SFR introduction and address distribution

CH557 controls and manages the device, and sets the working mode with the special function registers (SFR and xSFR).

SFR occupies 80H-FFH address range of the internal data storage space and can only be accessed by direct address commands. Registers with the x0h and x8h addresses can be accessed by bits to avoid modifying the values of other bits when accessing a specific bit. Other registers with the addresses that are not the multiple of 8 can only be accessed by bytes.

Some SFRs can only be written in safe mode, while they can be read only in non-safe mode , for example: GLOBAL_CFG, CLOCK_CFG, WAKE_CTRL, POWER_CFG, GPIO_IE.

Some SFRs have one or more aliases, for example: SPI0_CK_SE / SPI0_S_PRE, UDEV_CTRL / UHUB01_CTRL, UEP1_CTRL / UH_SETUP, UEP2_CTRL / UH_RX_CTRL, UEP2_T_LEN / UH_EP_PID, UEP3_CTRL / UH_TX_CTRL, UEP3_T_LEN / UH_TX_LEN, UEP2_DMA_H / UH_RX_DMA_H, UEP2_DMA_L / UH_RX_DMA_L, UEP2_DMA / UH_RX_DMA, UEP3_DMA_H / UH_TX_DMA_H, UEP3_DMA_L / UH_TX_DMA_L, UEP3_DMA / UH_TX_DMA, ROM_ADDR_L/ROM_DATA_LL, ROM_ADDR_H/ROM_DATA_LH, ROM_DATA_HL/ROM_DAT_BUF, ROM_DATA_HH/ROM_BUF_MOD.

Some addresses correspond to several independent SFRs, for example: ADC_DAT_H/TKEY_CTRL, SAFE_MOD/CHIP_ID, ROM_CTRL/ROM_STATUS.

CH557 contains the 8051 standard all SFR registers, and other device control registers are added. See the table below for SFRs.

Table 5.1.1 Internal special function registers (SFR)

SFR	0, 8	1, 9	2, A	3, B	4, C	5, D	6, E	7, F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRE	SPI0_SETUP	A_INV	RESET_KEEP	WDOG_COUNT
0xF0	B	P7_IO		ADC_CTRL	ADC_DAT_L	ADC_DAT_H TKEY_CTRL	ADC_CHAN	LED_STATUS
0xE8	IE_EX	IP_EX		USB_HUB_ST	UEP0_DMA_L	UEP0_DMA_H	UEP1_DMA_L	UEP1_DMA_H
0xE0	ACC	UHUB23_CTRL	USB_CTRL	USB_DEV_AD	UEP2_DMA_L UH_RX_DMA_L	UEP2_DMA_H UH_RX_DMA_H	UEP3_DMA_L UH_TX_DMA_L	UEP3_DMA_H UH_TX_DMA_H
0xD8	USB_INT_FG	USB_INT_ST	USB_MIS_ST	USB_RX_LEN	UEP0_CTRL	UEP0_T_LEN	UEP4_CTRL	UEP4_T_LEN
0xD0	PSW	UDEV_CTRL UHUB01_CTRL	UEP1_CTRL UH_SETUP	UEP1_T_LEN	UEP2_CTRL UH_RX_CTRL	UEP2_T_LEN UH_EP_PID	UEP3_CTRL UH_TX_CTRL	UEP3_T_LEN UH_TX_LEN
0xC8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	T2CAP1L	T2CAP1H
0xC0	P4	P4_LED_KEY	P4_MOD_OC	P4_DIR_PU	P0_MOD_OC	P0_DIR_PU	LED_DMA_L	LED_DMA_H
0xB8	IP	CLOCK_CFG	POWER_CFG	I2CS_INT_ST	SCON1	SBUF1	SBAUD1	SIF1
0xB0	P3	GLOBAL_CFG	GPIO_IE	I2CX_INT	SPI1_STAT	SPI1_DATA	SPI1_CTRL	SPI1_CK_SE
0xA8	IE	WAKE_CTRL	P5_IN	P5_OUT_PU	P5_OE	P6_IN	P6_OUT_PU	P6_OE
0xA0	P2	SAFE_MOD CHIP_ID	XBUS_AUX	PWM_DATA3	PWM_DATA4	PWM_DATA5	LED_COMMON	LED_PIN_OE
0x98	SCON	SBUF	PWM_DATA2	PWM_DATA1	PWM_DATA0	PWM_CTRL	PWM_CK_SE	PWM_CTRL2
0x90	P1		P1_MOD_OC	P1_DIR_PU	P2_MOD_OC	P2_DIR_PU	P3_MOD_OC	P3_DIR_PU
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_HL ROM_DAT_BUF	ROM_DATA_HH ROM_BUF_MOD
0x80	P0	SP	DPL	DPH	ROM_ADDR_L ROM_DATA_LL	ROM_ADDR_H ROM_DATA_LH	ROM_CTRL ROM_STATUS	PCON

Notes :(1) Those in red text can be accessed by bits;

(2). The following table shows the description of different color boxes

Grey	Register address
Magenta	SPI0 register
Violet	SPI1 register
Light blue	ADC register
Light green	USB register
Pink	Timer/counter 2 register
Yellow	Port setting register
Cyan	PWMX register
Orange	UART1 register
Olive	Timer/counter 0 and 1 register
Red	I2C register
Green	RGB LED PWM register
Teal	Flash-ROM register

xSFR occupies the 2000H-3FFFH address range of the external data storage space and actually uses only part of the address within the range of range 2100H-22FFH . After bXIR_XSFR is set to 1, MOVX_@r0/R1 command is dedicated to accessing xSFR, and some xSFRs can imitate the page data pdata feature of the external data storage space for quick access by aliasing the original name with a P character. For example, in C Program Language, read/write to I2CS_CTRL by accessing the xSFR of xdata feature in the address range of 2100H-22FFH with the long pointer of DPTR. Read/write to pI2CS_CTRL by accessing the xSFR of pdata feature in the address range of 00H-FFH with the short pointer of R0 or R1.

Some SFRs have one or more aliases, for example: UEP2_3_MOD/UH_EP_MOD.

Table 5.1.2 External special function registers (xSFR) with pdata feature

xSFR	0, 8	1, 9	2, A	3, B	4, C	5, D	6, E	7, F
0xE8	ANA_PIN	PIN_FUNC	PORT_CFG	CMP_DCDC				
0xE0	UEP4_1_MOD	UEP2_3_MOD UH_EP_MOD	USB_INT_EN					
0xD8	LED_INT_ADJ	LED_RED_ADJ	LED_GRE_ADJ	LED_BLU_ADJ	LED_FRA_STA	LED_COL_CNT		
0xD0		LED_CTRL	LED_CYCLE	LED_FRAME				
0xC8								
0xC0	I2CM_CTRL	I2CM_CK_SE	I2CM_START	I2CM_DATA	I2CM_STAT			
0x38			I2CS_STAT					
0x30			I2CS_CTRL	I2CS_DEV_A		I2CS_ADDR	I2CS_DATA	

5.2 SFR/xSFR classification and reset value

Figure 5.2 SFR and xSFR description and reset value

Function Classification	Name	Address	Description	Reset value
System setting registers	B	F0h	B register	0000 0000b
	ACC	E0h	Accumulator	0000 0000b
	A_INV	FDh	Inverted value of accumulator high bit and low bit	0000 0000b
	PSW	D0h	Program status word register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (in CH557 boot loader state)	0110 0000b
			Global configuration register (in CH557 application program state)	0100 0000b
			Global configuration register (in CH556 boot loader state)	0010 0000b
			Global configuration register (in CH556 application program state)	0000 0000b
	CHIP_ID	A1h	ID code of CH557 (read-only)	0101 0111b
			ID code of CH556 (read-only)	0101 0110b
	SAFE_MOD	A1h	Safe mode control register (write only)	0000 0000b

	DPH	83h	The data address pointer is 8 bits higher	0000 0000b
	DPL	82h	The data address pointer is 8 bits lower	0000 0000b
	DPTR	82h	DPL and DPH constitute a 16-bit SFR	0000h
	SP	81h	Stack pointer	0000 0111b
Clock, sleep and power control registers	WDOG_COUNT	FFh	Watchdog count register	0000 0000b
	RESET_KEEP	FEh	Reset keep register (in power on reset state)	0000 0000b
	POWER_CFG	BAh	Power management configuration register	0000 0xxxb
	CLOCK_CFG	B9h	System clock configuration register	1000 0011b
	WAKE_CTRL	A9h	Sleep wakeup control register	0000 0000b
	PCON	87h	Power supply control register (in power on reset state)	0001 0000b
	CMP_DCDC	21EBh	Comparator and DC-DC control register	0000 0000b
Interrupt control registers	IP_EX	E9h	Extend interrupt priority control register	0000 0000b
	IE_EX	E8h	Extend interrupt enable register	0000 0000b
	IP	B8h	Interrupt priority control register	0000 0000b
	IE	A8h	Interrupt enable register	0000 0000b
	GPIO_IE	B2h	GPIO interrupt enable register	0000 0000b
Flash-ROM registers	ROM_DATA_HH	8Fh	High byte of flash-ROM data register high word (read only)	xxxx xxxxb
	ROM_DATA_HL	8Eh	Low byte of flash-ROM data register high word (read only)	xxxx xxxxb
	ROM_DATA_HI	8Eh	ROM_DATA_HL and ROM_DATA_HH constitute a 16-bit SFR	xxxxh
	ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase/program operation	xxxx xxxxb
	ROM_DAT_BUF	8Eh	Data butter register for flash-ROM erase/program operation	xxxx xxxxb
	ROM_STATUS	86h	flash-ROM status register (read only)	0000 0000b
	ROM_CTRL	86h	flash-ROM control register (write only)	0000 0000b
	ROM_ADDR_H	85h	flash-ROM address register high byte	xxxx xxxxb
	ROM_ADDR_L	84h	flash-ROM address register low byte	xxxx xxxxb
	ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H constitute a 16-bit SFR	xxxxh
	ROM_DATA_LH	85h	High byte of flash-ROM data register low word (read only)	xxxx xxxxb
	ROM_DATA_LL	84h	Low byte of flash-ROM data register low word (read only)	xxxx xxxxb
	ROM_DATA_LO	84h	ROM_DATA_LL and ROM_DATA_LH constitute a 16-bit SFR	xxxxh
Port setting registers	XBUS_AUX	A2h	External bus auxiliary setting register	0000 0000b
	P7	F1h	P7 port input and output register	00PP 0011b
	P0_DIR_PU	C5h	P0 port direction control and pull-up enable register	1111 1111b

	P0_MOD_OC	C4h	P0 port output mode register	1111 1111b
	P4_DIR_PU	C3h	P4 port direction control and pull-up enable register	1111 1111b
	P4_MOD_OC	C2h	P4 port output mode register	1111 1111b
	P4_LED_KEY	C1h	P4 port LED current limit and keyboard mode register	0000 0000b
	P6_DIR	AFh	P6 port direction control register	0000 0000b
	P6_OUT_PU	AEh	P6 port output data and pull-up enable register	0000 0000b
	P6_IN	ADh	P6 port input register	PPPP PPPPb
	P5_DIR	ACh	P5 port direction control register	0000 0000b
	P5_OUT_PU	ABh	P5 port output data and pull-up enable register	0000 0000b
	P5_IN	AAh	P5 port input register	PPPP PPPPb
	P3_DIR_PU	97h	P3 port direction control and pull-up enable register	1111 1111b
	P3_MOD_OC	96h	P3 port output mode register	1111 1111b
	P2_DIR_PU	95h	P2 port direction control and pull-up enable register	1111 1111b
	P2_MOD_OC	94h	P2 port output mode register	1111 1111b
	P1_DIR_PU	93h	P1 port direction control and pull-up enable register	1111 1111b
	P1_MOD_OC	92h	P1 port output mode register	1111 1111b
	P4	C0h	P4 port input and output register	1111 1111b
	P3	B0h	P3 port input and output register	1111 1111b
	P2	A0h	P2 port input and output register	1111 1111b
	P1	90h	P1 port input and output register	1111 1111b
	P0	80h	P0 port input and output register	1111 1111b
	PORT_CFG	21EAh	Port interrupt and wakeup configuration and pull-down enable register	0000 0000b
	PIN_FUNC	21E9h	Pin function selection register	0000 0000b
	ANA_PIN	21E8h	Analog pin digital input disable register	0000 0000b
Timer/counter 0 and 1 registers	TH1	8Dh	Timer 1 count high byte	xxxx xxxxb
	TH0	8Ch	Timer 0 count high byte	xxxx xxxxb
	TL1	8Bh	Timer 1 count low byte	xxxx xxxxb
	TL0	8Ah	Timer 0 count low byte	xxxx xxxxb
	TMOD	89h	Timer0/1 mode register	0000 0000b
	TCON	88h	Timer0/1 control register	0000 0000b
UART0 registers	SBUF	99h	UART0 data register	xxxx xxxxb
	SCON	98h	UART0 control register	0000 0000b
Timer/counter 2 register	T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	xxxx xxxxb
	T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	xxxx xxxxb
	T2CAP1	CEh	T2CAP1L and T2CAP1H constitute a 16-bit SFR	xxxxh

	TH2	CDh	Timer 2 counter high byte	0000 0000b
	TL2	CCh	Timer 2 counter low byte	0000 0000b
	T2COUNT	CCh	TL2 and TH2 constitute a 16-bit SFR	0000h
	RCAP2H	CBh	Counting reload/capture 2 data register high byte	0000 0000b
	RCAP2L	CAh	Counting reload/capture 2 data register low byte	0000 0000b
	RCAP2	CAh	RCAP2L and RCAP2H constitutes 16-bit SFR	0000h
	T2MOD	C9h	Timer2 mode register	0000 0000b
	T2CON	C8h	Timer2 control register	0000 0000b
PWMX registers	PWM_DATA5	A5h	PWM5 data register	xxxx xxxxb
	PWM_DATA4	A4h	PWM4 data register	xxxx xxxxb
	PWM_DATA3	A3h	PWM3 data register	xxxx xxxxb
	PWM_CTRL2	9Fh	PWM extension control register	0000 0000b
	PWM_CK_SE	9Eh	PWM clock setting register	0000 0000b
	PWM_CTRL	9Dh	PWM control register	0000 0010b
	PWM_DATA0	9Ch	PWM0 data register	xxxx xxxxb
	PWM_DATA1	9Bh	PWM1 data register	xxxx xxxxb
	PWM_DATA2	9Ah	PWM2 data register	xxxx xxxxb
SPI0 registers	SPI0_SETUP	FCh	SPI0 setup register	0000 0000b
	SPI0_S_PRE	FBh	SPI0 slave mode preset data register	0010 0000b
	SPI0_CK_SE	FBh	SPI0 clock setting register	0010 0000b
	SPI0_CTRL	FAh	SPI0 control register	0000 0010b
	SPI0_DATA	F9h	SPI0 data receive/transmit register	xxxx xxxxb
	SPI0_STAT	F8h	SPI0 status register	0000 1000b
UART1 registers	SIF1	BFh	UART1 interrupt status register	0000 0000b
	SBAUD1	BEh	UART1 baud rate setting register	xxxx xxxxb
	SBUF1	BDh	UART1 data register	xxxx xxxxb
	SCON1	BCh	UART1 control register	0000 0000b
SPI1 registers	SPI1_CK_SE	B7h	SPI1 clock setting register	0010 0000b
	SPI1_CTRL	B6h	SPI1 control register	0000 0010b
	SPI1_DATA	B5h	SPI1 data receive/transmit register	xxxx xxxxb
	SPI1_STAT	B4h	SPI1 status register	0000 1000b
ADC/TKEY registers	ADC_CHAN	F6h	ADC analog signal channel selection register	0000 0000b
	TKEY_CTRL	F5h	Touch key charging impulse width control register (write only)	0000 0000b
	ADC_DAT_H	F5h	ADC result data high byte (read only)	0000 xxxxb
	ADC_DAT_L	F4h	ADC result data low byte (read only)	xxxx xxxxb
	ADC_DAT	F4h	ADC_DAT_L and ADC_DAT_H constitute a 16-bit SFR	0xxxh
	ADC_CTRL	F3h	ADC control and status register	x000 000xb
I2C global	I2CS_INT_ST	BBh	Mapping of I2CS slave status register	0000 1100b

and I2C host registers			I2CS_STAT	
	I2CX_INT	B3h	I2C and PWMX and RGB LED interrupt request register	0000 0000b
	I2CM_STAT	21C4h	I2CM host status register	0000 0000b
	I2CM_DATA	21C3h	I2CM host data register	xxxx xxxxb
	I2CM_START	21C2h	I2CM host start register	xxxx xxxxb
	I2CM_CK_SE	21C1h	I2CM host clock setting register	0000 0000b
	I2CM_CTRL	21C0h	I2CM host control register	000x 0000b
I2C slave registers	I2CS_STAT	223Ah	I2CS3 slave status register	0000 1100b
	I2CS_DATA	2236h	I2CS slave data receive/transmit register	xxxx xxxxb
	I2CS_ADDR	2235h	I2CS slave data address register (read-only)	xxxx xxxxb
	I2CS_DEV_A	2233h	I2CS slave device address register	0000 0000b
	I2CS_CTRL	2232h	I2CS slave control register	0000 0x00b
	I2CS_DMA_L	2139h	I2CS slave buffer start address low byte	xxxx xxxxb
	I2CS_DMA_H	2138h	I2CS slave buffer start address high byte	000x xxxxb
USB and global registers	UEP1_DMA_H	EFh	Endpoint 1 buffer start address high byte	000x xxxxb
	UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	xxxx xxxxb
	UEP1_DMA	EEh	UEP1_DMA_L and UEP1_DMA_H constitute a 16-bit SFR	xxxxh
	UEP0_DMA_H	EDh	Endpoint 0 and endpoint 4 buffer start address high byte	000x xxxxb
	UEP0_DMA_L	ECh	Endpoint 0 and endpoint 4 buffer start address low byte	xxxx xxxxb
	UEP0_DMA	ECh	UEP0_DMA_L and UEP0_DMA_H constitute a 16-bit SFR	xxxxh
	USB_HUB_ST	EBh	USB host root hub status register (read only)	0000 0000b
	UEP3_DMA_H	E7h	Endpoint 3 buffer start address high byte	000x xxxxb
	UEP3_DMA_L	E6h	Endpoint 3 buffer start address low byte	xxxx xxxxb
	UEP3_DMA	E6h	UEP3_DMA_L and UEP3_DMA_H constitute a 16-bit SFR	xxxxh
	UH_TX_DMA_H	E7h	USB host transmit buffer start address high byte	000x xxxxb
	UH_TX_DMA_L	E6h	USB host transmit buffer start address low byte	xxxx xxxxb
	UH_TX_DMA	E6h	UH_TX_DMA_L and UH_TX_DMA_H constitute a 16-bit SFR	xxxxh
	UEP2_DMA_H	E5h	Endpoint 2 buffer start address high byte	000x xxxxb
	UEP2_DMA_L	E4h	Endpoint 2 buffer start address low byte	xxxx xxxxb
	UEP2_DMA	E4h	UEP2_DMA_L and UEP2_DMA_H consitute a 16-bit SFR	xxxxh
	UH_RX_DMA_H	E5h	USB host receive buffer start address high byte	000x xxxxb
	UH_RX_DMA_L	E4h	USB host receive buffer start address low	xxxx xxxxb

			byte	
	UH_RX_DMA	E4h	UH_RX_DMA_L and UH_RX_DMA_H constitute a 16-bit SFR	xxxxh
	USB_DEV_AD	E3h	USB device address register	0000 0000b
	USB_CTRL	E2h	USB control register	0000 0110b
	UHUB23_CTRL	E1h	USB host root hub 2 and 3 port control register	0000 0000b
	UEP4_T_LEN	DFh	Endpoint 4 transmission length register	0000 0000b
	UEP4_CTRL	DEh	Endpoint 4 control register	0000 0000b
	UEP0_T_LEN	DDh	Endpoint 0 transmission length register	0000 0000b
	UEP0_CTRL	DCh	Endpoint 0 control register	0000 0000b
	USB_RX_LEN	DBh	USB reception length register (read only)	0xxx xxxxb
	USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
	USB_INT_ST	D9h	USB interrupt status register (read only)	0011 xxxxb
	USB_INT_FG	D8h	USB interrupt flag register	0000 0000b
	UEP3_T_LEN	D7h	Endpoint 3 transmission length register	0000 0000b
	UH_TX_LEN	D7h	USB host transmission length register	0000 0000b
	UEP3_CTRL	D6h	Endpoint 3 control register	0000 0000b
	UH_TX_CTRL	D6h	USB host transmission endpoint control register	0000 0000b
	UEP2_T_LEN	D5h	Endpoint 2 transmission length register	0000 0000b
	UH_EP_PID	D5h	USB host token setting register	0000 0000b
	UEP2_CTRL	D4h	Endpoint 2 control register	0000 0000b
	UH_RX_CTRL	D4h	USB host reception endpoint control register	0000 0000b
	UEP1_T_LEN	D3h	Endpoint 1 transmission length register	0000 0000b
	UEP1_CTRL	D2h	Endpoint 1 control register	0000 0000b
	UH_SETUP	D2h	USB host auxiliary setting register	0000 0000b
	UDEV_CTRL	D1h	USB device port control register	0000 0000b
	UHOST_CTRL	D1h	USB host port control register	0000 0000b
	UHUB01_CTRL	D1h	USB host root hub 0 and 1 port control register	0000 0000b
	USB_INT_EN	21E2h	USB interrupt enable register	0000 0000b
	UEP2_3_MOD	21E1h	Endpoint 2, 3 mode control register	0000 0000b
	UH_EP_MOD	21E1h	USB host endpoint mode control register	0000 0000b
	UEP4_1_MOD	21E0h	Endpoint 1, 4 mode control register	0000 0000b
RGB LED registers	LED_STATUS	F7h	RGB LED status register	0001 xxxxb
	LED_DMA_H	C7h	RGB LED buffer current address high byte	xxxx xxxxb
	LED_DMA_L	C6h	RGB LED buffer current address low byte	xxxx xxxxb
	LED_DMA	C6h	LED_DMA_L and LED_DMA_H constitute a 16-bit SFR	xxxxh
	LED_PWM_OE	A7h	RGB LED drive PWM pin enable register	0000 0000b

	LED_COMMON	A6h	RGB LED drive COMMON pin selection register	0000 0000b
	LED_COL_CNT	21DDh	RGB LED color counter register (read only)	0000 0000b
	LED_FRA_STA	21DCh	RGB LED frame status register (read only)	0000 0000b
	LED_BLU_ADJ	21DBh	RGB LED blue adjustment register	0000 0000b
	LED_GRE_ADJ	21DAh	RGB LED green adjustment register	0000 0000b
	LED_RED_ADJ	21D9h	RGB LED red adjustment register	0000 0000b
	LED_INT_ADJ	21D8h	RGB LED brightness adjustment register	0000 0000b
	LED_FRAME	21D3h	RGB LED frame configuration register	0000 0000b
	LED_CYCLE	21D2h	RGB LED cycle configuration register	0000 0000b
	LED_CTRL	21D1h	RGB LED control register	0000 0000b

5.3 General-purpose 8051 register

Table 5.3.1 General-purpose 8051 registers

Name	Address	Description	Reset value
A_INV	FDh	Inverted value of accumulator high bit and low bit	00h
B	F0h	B register	00h
A, ACC	E0h	Accumulator	00h
PSW	D0h	Program status word register	00h
GLOBAL_CFG	B1h	Global configuration register (in CH557 boot loader state)	60h
		Global configuration register (in CH557 application program state)	40h
		Global configuration register (in CH556 boot loader state)	20h
		Global configuration register (in CH556 application program state)	00h
CHIP_ID	A1h	ID code of CH557 (read-only)	57h
		ID code of CH556 (read-only)	56h
SAFE_MOD	A1h	Safe mode control register (read only)	00h
PCON	87h	Power supply control register (in power on reset state)	10h
DPH	83h	Data address pointer high 8 bits	00h
DPL	82h	Data address pointer low 8 bits	00h
DPTR	82h	DPL and DPH constitute a 16-bit SFR	0000h
SP	81h	Stack pointer	07h

B register (B):

Bit	Name	Access	Description	Reset value
[7:0]	B	RW	Arithmetic operation register, mainly used for multiplication and division operations, accessed by bits.	00h

A accumulator (A, ACC):

Bit	Name	Access	Description	Reset value
[7:0]	A/ACC	RW	Arithmetic operation accumulator, accessed by bits	00h

Program status word register (PSW):

Bit	Name	Access	Description	Reset value
7	CY	RW	Carry flag bit, used to record the carry or borrow of the highest bit when performing arithmetic operations and logical operations. In 8-bit addition operation, this bit is set if the highest bit is carried, otherwise it is cleared. In 8-bit subtraction operation, this bit is set if the highest bit is borrowed, otherwise it is cleared. Logical command can set and reset this bit.	0
6	AC	RW	Auxiliary carry flag bit. In addition and subtraction operations, if there is a carry or borrow from the higher 4 bits to the lower 4 bits, then AC is set, otherwise it is reset.	0
5	F0	RW	General flag bit 0, accessed by bits. User-defined. Set and reset by software.	0
4	RS1	RW	Register bank selection high bit	0
3	RS0	RW	Register bank selection low bit	0
2	OV	RW	Overflow flag bit. In addition and subtraction operations, if the operation result exceeds 8-bit binary number, OV is set to 1 and the flag overflows, otherwise it is reset.	0
1	F1	RW	Addressable common flag bit 1 by bit: the users can define it by their own, and reset or set by software	0
0	P	RO	Parity flag bit. This bit records the parity of '1' in accumulator A after the command is executed. If the number of '1' is an odd number, P is set. If the number of '1' is an even number, P is reset.	0

The state of processor is stored in the program status word register (PSW), and PSW can be accessed by bits. The status word includes the carry flag bit, auxiliary carry flag bit for BCD code processing, parity flag bit, overflow flag bit, as well as RS0 and RS1 for working register bank selection.The area where the working register bank is located can be accessed directly or indirectly.

Table 5.3.2 RS1 and RS0 working register bank selection table

RS1	RS0	Working register bank
0	0	Bank 0 (00h-07h)
0	1	Bank 1 (08h-0Fh)
1	0	Bank 2 (10h-17h)
1	1	Bank 3 (18h-1Fh)

Table 5.3.3 Operations that affect flag bits (X indicates that the flag bit is related to the operation result)

Operation	CY	OV	AC	Operation	CY	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		
MUL	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
DA A	X			ANL C,/bit	X		
RRC A	X			ORL C, bit	X		
RLC A	X			ORL C,/bit	X		
CJNE	X						

Data address pointer (DPTR):

Bit	Name	Access	Description	Reset value
[7:0]	DPL	RW	Data pointer low byte	00h
[7:0]	DPH	RW	Data pointer high byte	00h

DPL and DPH constitute a16-bit data pointer (DPTR), which is used to access xSFR, xBUS, xRAM data memory and program memory. The actual DPTR corresponds to 2 sets of physical 16-bit data pointers, DPTR0 and DPTR1, which are dynamically selected by DPS in XBUS_AUX.

Stack pointer (SP):

Bit	Name	Access	Description	Reset value
[7:0]	SP	RW	Stack pointer, mainly used for program calls and interrupt calls as well as data in and out of the stack	07h

Specific function of stack: protect breakpoint and protect site, and carry out management on the first-in last-out principle. During instack, SP pointer automatically adds 1, saving the data and breakpoint information. During outstack, SP pointer points to the data unit and automatically substracts 1. The initial value of SP is 07h after reset, and the corresponding default stack storage starts from 08h.

5.4 Special registers

Inverted value of accumulator high bit and low bit (A_INV):

Bit	Name	Access	Description	Reset value
[7:0]	A_INV	RO	Inverted value of accumulator high bit and low bit, result of bit 0 ~ bit 7 in bitwise reverse order. Bit 7 and bit 6 ~ bit 0 of A_INV correspond to bit 0 and bit 1 ~ bit 7 of ACC respectively.	00h

Global configuration register (ACC), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	For CH557, it is always 01.	01b
[7:6]	Reserved	RO	For CH556, it is always 00.	00b
5	bBOOT_LOAD	RO	Boot loader status bit, used to distinguish ISP boot loader state or application state. Set to 1 during power on. Reset during software reset. For the chip with ISP boot loader, if this bit is 1, it has never been reset by software and it is usually in ISP boot loader running after power on state. If this bit is 0, it has been reset by software, and it is usually in application state.	1
4	bSW_RESET	RW	Software reset control bit. If it is set to 1, software reset occurs. Automatically reset by hardware.	0
3	bCODE_WE	RW	Flash-ROM write enable bit Write protection if this bit is 0. Flash-ROM can be written and erased if this bit is 1	0
2	bDATA_WE	RW	Flash-ROM DataFlash area write enable bit Write protection if this bit is 0. DataFlash area can be written and erased if this bit is 1	0
1	bXIR_XSFR	RW	MOVX_@R0/R1 commands access range control bit: If this bit is 0, all xRAM/xSFR in xdata area can be accessed. If this bit is 1, it's dedicated to accessing xSFR rather than xRAM.	0
0	bWDOG_EN	RW	Watchdog reset enable bit If this bit is 0, watchdog is only used as a timer. If this bit is 1, watchdog reset enabled when timing overflows.	0

ID code of chip (CHIP_ID):

Bit	Name	Access	Description	Reset value
[7:0]	CHIP_ID	RO	For CH557, always 57h, used to identify the chip	57h
[7:0]	CHIP_ID	RO	For CH556, always 56h, used to identify the chip	56h

Safe mode control register (SAFE_MOD):

Bit	Name	Access	Description	Reset value
[7:0]	SAFE_MOD	WO	Used to enter and terminate safe mode	00h

Some SFRs can only be written in safe mode, while they are always read-only in non-safe mode. Steps for entering safe mode:

(1). Write 55h into this register.

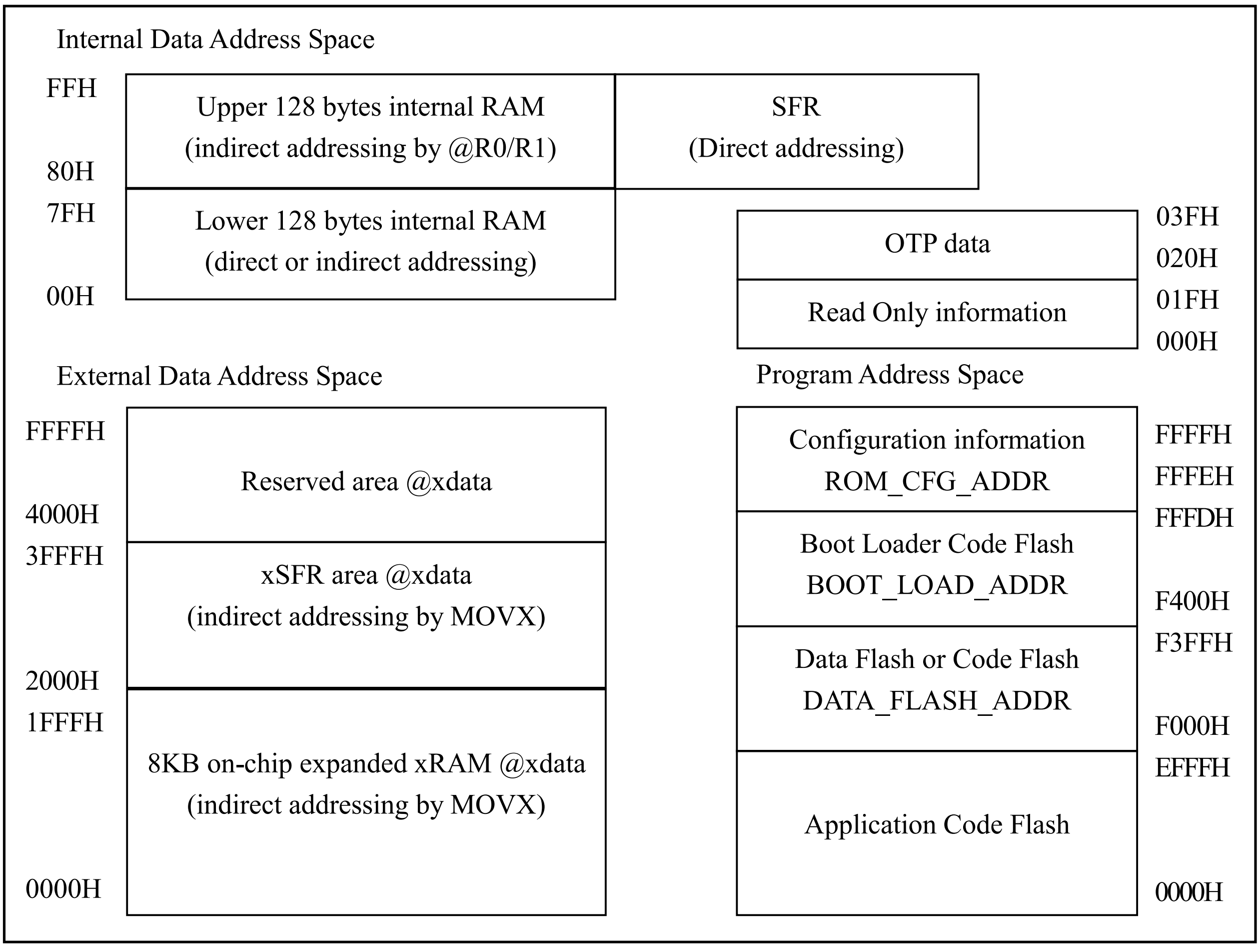
(2). And then write AAh into this register.
(3). After that, they are in safe mode for about 13 to 23 system clock cycles, and one or more safe class SFR or ordinary SFR can be rewritten in such validity period.
(4). Automatically terminate the safe mode after the expiration of the above validity period.
(5). Alternatively, write any value to the register to prematurely terminate safe mode.

6. Memory structure

6.1 Memory space

CH557 addressing space is divided into program address space, internal data address space, external data address space, read only information and OTP data space.

Figure 6.1 Memory structure diagram



6.2 Program address space

The program address space is 64KB in total, as shown in Figure 6.1, all of which is used for flash-ROM, including the Code Flash area to save the command code, the Data Flash area to save the non-volatile data, and the Configuration Information area.

Data Flash (EEPROM) address ranges from F000h to F3FFH. It supports single byte read (8 bits), single byte write (8 bits), block write (1 ~ 64 bytes), block erase (64 bytes) operations. The data remains unchanged after power failure of chip, and it can also be used as Code Flash.

Code Flash includes the application code for the low address area and the boot loader code for the high address area, or these two areas and Data Flash may be combined to save a single application code.

Configuration information area has 16 bits of data, which is set by the programmer as required, refer to Table 6.1.

Table 6.2 flash-ROM configuration information description

Bit address	Bit name	Description	Recommended value
15	Code_Protect	flash-ROM code and data protection mode: 0: Read enabled; 1: Disable the programmer to read out, and keep the program secret	0/1
14	No_Boot_Load	Enable BootLoader start mode 0: Start from the application from 0000h address. 1: Start from the boot loader from F400h address.	1
13	En_Long_Reset	Extra delay reset during enable power on reset: 0: Standard short reset; 1: Wide reset, with extra 44mS reset time added	0
12	En_P71_RESET	Enable P7.1 as manual reset input pin: 0: Disable. 1: RST# enabled.	0
11		Reserved	0
10		Reserved	0
9	Must_1	(Automatically set to 1 by the programmer as required)	1
8	Must_0	(Automatically set to 0 by the programmer as required)	0
[7:3]	All_0	(Automatically set to 00000b by the programmer as required)	00000b
[2:0]	LV_RST_VOL (Vpot)	Select the threshold voltage of power supply low voltage detection reset (LVR) module (error 5%): 000: Select 2.5V. 001: Select 2.7V. 010: Select 2.9V. 011: Select 3.1V. 100: Select 3.9V. 101: Select 4.1V. 110: Select 4.3V. 111: Select 4.5V.	000b

6.3 Data address space

The internal data storage space, with 256 bytes in total, as shown in Figure 6.1, has been all used for SFR and iRAM, in which iRAM is used for stack and fast temporary data storage, and can be subdivided into the working registers R0-R7, bit variable bdata, byte variable data and idata, etc.

External data storage space is 64KB in total, as shown in Figure 6.1. Except that part of it is used for 16 KB on-chip expanded xRAM and xSFR, the remaining 4000h to FFFFh addresses are reserved.

Read-only information area and OTP data area each has 32 bytes, as shown in Figure 6.1, and needs to be accessed through a dedicated operation.

6.4 flash-ROM register

Table 6.4 flash-ROM operation registers

Name	Address	Description	Reset value
ROM_DATA_HH	8Fh	High byte of flash-ROM data register high word (read only)	xxh
ROM_DATA_HL	8Eh	Low byte of flash-ROM data register high word (read only)	xxh
ROM_DATA_HI	8Eh	ROM_DATA_HL and ROM_DATA_HH constitute a 16-bit SFR	xxxxh
ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase/program operation	xxh
ROM_DAT_BUF	8Eh	Data butter register for flash-ROM erase/program operation	xxh
ROM_STATUS	86h	flash-ROM status register (read only)	00h
ROM_CTRL	86h	flash-ROM control register (read only)	00h
ROM_ADDR_H	85h	flash-ROM address register high byte	xxh
ROM_ADDR_L	84h	flash-ROM address register low byte	xxh
ROM_ADDR	84h	ROM_ADDR_L and ROM_ADDR_H constitute a 16-bit SFR	xxxxh
ROM_DATA_LH	85h	High byte of flash-ROM data register low word (read only)	xxh
ROM_DATA_LL	84h	Low byte of flash-ROM data register low word (read only)	xxh
ROM_DATA_LO	84h	ROM_DATA_LL and ROM_DATA_LH constitute a 16-bit SFR	xxxxh

flash-ROM address register (ROM_ADDR):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_ADDR_H	RW	flash-ROM address high byte	xxh
[7:0]	ROM_ADDR_L	RW	flash-ROM address low byte	xxh

flash-ROM data register (ROM_DATA_HI, ROM_DATA_LO):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DATA_HH	RO	High byte of flash-ROM data register high word (16 bits)	xxh
[7:0]	ROM_DATA_HL	RO	Low byte of flash-ROM data register high word (16 bits)	xxh
[7:0]	ROM_DATA_LH	RO	High byte of flash-ROM data register low word (16 bits)	xxh
[7:0]	ROM_DATA_LL	RO	Low byte of flash-ROM data register low word (16 bits)	xxh

Buffer mode register for flash-ROM erase/program operation (ROM_BUF_MOD):

Bit	Name	Access	Description	Reset value
7	bROM_BUF_BYTE	RW	Buffer mode for flash-ROM write operation (erase or program): 0: Select the data block programming mode, and the data to be written is stored in xRAM pointed to by DPTR. During programming, CH557 automatically fetches data from xRAM in sequence and temporarily store it in ROM_DAT_BUF and then write into flash-ROM. It supports 1 to 64 bytes of data, and the actual length =MASK_ROM_ADR_END-ROM_ADDR_L[5:0]+1; 1: Select single-byte programming or 64-byte block erase mode, and the data to be written is directly stored in ROM_DAT_BUF.	x
6	Reserved	RW	Reserved	x
[5:0]	MASK_ROM_ADDR	RW	Lower 6 bits of the end address of the flash-ROM block programming operation (including such address) in flash-ROM data block programming mode. Reserved in flash-ROM single byte programming or 64-byte erase mode, and recommended to be 00h.	xxh

Data buffer register for flash-ROM erase/program operation (ROM_DAT_BUF):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DAT_BUF	RW	Data butter register for flash-ROM erase/program operation	xxh

flash-ROM control register (ROM_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_CTRL	WO	flash-ROM control register	00h

flash-ROM status register (ROM_STATUS):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	1
6	bROM_ADDR_OK	RO	flash-ROM operation address OK status bit: 0: Invalid. 1: Address is valid.	0
[5:2]	Reserved	RO	Reserved	0000b

1	bROM_CMD_ERR	RO	flash-ROM operation command error status bit: 0: Command is valid. 1: Unknown command, or overtime	0
0	Reserved	RO	Reserved	0

6.5 flash-ROM operation steps

1. Erase the flash-ROM, and change all data bits in the target block to 0:

(1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(2). Set the global configuration register (GLOBAL_CFG) to start write enable (bCODE_WE or bDATA_WE corresponds to code or data).

(3). Set the address register (ROM_ADDR), to write a 16-bit target address, actually only the higher 10 bits are valid.

(4). Set the buffer mode register for erase/program operation (ROM_BUF_MOD) to 80h, to select the 64-byte block erase mode.

(5). Optional, set the data buffer register for erase/program operation (ROM_DAT_BUF) to 00h.

(6). Set the operation control register (ROM_CTRL) to 0A6h, to execute block erase operation and the program is automatically suspended during operation.

(7). After the operation is completed, the program resumes running. In this case, you can inquire the status register (ROM_STATUS) to check the status of the operation. If more than one block needs to be erased, repeat the steps of (3), (4), (5), (6) and (7). The sequence of step (3), (4), and (5) can be exchanged.

(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0).

2. Write flash-ROM in single byte, change some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):

(1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(2). Set the global configuration register (GLOBAL_CFG) to start write enable (bCODE_WE or bDATA_WE corresponds code or data).

(3). Set the address register (ROM_ADDR) to write a 16-bit target address.

(4). Set the buffer mode register for erase/program operation (ROM_BUF_MOD) to 80h, to select the single byte programming mode.

(5). Set the data buffer register for erase/program operation (ROM_DAT_BUF) to the byte data to be written.

(6). Set the operation control register (ROM_CTRL) to 09Ah, to execute write operation, and the program is automatically suspended during operation.

(7). After the operation is completed, the program resumes running. In this case, you can inquire the status register (ROM_STATUS) to check the status of the operation. If more than one block data needs to be written, repeat the steps of (3), (4), (5), (6) and (7). The sequence of step (3), (4), and (5) can be exchanged.

(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0).

3. Block write flash-ROM, change some data bits in multiple target bytes from 0 to 1 (the bit data cannot be changed from 1 to 0):

(1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(2). Set the global configuration register GLOBAL_CFG start write enabling (bCODE_WE or bDATA_WE corresponds to code or data).

(3). Set the address register (ROM_ADDR), to write a 16-bit start target address, such as 1357h.

(4). Set the buffer mode register for erase/program operation (ROM_BUF_MOD to the lower 6 bits of the end target address (including), and such end address should be greater than or equal to the ROM_ADDR_L[5:0] start target address, select the data block programming mode, for example, if the end address is 1364h, the ROM_BUF_MOD should be set to 24h (64H &3Fh), and the calculated number of bytes of the data block =0Dh.

(5). In the xRAM, allocate a buffer area based on the alignment in 64 bytes, for example 0580h～05BFh, specify the offset address in such buffer area with the lower 6 bits of the start target address, obtain the xRAM buffer start address of this data block programming operation, store the data block to be written from the xRAM buffer start address, and set the xRAM buffer start address into DPTR, e.g. DPTR=0580h+(57h&3Fh)=0597h, actually only the xRAM of 0597h ~ 05A4h address is used in this programming operation.

(6). Set the operation control register (ROM_CTRL) to 09Ah, to execute write operation, and the program is automatically suspended during operation.

(7). After the operation is completed, the program resumes running. In this case, you can inquire the status register (ROM_STATUS) to check the status of the operation. If more than one block data needs to be written, repeat the steps of (3), (4), (5), (6) and (7). The sequence of step (3), (4), and (5) can be exchanged.

(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0).

4. Read flash-ROM:

Directly use MOVC command, or read the code or data of the target address through the pointer to the program address space.

5. Write to OTP data area in single byte, change some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):

(1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(2). Set the global configuration register (GLOBAL_CFG) to start write enable (bDATA_WE).

(3). Set the address register (ROM_ADDR), to write the target address (20h～3Fh), actually only the higher 4 bits in the lower 6 bits are valid.

(4). Set the buffer mode register for erase/program operation (ROM_BUF_MOD) to 80h, to select the single byte programming mode;

(5). Set the data buffer register for erase/program operation (ROM_DAT_BUF) to the byte data to be written.

(6). Set the operation control register (ROM_CTRL) to 099h, to execute write operation, and the program is automatically suspended during operation.

(7). After the operation is completed, the program resumes running. In this case, you can inquire the status register (ROM_STATUS) to check the status of the operation. If more than one block data needs to be written, repeat the steps of (3), (4), (5), (6) and (7). The sequence of step (3), (4), and (5) can be exchanged.

(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(9). Set the global configuration register (GLOBAL_CFG) to start write protection (bCODE_WE=0, bDATA_WE=0).

6. Read the ReadOnly information area or OTP data area in 4 bytes:

(1). Set the address register (ROM_ADDR), to write the target address based on the alignment in 4 bytes (00h～3Fh), actually only the lower 6 bits are valid.

(2). Set the operation control register (ROM_CTRL) to 08Dh, to execute read operation, and the program is automatically suspended during operation.

(3). After the operation is completed, the program resumes running. In this case, you can inquire the status register (ROM_STATUS) to check the status of the operation.

(4). Obtain 4-byte data from ROM_DATA_HI and ROM_DATA_LO in flash-ROM data register.

7. Notes: it is recommended that flash-ROM/EEPROM is erased/programmed only at the ambient temperature of -20℃ ~ 85℃. If the erase/program operation is performed beyond the above temperature range, it is normal usually, but there may be the possibility of reducing data retention ability TDR and reducing the number of erase/program operations (NEPCE) or even affecting the accuracy of data.

6.6 On-board program and ISP download

When Code_Protect=0, the codes and data in CH557 flash-ROM can be read and written by an external programmer through the synchronous serial interface. When Code_Protect=1, the codes and data in the flash-ROM are protected and cannot be read out, but can be erased, and the code protection is removed after erased and powered on again.

When CH557 is preset with BootLoader program, it supports various ISP download types such as USB or UART to load the applications. But in the absence of a boot loader program, the boot loader program or application can only be written to CH557 by an external dedicated programmer. To support on-board program, 4 connection pins between the CH557 and the programmer should be reserved in the circuit. The necessary connecting pins are P1.4, P1.6 and P1.7.

Table 6.6.1 Connection pins to the programmer

Pin	GPIO	Pin description
VDD	VDD	It is required to control chip power in programming state.
SCS	P1.4	Chip Select input pin (necessary) in programming state. High level by default, active at low level.
SCK	P1.7	Clock input pin (necessary) in programming state
MISO	P1.6	Data output pin (necessary) in programming state

6.7 Unique ID

Each MCU has a unique ID number when it is delivered from the factory, namely the chip identification number. This ID data and its checksum has 8 bytes in total, stored in the read-only information area at 10h offset address, please refer to the C Program Language Example routines for specific operations.

Table 6.7.1 Chip ID address table

Offset address	ID data description
10h, 11h	ID first word data, correspond to the lowest byte and the second low byte of the ID number in order
12h, 13h	ID secondary word data, correspond to the second high byte and high byte of the ID number in order
14h, 15h	ID last word data, correspond to the second highest byte and the highest byte of the 48-bit ID number in order
16h, 17h	16-bit cumulative sum of ID first word, secondary word, last word data, used for ID check

The ID number can be used with the download tools to encrypt the target program. For the general application, only the first 32 bits of the ID number are used.

7. Power control, sleep and reset

7.1 External power input

CH557 has a built-in 5V to 3.3V low dropout voltage regulator (LDO), and the generated 3.3V power supply is used in USB and other modules. CH557 supports external 5V or 3.3V or even 2.8V supply voltage input. Refer to the following table for the two supply voltage input modes.

External supply voltage	VDD pin voltage: 2.8V to 5V external voltage	V33 pin voltage: 3.3V internal USB voltage (Notes: V33 is automatically shorted to VDD during sleep)
3.3V or 2.8V including less than 3.6V	Input external 3.3V voltage to I/O and voltage regulator. Must be connected with a decoupling capacitor (not less than 0.1uF) to ground.	VDD input shorted as the internal USB power Must be connected with a decoupling capacitor (not less than 0.1uF) to ground.
5V including more than 3.6V	Input external 5V voltage to I/O and voltage regulator. Must be connected with a decoupling capacitor (not less than 0.1uF) to ground.	Internal voltage regulator 3.3V output and 3.3V internal USB power input, Must be connected with a decoupling capacitor (not less than 0.1uF) to ground.

After power on or system reset, CH557 is in running state by default. On the premise that the performance meets the requirements, the power consumption can be reduced during operation by appropriately reducing the system clock frequency. When CH557 does not need to run at all, PD in PCON can be set to enter the Sleep mode. In Sleep mode, external wakeup can be implemented via USB, UART0, UART1, SPI0 and part of GPIO.

7.2 Power supply and sleep control register

Table 7.2.1 Power supply and sleep control registers

Name	Address	Description	Reset value
WDOG_COUNT	FFh	Watchdog count register	00h
RESET_KEEP	FEh	Reset keep register	00h

POWER_CFG	BAh	Power management configuration register	0xh
WAKE_CTRL	A9h	Wakeup control register	00h
PCON	87h	Power control register	10h
CMP_DCDC	21EBh	Comparator and DC-DC control register	00h

Watchdog count register (WDOG_COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	WDOG_COUNT	RW	Current count of watchdog. It overflows when the count is full from 0FFh to 00h, and the bWDOG_IF_TO interrupt flag is automatically set to 1 during overflow	00h

Reset keep register (RESET_KEEP):

Bit	Name	Access	Description	Reset value
[7:0]	RESET_KEEP	RW	Reset keep register. The value can be modified manually and will not be affected by any other reset except for power on reset	00h

Power management configuration register (POWER_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bPWR_DN_MODE	RW	Sleep power down mode selection: 0: Select the power-down/deep-sleep mode, and it can save more power but wake up slowly. 1: Select Standby/normal Sleep mode, it can wake up quickly.	0
6	bCMP_RESULT	RO	Voltage comparator result output bit 0: The input voltage is lower than the reference voltage. 1: The input voltage is higher than the reference voltage.	0
5	bLV_RST_OFF	RW	Low voltage reset detection module OFF control 0: Supply voltage detection ON, and reset signal is generated when at low voltage. 1: Low voltage detection OFF.	0
4	bLDO_3V3_OFF	RW	LDO OFF control (auto OFF during sleep): 0: 3.3V voltage is generated by VDD for USB and other modules. 1: LDO OFF, and V33 is internally shorted to VDD.	0
3	bLDO_CORE_VOL	RW	Core voltage mode: 0: Normal voltage mode. 1: Boost voltage mode, which has better performance and support higher clock frequency.	0
[2:0]	MASK_ULLDO_VOL	RW	Data retention supply voltage selection in power down/deep sleep mode:	xxxb

			000: Select 1.5V. 001: Select 1.57V. 010: Select 1.64V. 011: Select 1.71V. 100: Select 1.78V. 101: Select 1.85V. 110: Select 1.92V. 111: Select 1.99V. The above values are for reference only and not recommended to modify.	

Wakeup control register (WAKE_CTRL), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bWAK_BY_USB	RW	USB event wakeup enable Wakeup is disabled if the bit is 0.	0
6	bWAK_RXD1_LO	RW	UART1 receive input low level wakeup enable Wakeup is disabled if the bit is 0. Select either RXD1 or RXD1_ based on bUART1_PIN_X=0/1	0
5	bWAK_P1_5_LO	RW	P1.5 low level wakeup enable Wakeup is disabled if the bit is 0.	0
4	bWAK_P1_4_LO	RW	P1.4 low level wakeup enable Wakeup is disabled if the bit is 0.	0
3	Reserved	RO	Reserved	0
2	bWAK_P3_3_LO	RW	P3.3 low level wakeup enable Wakeup is disabled if the bit is 0.	0
1	bWAK_INT0_EDGE	RW	INT0 edge change wakeup enable Wakeup is disabled if the bit is 0. Select either INT0 or INT0_ pin based on bINT0_PIN_X=0/1	0
0	bWAK_RXD0_LO	RW	UART0 receive input low level wakeup enable Wakeup is disabled if the bit is 0. Select either RXD0 or RXD0_ pin based on bUART0_PIN_X=0/1	0

Other signal sources that can wake up the chip include:

When bP4_IE_LEVEL is 1, the level change on any one of P4.0 to P4.7 pins can wake up the chip.

When bP2L_IE_LEVEL is 1, the level change on any one of P2.0 to P2.3 pins can wake up the chip.

When bP1L_IE_LEVEL is 1, the level change on any one of P1.0 to P1.3 pins can wake up the chip.

When bP0_IE_LEVEL is 1, the level change on any one of P0.0 to P0.7 pins can wake up the chip.

When En_P71_RESET is 1, enable RST#, and the low level on P7.1 pin can wake up and reset the chip.

Power control register (PCON):

Bit	Name	Access	Description	Reset value
7	SMOD	RW	When the UART0 baud rate is generated by timer 1, select the communication baud rate of UART0 mode 1, 2 and 3:	0

			0: Slow mode; 1: Fast mode	
6	Reserved	RO	Reserved	0
5	bRST_FLAG1	R0	Last reset flag high bit	0
4	bRST_FLAG0	R0	Last reset flag low bit	1
3	GF1	RW	General flag bit 1 User-defined. Reset and set by software.	0
2	GF0	RW	General flag bit 0 User-defined. Reset and set by software.	0
1	PD	RW	Sleep mode enable Sleep after set to 1. Automatically reset by hardware after wakeup. It is strongly recommended to disable the global interrupt before sleep (EA=0).	0
0	Reserved	RO	Reserved	0

Table 7.2.2 Last reset flag description

bRST_FLAG1	bRST_FLAG0	Reset flag description
0	0	Software reset Source: bSW_RESET=1 and (bBOOT_LOAD=0 or bWDOG_EN=1).
0	1	Power on reset or low voltage detection reset Source: voltage on VDD pin is lower than detection level.
1	0	Watchdog reset Source: bWDOG_EN=1 and watchdog timeout overflows.
1	1	External pin manual reset Source: En_P71_RESET=1 and P71 input low level.

Comparator and DC-DC control register (CMP_DCDC):

Bit	Name	Access	Description	Reset value
7	bDCDC_ACT	RO	DC-DC output activate state (read only): 0: Free. 1: The driver is being activated.	0
6	bDCDC_PIN	RW	DC-DC output pin and polarity selection: 0: Only DCO pin outputs bDCDC_ACT signal. 1: DCO pin outputs bDCDC_ACT negative polarity signal, and P6.4 pin outputs bDCDC_AC signal whose polarity is controlled by P6_OUT_PU[4]. When P6_OUT_PU[4]=0, output the positive polarity. When P6_OUT_PU[4]=1, output the negative polarity.	0
[5:4]	MASK_DCDC_FREQ	RW	When MASK_CMP_VREF!=000, select the reference frequency of DC-DC controller (the actual maximum output frequency is 1/3 of the reference frequency): 00: DC-DC controller OFF.	00b

			01: 3MHz selected as reference frequency. 10: 1.5MHz selected as reference frequency. 11: 750KHz selected as reference frequency. When MASK_CMP_VREF=000, directly control bDCDC_ACT state: 00: Set bDCDC_ACT=0. 01/10/11: Set bDCDC_ACT=1	
3	bCMP_PIN	RW	Input voltage source selection of voltage comparator (positive phase input): 0: Select the divided input VDD power supply. 1: Select to connect to analog input channel via voltage divider, share with ADC/TKEY, the external input pin is selected by ADC_CHAN, and bADC_EN=1.	0
[2:0]	MASK_CMP_VREF	RW	Reference voltage selection of comparator (inverted input): 000: Comparator OFF. 001: Select internal reference voltage, around 1.2V. 010: Select 3.3V. 011: Select 5V. 100: Select 5.4V. 101: Select 5.8V. 110: Select 6.2V. 111: Select 6.6V.	000b

The inverted input of the voltage comparator (CMP) is selected by MASK_CMP_VREF for the reference voltage, actually the reference voltage remains unchanged, while adjust the voltage divider of the positive phase input to simulate the selection equivalent to the reference voltage. Due to the existence of the voltage divider, the impedance of the positive phase input is between 50KΩ and 150KΩ, and the CMP is generally used for supply voltage supervisor and DC-DC control.

7.3 Reset control

CH557 has 5 reset sources: power on reset, power supply low voltage reset, external reset, software reset, and watchdog reset.The last three are thermal reset.

7.3.1 Power on reset and power supply low voltage reset

The power on reset (POR) is generated by the on-chip power on detection circuit. Automatically delay Tpor through hardware to keep reset. After the delay, the CH557 runs.

Low voltage reset (LVR) is generated by the on-chip voltage detection circuit. The LVR circuit continuously monitors the supply voltage on VDD pin. When it is lower than the detection level (Vpot), the low voltage reset is generated. Automatically delay Tpor through hardware to keep reset. After the delay, the CH557 runs.

Only power on reset and power supply low voltage reset can enable CH557 to reload the configuration information and reset RESET_KEEP, other thermal resets do not affect it.

7.3.2 External reset

The external reset is generated by the low level applied to the RST# pin. The reset process is triggered when En_P71_RESET is 1, and the low level duration on the RST# pin is greater than Trst. When the external low level signal is canceled, the hardware will automatically delay Trdl to remain the reset state. After the delay, CH557 will be executed from address 0.

Notes: The RST# pin is also the XO pin of the external crystal oscillator. It is necessary to avoid long wire which may cause additional capacitance or introduce interference.

7.3.3 Software reset

CH557 supports internal software reset, so that the CPU can be actively reset and re-run without external intervention. Set bSW_RESET in global configuration register (GLOBAL_CFG) to 1 to reset the software, and automatically delay Trdl to keep reset. After the delay, CH557 executes from address 0, and the bSW_RESET bit is reset automatically by hardware.

When bSW_RESET is set to 1, if bBOOT_LOAD=0 or bWDOG_EN=1, then bRST_FLAG1/0 after reset will indicate a software reset. When bSW_RESET is set to 1, if bBOOT_LOAD=1 and bWDOG_EN=0, then bRST_FLAG1/0 remains the previous reset flag rather than generate a new one.

For a chip with ISP boot loader, after power on reset, firstly run the boot loader, and the program will reset the chip via software as needed to switch to the application state; such software reset only cause reset of bBOOT_LOAD, and do not affect bRST_FLAG1/0 state (due to bBOOT_LOAD = 1 before reset), so when switching to the application state, bRST_FLAG1/0 still indicates the power on reset state.

7.3.4 Watchdog reset

Watchdog reset is generated when the watchdog timer overflows. The watchdog timer is an 8-bit counter, whose count clock frequency is Fsys/131072, and the overflow signal is generated when the count reaches 0FFh to 00h.

The watchdog timer overflow signal triggers the interrupt flag (bWDOG_IF_TO) to 1, which is automatically reset when WDOG_COUNT is reloaded or inputting the corresponding interrupt service program.

Different timing cycles (Twdc) are achieved by writing different count initial values to WDOG_COUNT. When the system clock frequency is 12MHz, the watchdog timing cycle (Twdc) is about 2.8 s when 00h is written, and about 1.4 s when 80h is written.

If bWDOG_EN=1 when watchdog timer overflows, watchdog reset is generated and automatically delay Trdl to keep reset. After the delay, CH557 executes from address 0.

When bWDOG_EN=1, to avoid watchdog reset, WDOG_COUNT must be reset timely to avoid its overflow.

8. System clock

8.1 Clock block diagram

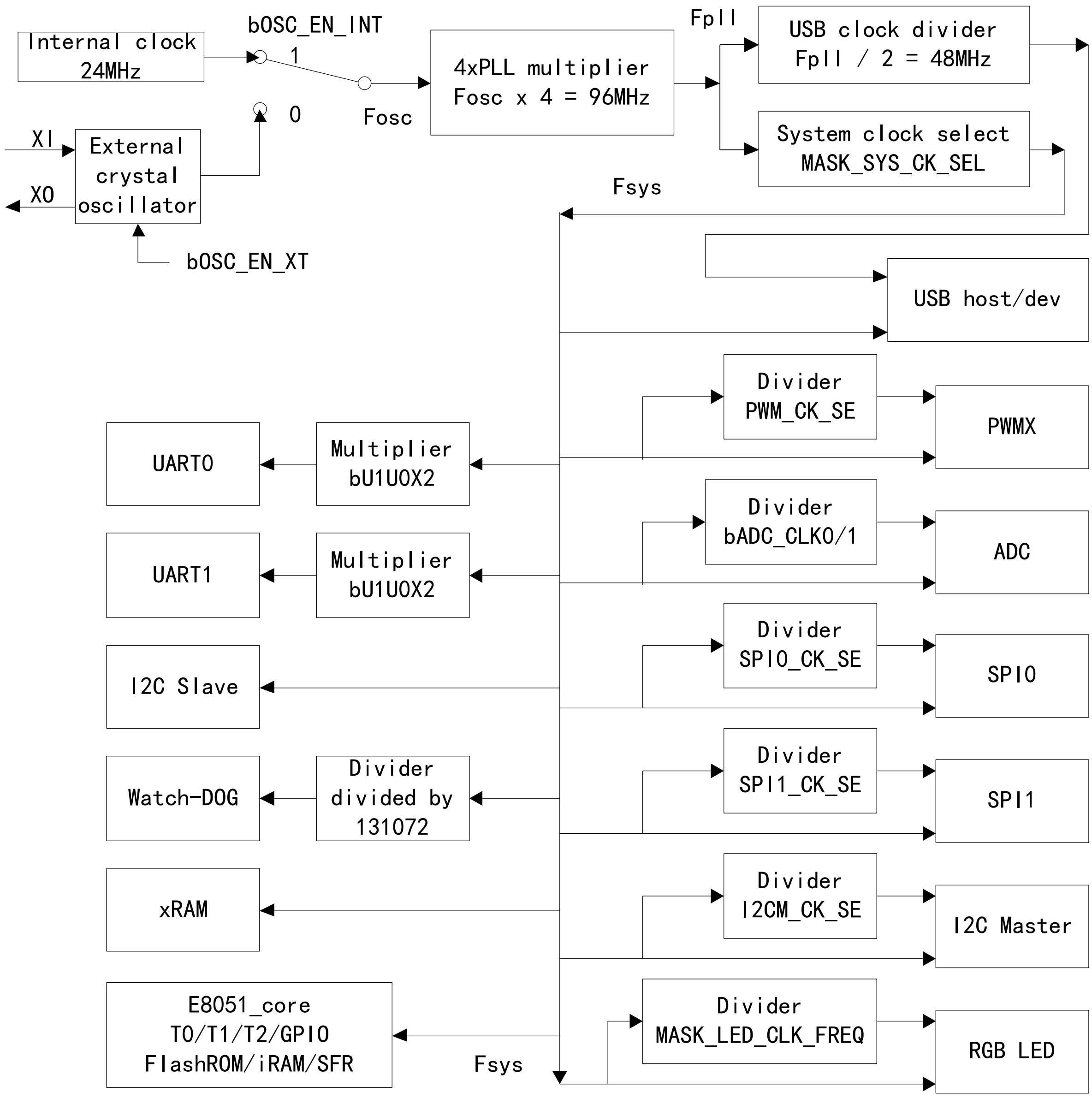


Figure 8.1.1 Clock system and structure diagram

After the internal clock or external clock is alternatively selected as the original clock (Fosc), Fpll high frequency clock is generated after PLL multiplier, and finally the system clock (Fsys) and USB module clock (Fusb4x) are respectively obtained via the 2 groups of frequency dividers. The system clock (Fsys) is directly provided for each module of CH557.

8.2 Register description

Table 8.2.1 Clock control register

Name	Address	Description	Reset value
CLOCK_CFG	B9h	System clock configuration register	83h

System clock configuration register (CLOCK_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bOSC_EN_INT	RW	Internal clock oscillator enable 1: Internal clock oscillator enabled, and the internal clock selected. 0: Internal clock oscillator disabled, and the external crystal oscillator selected to provide the clock.	1
6	bOSC_EN_XT	RW	External crystal oscillator enable 1: The P7.0/P7.1 pin used as XI/XO, and the oscillator enabled. A quartz crystal or a ceramic oscillator needs to be externally connected between the XI and XO. 0: External oscillator disabled.	0
5	bWDOG_IF_TO	RO	Watchdog timer interrupt flag bit 1: Interrupt triggered by the timer overflow signal. 0: No interrupt. This bit is automatically cleared when the watchdog count register (WDOG_COUNT) is reloaded or after it enters the corresponding interrupt service program.	0
[4:3]	Reserved	RO	Reserved	00b
[2:0]	MASK_SYS_CK_SEL	RW	System clock selection. Refer to the Table 8.2.2.	011b

Table 8.2.2 System clock frequency selection

MASK_SYS_CK_SEL	System clock frequency (Fsys)	Relation with crystal frequency (Fxt)	Fsys when Fosc=24MHz
000b	Fpll / 512	Fxt / 128	187.5KHz
001b	Fpll / 128	Fxt / 32	750KHz
010b	Fpll / 32	Fxt / 8	3MHz
011b	Fpll / 8	Fxt / 2	12MHz
100b	Fpll / 6	Fxt / 1.5	16MHz
101b	Fpll / 4	Fxt / 1	24MHz
110b	Fpll / 3	Fxt / 0.75	32MHz
111b	Fpll / 2	Fxt / 0.5	Reserved (48MHz only for test)

8.3 Clock configuration

The internal clock is used by default after the CH557 is powered on, and the internal clock frequency is 24MHz. Select either an internal clock or an external crystal oscillator clock through CLOCK_CFG. If the external crystal oscillator is disabled, the XI and XO pins can be used as P7.0 and P7.1 general-purpose I/O ports respectively. If an external crystal oscillator is selected to provide the clock, the crystal should be cross connected between the XI and XO pins, and the oscillating capacitors should be connected to GND with the XI and XO pins respectively. If the clock signal is input directly from the outside, it should be input from the XI pin with the XO pin suspended.

Original clock frequency: Fosc = bOSC_EN_INT ? 24MHz: Fxt
PLL frequency: Fpll = Fosc * 4
USB clock frequency: Fusb4x = Fpll / 2
The system clock frequency (Fsys) is obtained by Fpll division as shown in Table 8.2.2.
In default state after reset, Fosc=24MHz, Fpll=96MHz, Fusb4x=48MHz, and Fsys=12MHz.

Steps for switching to the external crystal oscillator to provide the clock are as follows:
(1). Make P7.0(XI) pin output low level (used for oscillation capacitor discharge, ensure P7.1 will not cause reset by low level)
P7 = P7 & 0xF0 | 0x06 ; // Before the external crystal oscillator is enabled, P7.0 is at low level and P7.1 is pulled up
(2). Enter the safe mode: first SAFE_MOD = 55h; then SAFE_MOD = AAh.
(3). Set bOSC_EN_XT in CLOCK_CFG to 1 with "OR" operation, other bits remain unchanged, to enable crystal oscillator.
(4). Delay several milliseconds, usually 1mS ~ 10mS, to wait for the crystal oscillator to work steadily.
(5). Re-enter the safe mode: first SAFE_MOD = 55h; then SAFE_MOD = AAh.
(6). Reset bOSC_EN_INT in CLOCK_CFG to 0 with "AND" operation, other bits remain unchanged, and switch to external clock.
(7). Terminate the safe mode, write any value into SAFE_MOD to prematurely terminate the safe mode.

Steps for modifying the system dominant frequency are as follows:
(1). Enter the safe mode: first SAFE_MOD = 55h; then SAFE_MOD = AAh.
(2). Write new value to CLOCK_CFG.
(3). Terminatethe safe mode: write any value into SAFE_MOD to prematurely terminate the safe mode.

Notes:
(1). If the USB module is used, the Fusb4x must be 48MHz. In addition, when the full-speed USB is used, Fsys is not less than 6 MHz. When the low-speed USB is used, Fsys is not less than 1.5 MHz.
(2). For USB host applications or more demanding USB device applications, it is recommended to switch to the external crystal oscillator to provide the clock.
(3). A lower system clock frequency Fsys is preferred to be used to reduce the system dynamic power consumption and widen the operating temperature range.

9. Interrupt

CH557 supports 15 sets of interrupt signal sources, including 6 sets of interrupts (INT0, T0, INT1, T1, UART0 and T2) compatible with the standard MCS51, and 9 sets of extended interrupts (SPI0, USB, ADC, UART1, PWMX/LED/I2C, GPIO and WDOG). The GPIO interrupt can be selected from several I/O pins. I2C includes I2CM and I2CS.

Interrupt service programs are advised to be as compact as possible, to avoid calling functions and subroutines as well as reading and writing xdata variables and code constants.

9.1 Register description

Table 9.1.1 Interrupt Vector Table

Interrupt sources	Entry address	Interrupt No.	Description	Default priority sequence
INT_NO_INT0	0x0003	0	External interrupt 0	High priority ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ Low priority
INT_NO_TMR0	0x000B	1	Timer 0 interrupt	
INT_NO_INT1	0x0013	2	External interrupt 1	
INT_NO_TMR1	0x001B	3	Timer 1 interrupt	
INT_NO_UART0	0x0023	4	UART0 interrupt	
INT_NO_TMR2	0x002B	5	Timer 2 interrupt	
INT_NO_SPI0	0x0033	6	SPI0 interrupt	
None	0x003B	7	Reserved	
INT_NO_USB	0x0043	8	USB interrupt	
INT_NO_ADC	0x004B	9	ADC interrupt	
INT_NO_UART1	0x0053	10	UART1 interrupt	
INT_NO_PWM_I2C	0x005B	11	Data is distinguished based on I2CX_INT after interrupt, and it is the "or" of the following 7 interrupts: PWMX interrupt (when bPWM_IE_END=1); RGB LED interrupt (when bLED_IE_INHIB=1); I2CM interrupt (when bI2CM_IE=1); I2CS interrupt (when bI2CS_IE_*=1).	
INT_NO_GPIO	0x0063	12	GPIO Interrupt	
INT_NO_WDOG	0x006B	13	Watchdog timer interrupt	

Table 9.1.2 Interrupt registers

Name	Address	Description	Reset value
IP_EX	E9h	Extend interrupt priority control register	00h
IE_EX	E8h	Extend interrupt enable register	00h
GPIO_IE	B2h	GPIO interrupt enable register	00h
IP	B8h	Interrupt priority control register	00h
IE	A8h	Interrupt enable register	00h

Interrupt enable register (IE):

Bit	Name	Access	Description	Reset value
7	EA	RW	Global interrupt enable bit 1: Interrupt enabled when E_DIS is 0; 0: All interrupts requests are masked.	0
6	E_DIS	RW	Global interrupt disable bit 1: All interrupts requests are masked. 0: Interrupt enabled when EA is 1.	0

			This bit is usually used to disable interrupt temporarily during flash-ROM operation	
5	ET2	RW	Timer 2 interrupt enable bit 1: T2 interrupt enabled. 0: Interrupt request is masked.	0
4	ES	RW	UART0 interrupt enable bit 1: UART0 interrupt enabled. 0: Interrupt request is masked.	0
3	ET1	RW	Timer 1 interrupt enable bit 1: T1 interrupt enabled. 0: Interrupt request is masked.	0
2	EX1	RW	External interrupt 1 enable bit 1: INT1 interrupt enabled. 0: Interrupt request is masked.	0
1	ET0	RW	Timer 0 interrupt enable bit 1: T0 interrupt enabled. 0: Interrupt request is masked.	0
0	EX0	RW	External interrupt 0 enable bit 1: INT0 interrupt enabled. 0: Interrupt request is masked.	0

Extend interrupt enable register (IE_EX):

Bit	Name	Access	Description	Reset value
7	IE_WDOG	RW	Watchdog timer interrupt enable bit 1: WDOG interrupt enabled. 0: Interrupt request is masked.	0
6	IE_GPIO	RW	GPIO interrupt enable bit 1: Interrupt in GPIO_IE enabled. 0: All interrupts in GPIO_IE are masked.	0
5	IE_PWM_I2C	RW	PWMX, RGB LED, I2CM and I2CS enable bit 1: Interrupt enabled. 0: Interrupt request is masked.	0
4	IE_UART1	RW	UART1 interrupt enable bit 1: UART1 interrupt enabled. 0: Interrupt request is masked.	0
3	IE_ADC	RW	ADC interrupt enable bit 1: ADC interrupt enabled. 0: Interrupt request is masked.	0
2	IE_USB	RW	USB interrupt enable bit 1: USB interrupt enabled. 0: Interrupt request is masked.	0
1	Reserved	RO	Reserved	0
0	IE_SPI0	RW	SPI0 interrupt enable bit	0

			1: SPI0 interrupt enabled. 0: Interrupt request is masked.	

GPIO interrupt enable register (GPIO_IE), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: 0: Level interrupt mode selected. If the GPIO pin inputs a valid level, bIO_INT_ACT is 1 and always requests interrupt. If GPIO inputs an invalid level, bIO_INT_ACT is 0 and the interrupt request is canceled. 1: Edge interrupt mode selected. When GPIO pin inputs a valid edge, the bIO_INT_ACT interrupt flag is generated and an interrupt is requested. The interrupt flag cannot be cleared by software and can only be cleared automatically when reset or in level interrupt mode or when it enters the corresponding interrupt service program.	0
6	bIE_RXD1_LO	RW	1: UART1 receive pin interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: UART1 receive pin interrupt disabled. Select either RXD1 or RXD1_ based on bUART1_PIN_X=0/1	0
5	bIE_P1_5_LO	RW	1: P1.5 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P1.5 interrupt disabled.	0
4	bIE_P1_4_LO	RW	1: P1.4 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P1.4 interrupt disabled.	0
3	bIE_P0_3_LO	RW	1: P0.3 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P0.3 interrupt disabled.	0
2	bIE_P5_3X5X7	RW	1: P5.3, P5.5 and P5.7 level change interrupt enabled. 0: P5.3, P5.5 and P5.7 level change interrupt disabled.	0
1	bIE_P7_1_LO	RW	When bOSC_EN_XT=0, 1: P7.1 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P7.1 interrupt disabled.	0
1	bIE_CMP_RES_LO	RW	When MASK_CMP_VREF!=000, 1: bCMP_RESULT interrupt enabled (active when below the reference voltage in level mode, and active from above to below the reference voltage in edge mode). 0: bCMP_RESULT interrupt disabled.	0
0	bIE_RXD0_LO	RW	1: UART0 receive pin interrupt enabled (active at low level in level mode, while active at falling edge in edge mode).	0

			0: UART0 receive pin interrupt disabled. Select either RXD0 or RXD0_ pin based on bUART0_PIN_X=0/1	

Other signal sources that can generate GPIO interrupt:

When bP4_IE_LEVEL is 1, the level change on any one of P4.0 to P4.7 pins generates GPIO interrupt.
When bP2L_IE_LEVEL is 1, the level change on any one of P2.0 to P2.3 pins generates GPIO interrupt.
When bP1L_IE_LEVEL is 1, the level change on any one of P1.0 to P1.3 pins generates GPIO interrupt.
When bP0_IE_LEVEL is 1, the level change on any one of P0.0 to P0.7 pins generates GPIO interrupt.

Interrupt priority control register (IP):

Bit	Name	Access	Description	Reset value
7	PH_FLAG	RO	Flag bit for high-priority interrupt in progress	0
6	PL_FLAG	RO	Flag bit for low-priority interrupt in progress	0
5	PT2	RW	Timer 2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer 1 interrupt priority control bit	0
2	PX1	RW	External interrupt 1 interrupt priority control bit	0
1	PT0	RW	Timer 0 interrupt priority control bit	0
0	PX0	RW	External interrupt 0 interrupt priority control bit	0

Extend interrupt priority control register (IP_EX):

Bit	Name	Access	Description	Reset value
7	bIP_LEVEL	RO	Current interrupt nested level flag bit 0: No interrupt, or 2-level nested interrupt. 1: Current 1-level nested interrupt	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWM_I2C	RW	PWMX, RGB LED, I2CM and I2CS interrupt priority control bit	0
4	bIP_UART1	RW	UART1 interrupt priority control bit	0
3	bIP_ADC	RW	ADC interrupt priority control bit	0
2	bIP_USB	RW	USB interrupt priority control bit	0
1	Reserved	RO	Reserved	0
0	bIP_SPI0	RW	SPI0 interrupt priority control bit	0

IP and IP_EX registers are used to set the interrupt priority. If a bit is set to 1, then the corresponding interrupt source is set to high-priority. If a bit is reset, then the corresponding interrupt source is set to low-priority. For the interrupt sources at the same level, the system has a priority sequence by default, as shown in Table 9.1.1. The combination of PH_FLAG and PL_FLAG represents the priority of interrupts.

Table 9.1.3 Current interrupt priority state

PH_FLAG	PL_FLAG	Interrupt priority state at present
0	0	No interrupt at present
0	1	Low-priority interrupt is executed at present

1	0	High-priority interrupt is executed at present
1	1	Unexpected state, unknown error

10. I/O ports

10.1 Introduction to GPIO

CH557 provides up to 58 I/O pins, some of which have alternate functions. The inputs and outputs of P0 to P4 ports can be accessed by bits.

If the pin is not configured with alternate functions, it is a general-purpose I/O pin by default. When used as general-purpose digital I/O ports, all of them have a real "read-modify-write" function that allows SETB, CLR and other bit operation commands to independently change the direction and port level of a pin.

10.2 GPIO register

All registers and bits in this section are represented in a generic format: a lowercase "n" represents the serial number of the ports (n=0, 1, 2, 3, 4)), a lowercase "m" represents the serial number of the ports (n=5, 6), while a lowercase "x" represents the serial number of the bits (x=0, 1, 2, 3, 4, 5, 6, 7).

Table 10.2.1 GPIO registers

Name	Address	Description	Reset value
P0	80h	P0 port input/output register	FFh
P0_DIR_PU	C5h	P0 port direction control and pull-up enable register	FFh
P0_MOD_OC	C4h	P0 port output mode register	FFh
P1	90h	P1 port input/output register	FFh
P1_DIR_PU	93h	P1 port direction control and pull-up enable register	FFh
P1_MOD_OC	92h	P1 port output mode register	FFh
P2	A0h	P2 port input/output register	FFh
P2_DIR_PU	95h	P2 port direction control and pull-up enable register	FFh
P2_MOD_OC	94h	P2 port output mode register	FFh
P3	B0h	P3 port input/utput register	FFh
P3_DIR_PU	97h	P3 port direction control and pull-up enable register	FFh
P3_MOD_OC	96h	P3 port output mode register	FFh
P4	C0h	P4 port input/output register	FFh
P4_DIR_PU	C3h	P4 port direction control and pull-up enable register	FFh
P4_MOD_OC	C2h	P4 port output mode register	FFh
P4_LED_KEY	C1h	P4 port LED current limiting and keyboard mode register	00h
P5_IN	AAh	P5 port input register	PPh
P5_OUT_PU	ABh	P5 port output data and pull-up enable register	00h

P5_DIR	ACh	P5 port direction control register	00h
P6_IN	ADh	P6 port input register	PPh
P6_OUT_PU	AEh	P6 port output data and pull-up enable register	00h
P6_DIR	AFh	P6 port direction control register	00h
P7	F1h	P7 port input and output register	P3h
XBUS_AUX	A2h	External bus auxiliary setting register	00h
PORT_CFG	21EAh	Port interrupt and wakeup configuration and pull-down enable register	00h
PIN_FUNC	21E9h	Pin function selection register	00h
ANA_PIN	21E8h	Analog pin digital input disable register	00h

Pn port input/output register (Pn):

Bit	Name	Access	Description	Reset value
[7:0]	Pn.0～Pn.7	RW	Pn.x pin state input and data output bits, accessed by bits	FFh

Pn port output mode register (Pn_MOD_OC):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_MOD_OC	RW	Pn.x pin output mode setting 0: Push-pull output. 1: Open-drain output.	FFh

Pn port direction control and pull-up enable register (Pn_DIR_PU):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_DIR_PU	RW	Pn.x pin direction control in push-pull output mode: 0: Input. 1: Output. Pn.x pin pull-up resistor enable control in open-drain output mode: 0: Pull-up resistor disabled. 1: Pull-up resistor enabled.	FFh

Pm port input register (Pm_IN):

Bit	Name	Access	Description	Reset value
[7:0]	Pm.0～Pm.7	RW	Pm.x pin state input bit	PPh

Pm port output data and pull-up enable register (Pm_OUT_PU):

Bit	Name	Access	Description	Reset value
[7:0]	Pm_OUT_PU	RW	Pm.x pin output data when Pm_DIR[x]=1: 0: Output low level. 1: Output high level. Pm.x pin pull-up resistor enable control when Pm_DIR[x]=0: 0: Pull-up resistor disabled. 1: Pull-up resistor enabled.	00h

Pm port direction control register (Pm_DIR):

Bit	Name	Access	Description	Reset value
[7:0]	Pm_DIR	RW	Pm.x pin direction control: 0: Input. 1: Output	00h

Relevant configuration of Pn port is implemented by the combination of Pn_MOD_OC[x] and Pn_DIR_PU[x] as follows.

Table 10.2.2 Port configuration register combination

Pn_MOD_OC	Pn_DIR_PU	Working mode description (take P4.x as an example, and only when P4_LED_KEY[x]=0)
0	0	High impedance input mode, pin has no pull-up or pull-down resistor
0	1	Push-pull output mode, has symmetrical drive capability which can output or absorb large current
1	0	Open-drain output, support high impedance input, pin has no pull-up resistor
1	1	Quasi-bidirectional mode (standard 8051), open-drain output, support input, pin has pull-up resistor, when the output is changed from low level to high level, it will automatically drive the high level of 2 clock cycles to accelerate the conversion

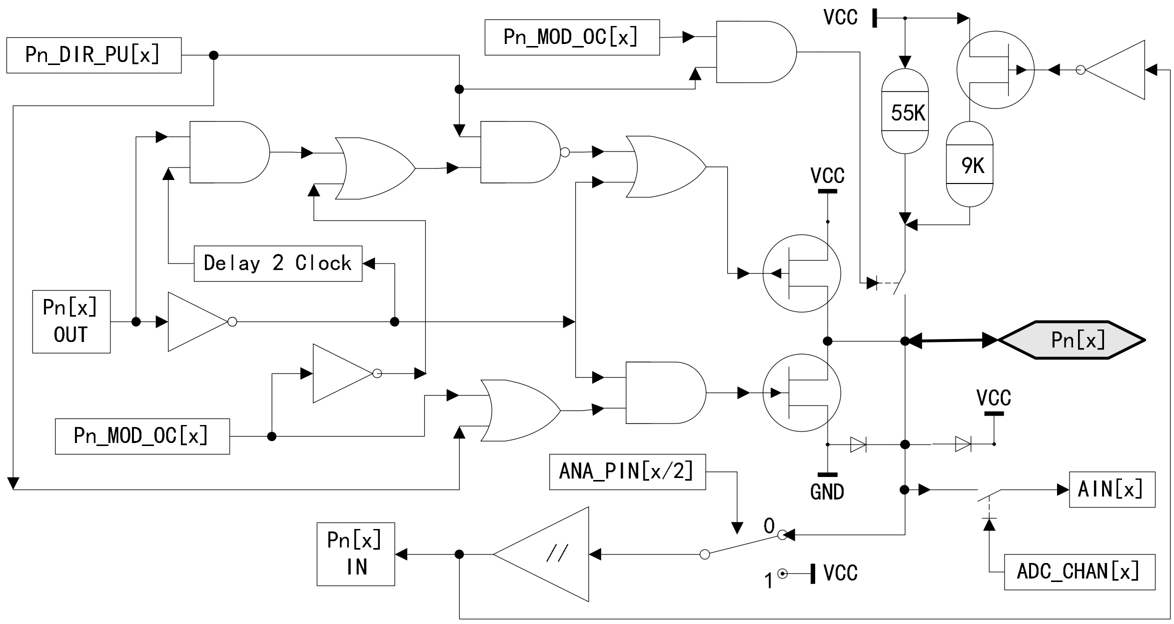
Table 10.2.3 Configuration register combination for P4.x port and when P4_LED_KEY[x]=1

P4_MOD_OC	P4_DIR_PU	Working mode description (when P4_LED_KEY[x]=1)
0	0	High impedance input mode, pin has no pull-up or pull-down resistor
0	1	Push-pull output mode, it can output large current and absorb the limiting current to directly drive the LED
1	0	Open-drain output, support current mode keypad signal input, pin has no pull-up resistor
1	1	Quasi-bidirectional mode (standard 8051), open-drain output, support current mode keypad signal input, pin has pull-up resistor, when the output is changed from low level to high level, it will automatically drive the high level of 2 clock cycles to accelerate the conversion

The P1 to P4 ports support pure input, push-pull output and quasi-bidirectional modes, etc.. Each pin has a freely controlled internal pull-up resistor, and a protective diode connected to VDD and GND.

Figure10.2.1 shows the schematic diagram of P0.x pin of P0 port and P1.x pin of P1 port. If AIN, ADC_PIN and ADC_CHAN are removed, it can be applied to P2, P3 and P4 ports.

Figure 10.2.1 I/O pin schematic diagram



The resistance value in the figure is for reference only. For P0.0 ~ P0.7, P3.3 and P3.4, the 55K resistors in the figure should be 5K, and the 9K resistors in the figure should be 60K.

Table 10.2.4 P5.x configuration register combination

P5_DIR	P5_OUT_PU	bUH?_PD_EN	bUC_DEV_PU_EN	Working mode description
0	0	0	0 @P5.0/P5.1	High impedance input mode, pin has 1000K pull-down resistor
0	0	0	1 @P5.0/P5.1	Input mode, pin has a 1.5K pull-up resistor to V33
0	0	0	None in P5.2～P5.7	High impedance input mode, pin has no pull-up or pull-down resistor
0	0	1	0	Input mode, pin has a 15K pull-down resistor
0	1	0	0	Input mode, pin has a 7.5K pull-up resistor to VDD. If it enters power-down deep-sleep mode when VDD is higher than 4V and USB device is enabled, the USB 1.5K pull-up must be replaced with the 7.5K pull-up during sleep. Enable the 7.5K pull-up firstly and then disable the 1.5K pull-up before sleep. Enable the 1.5K pull-up firstly and then disable the 7.5K pull-up after wakeup.
1	0			Push-pull output mode, output low level, and sink large current
1	1			Push-pull output mode, output high level, and output large current

Table 10.2.5 P6.x configuration register combination

P6_DIR	P6_OUT_PU	Working mode description
0	0	High impedance input mode, pin has a 1000K pull-down resistor
0	1	Input mode, pin has a 7.5K pull-up resistor to VDD
1	0	Push-pull output mode, output low level, and sink large current
1	1	Push-pull output mode, output high level, and output large current

P7 port input/output register (P7):

Bit	Name	Access	Description	Reset value
7	bBUZZ_FREQ1	RW	Output frequency selection of BUZZ pin drive buzzer: 00: BUZZ output disabled. 01: 1 KHz selected. 10: 667 Hz selected. 11: 500 Hz selected.	0
6	bBUZZ_FREQ0	RW		0
5	bP7_1_IN	RO	P7.1 pin data input bit	P
4	bP7_0_IN	RO	P7.0 pin data input bit	P
3	bP7_1_DIR	RW	P7.1 pin direction control: 0: Input. 1: Output.	0
2	bP7_0_DIR	RW	P7.0 pin direction control: 0: Input. 1: Output.	0
1	bP7_1_OUT_PU	RW	P7.1 pin output data when bP7_1_DIR =1: 0: Output low level. 1: Output high level. P7.1 pin pull-up resistor enable control when bP7_1_DIR =0: 0: The pull-up resistor disabled. 1: The pull-up resistor enabled.	1
0	bP7_0_OUT_PU	RW	P7.0 pin output data when bP7_0_DIR =1: 0: Output low level. 1: Output high level. P7.0 pin pull-up resistor enable control when bP7_0_DIR =0: 0: The pull-up resistor disabled. 1: The pull-up resistor enabled.	1

Table 10.2.6 P7.x configuration register combination

bP7_?_DIR	bP7_?_OUT_PU	bOSC_EN_XT	Working mode description
0	0	0	High impedance input mode, pin has no pull-up or pull-down resistor
0	1	0	Input mode, pin has pull-up resistor
1	0	0	Push-pull output mode, output low level, and sink large current
1	1	0	Push-pull output mode, output high level, and output large current
X	X	1	P7.0/P7.1 is used for external crystal oscillator as XI/XO

Port interrupt and wakeup configuration and pull-down enable register (PORT_CFG):

Bit	Name	Access	Description	Reset value
7	bP4_IE_LEVEL	RW	Interrupt enable and wakeup enable of level change on any one of P4.0 to P4.7 pins: 0: Interrupt and wakeup disabled. 1: Interrupt and wakeup enabled.	0
6	bP2L_IE_LEVEL	RW	Interrupt enable and wakeup enable of level change on any one of P2.0 to P2.3 pins: 0: Interrupt and wakeup disabled. 1: Interrupt and wakeup enabled.	0
5	bP1L_IE_LEVEL	RW	Interrupt enable and wakeup enable of level change on any one of P1.0 to P1.3 pins: 0: Interrupt and wakeup disabled. 1: Interrupt and wakeup enabled.	0
4	bP0_IE_LEVEL	RW	Interrupt enable and wakeup enable of level change on any one of P0.0 to P0.7 pins: 0: Interrupt and wakeup disabled. 1: Interrupt and wakeup enabled.	0
3	bP23_PDE	RW	P2.3 pin pull-down resistor enable control: 0: The pull-down resistor disabled. 1: The pull-down resistor enabled.	0
2	bP22_PDE	RW	P2.2 pin pull-down resistor enable control: 0: The pull-down resistor disabled; 1: The pull-down resistor enabled.	0
1	bP21_PDE	RW	P2.1 pin pull-down resistor enable control: 0: The pull-down resistor disabled. 1: The pull-down resistor enabled.	0
0	bP20_PDE	RW	P2.0 pin pull-down resistor enable control: 0: The pull-down resistor disabled. 1: The pull-down resistor enabled.	0

Analog pin digital input disable register (ANA_PIN):

Bit	Name	Access	Description	Reset value
7	bP70_P71_DI_DIS	RW	P7.0 and P7.1 digital input disable: 0: P7.0 and P7.1 digital input enabled. 1: P7.0 and P7.1 digital input disabled to save power consumption.	0
6	bAIN12_13_DI_DIS	RW	AIN12 and AIN13 digital input disable: 0: AIN12 and AIN13 digital input enabled. 1: AIN12 and AIN13 digital input disabled to save power consumption.	0
5	bAIN10_11_DI_DIS	RW	AIN10 and AIN11 digital input disable:	0

			0: AIN10 and AIN11 digital input enabled. 1: AIN10 and AIN11 digital input disabled to save power consumption.	
4	bAIN8_9_DI_DIS	RW	AIN8 and AIN9 digital input disable: 0: AIN8 and AIN9 digital input enabled. 1: AIN8 and AIN9 digital input disabled to save power consumption.	0
3	bAIN6_7_DI_DIS	RW	AIN6 and AIN7 digital input disable: 0: AIN6 and AIN7 digital input enabled. 1: AIN6 and AIN7 digital input disabled to save power consumption.	0
2	bAIN4_5_DI_DIS	RW	AIN4 and AIN5 digital input disable: 0: AIN4 and AIN5 digital input enabled. 1: AIN4 and AIN5 digital input disabled to save power consumption.	0
1	bAIN2_3_DI_DIS	RW	AIN2 and AIN3 digital input disable: 0: AIN2 and AIN3 digital input enabled. 1: AIN2 and AIN3 digital input disabled to save power consumption.	0
0	bAIN0_1_DI_DIS	RW	AIN0 and AIN1 digital input disable: 0: AIN0 and AIN1 digital input enabled. 1: AIN0 and AIN1 digital input disabled to save power consumption.	0

10.3 GPIO alternate functions and map

Some I/O pins of CH557 have alternate functions. After power on, they are all general-purpose I/O pins by default. After different functional modules are enabled, the corresponding pins are configured as corresponding functional pins of each functional module.

Pin function selection register (PIN_FUNC):

Bit	Name	Access	Description	Reset value
7	bPWM1_PIN_X	RW	PWM1 pin mapping enable bit 0: P2.4. 1: P7.0.	0
6	bPWM0_PIN_X	RW	PWM0 pin mapping enable bit 0: P2.5. 1: P1.5.	0
5	bUART1_PIN_X	RW	UART1 pin mapping enable bit 0: RXD1/TXD1 mapped on P2.6/P2.7. 1: RXD1/TXD1 mapped on P1.6/P1.7.	0
4	bUART0_PIN_X	RW	UART0 pin mapping enable bit 0: RXD0/TXD0 mapped on P3.0/P3.1. 1: RXD0/TXD0 mapped on P0.2/P0.3.	0
3	bIO_INT_ACT	R0	GPIO interrupt request activate status: When bIE_IO_EDGE=0, 1: GPIO inputs valid level and requests the interrupt.	0

			0: The input level is invalid. When bIE_IO_EDGE=1, this bit is used as the edge interrupt flag, 1: A valid edge is detected. This bit cannot be cleared by software and can only be cleared automatically when reset or in level interrupt mode or when it enters the corresponding interrupt service program.	
2	bINT0_PIN_X	RW	INT0 pin mapping enable bit 0: P3.2. 1: P1.2.	0
1	bT2EX_PIN_X	RW	T2EX/CAP2 pin mapping enable bit 0: P1.1. 1: P2.5.	0
0	bT2_PIN_X	RW	T2/CAP1 pin mapping enable bit 0: P1.0. 1: P2.4.	0

Table 10.3.1 Alternate functions of GPIO pins

GPIO	Other functions: priority sequence from left to right
P0[0]	SCL0/bSCL0, AIN8, P0.0
P0[1]	SDA0/bSDA0, AIN9, P0.1
P0[2]	RXD_/bRXD_, AIN10, P0.2
P0[3]	TXD_/bTXD_, AIN11, P0.3
P0[4]	AIN12, P0.4
P0[5]	AIN13, P0.5
P0[6]	P0.6
P0[7]	P0.7
P1[0]	T2/bT2, CAP1/bCAP1, AIN0, P1.0
P1[1]	T2EX/bT2EX, CAP2/bCAP2, AIN1, P1.1
P1[2]	INT0_/bINT0, AIN2, P1.2
P1[3]	AIN3, P1.3
P1[4]	SCS/bSCS, AIN4, P1.4
P1[5]	MOSI/bMOSI, PWM0_/bPWM0_, AIN5, P1.5
P1[6]	MISO/bMISO, RXD1_/bRXD1_, AIN6, P1.6
P1[7]	SCK/bSCK, TXD1_/bTXD1_, AIN7, P1.7
P2[0]	PWM5/bPWM5, P2.0
P2[1]	PWM4/bPWM4, P2.1
P2[2]	PWM3/bPWM3, P2.2
P2[3]	PWM2/bPWM2, P2.3
P2[4]	PWM1/bPWM1, T2_/bT2_, CAP1_/bCAP1_, P2.4
P2[5]	PWM0/bPWM0, T2EX_/bT2EX_, CAP2_/bCAP2_, P2.5
P2[6]	RXD1/bRXD1, P2.6
P2[7]	TXD1/bTXD1, P2.7
P3[0]	RXD/bRXD, P3.0
P3[1]	TXD/bTXD, P3.1
P3[2]	INT0/bINT0, P3.2
P3[3]	MSCL/bMSCL, INT1/bINT1, P3.3

P3[4]	MSDA/bMSDA, T0/bT0, P3.4
P3[5]	MOSI1/bMOSI1, T1/bT1, P3.5
P3[6]	MISO1/bMISO1, P3.6
P3[7]	SCK1/bSCK1, P3.7
P4[0]～P4[7]	P4.0～P4.7
P5[0]	bDM/bHM0, P5.0
P5[1]	bDP/bHP0, P5.1
P5[2]	bHM1, bALE_, P5.2
P5[3]	bHP1, P5.3
P5[4]	bHM2, P5.4
P5[5]	bHP2, P5.5
P5[6]	bHM3, P5.6
P5[7]	bHP3, P5.7
P6[0]	P6.0
P6[1]	P6.1
P6[2]	P6.2
P6[3]	P6.3
P6[4]	bDCO_, P6.4
P6[5]	P6.5
P6[6]	P6.6
P6[7]	P6.7
P7[0]	XI, bPWM1_, P7.0
P7[1]	XO, bRST, bALE, P7.1
DCO	

The priority sequence from left to right mentioned in the above table refers to the priority when multiple functional modules compete to use the GPIO.

11. External Bus (xBUS)

CH557 does not provide bus signals for the outside, and it does not support the external bus, but can normally access the on-chip xRAM.

External bus auxiliary setting register (XBUS_AUX):

Bit	Name	Access	Description	Reset value
7	bUART0_TX	R0	UART0 transmit status If this bit is 1, the transmission is in progress.	0
6	bUART0_RX	R0	UART0 receive status If this bit is 1, the reception is in progress.	0
5	bSAFE_MOD_ACT	R0	Safe mode activate status If this bit is 1, it is in safe mode currently.	0
4	bALE_CLK_EN	RW	ALE pin clock output enable 1: P5.2 (when P5_DIR[2]=1) or P7.1 (when	0

			P5_DIR[2]=0 and bP7_1_DIR=1 and bOSC_EN_XT=0) enabled to select the divided clock of system clock frequency. 0: Output clock signal disabled.	
3	bALE_CLK_SEL	RW	ALE pin clock selection when bALE_CLK_EN=1 0: Divided by 12. 1: Divided by 4.	0
3	GF2	RW	General flag bit 2 when bALE_CLK_EN=0: User-defined. Cleared and set by software	0
2	bDPTR_AUTO_INC	RW	Enable the DPTR to add 1 automatically at the end of MOVX_@DPTR command	0
1	Reserved	RO	Reserved	0
0	DPS	RW	Dual DPTR data pointer selection bit: 0: DPTR0 selected. 1: DPTR1 selected.	0

Table 11.1 P5.2/P7.1 alternate ALE output state

bALE_CLK_EN	bALE_CLK_SEL	P5_OUT_PU[2]@P5.2 bP7_1_OUT_PU@P7.1	P5.2 or P7.1 selected pin function description
0	X	X	Default status, ALE disabled
1	0	0	Output Fsys/12
1	1	0	Output Fsys/4
X	X	1	Output high level

12. Timer

12.1 Timer0/1

Timer0 and Timer1 are 2 16-bit timers/counters which are configured by TCON and TMOD. TCON is used for timer/counter T0 and T1 startup control and overflow interrupt as well as external interrupt control. Each timer is a 16-bit timing unit composed of 2 8-bit registers. The high byte counter of timer 0 is TH0 and the low byte counter of timer 0 is TL0. The high byte counter of timer 1 is TH1 and the low byte counter of timer 1 is TL1. Timer 1 can also be used as the baud rate generator of UART0.

Table 12.1.1 Timer0/1 registers

Name	Address	Description	Reset value
TH1	8Dh	Timer 1 count high byte	xxh
TH0	8Ch	Timer 0 count high byte	xxh
TL1	8Bh	Timer 1 count low byte	xxh
TL0	8Ah	Timer 0 count low byte	xxh
TMOD	89h	Timer0/1 mode register	00h
TCON	88h	Timer0/1 control register	00h

Timer/counter 0/1 control register (TCON):

Bit	Name	Access	Description	Reset value
7	TF1	RW	Timer1 overflow interrupt flag bit Automatically cleared after it enters Timer1 interrupt.	0
6	TR1	RW	Timer1 startup/stop bit Set to 1 to startup. Set and cleared by software.	0
5	TF0	RW	Timer0 overflow interrupt flag bit Automatically cleared after it enters Timer0 interrupt.	0
4	TR0	RW	Timer0 startup/stop bit Set to 1 to startup. Set and cleared by software.	0
3	IE1	RW	INT1 interrupt request flag bit Automatically cleared after entering INT1 interrupt.	0
2	IT1	RW	INT1 trigger mode control bit 0: INT1 triggered by low level; 1: INT1 triggered by falling edge.	0
1	IE0	RW	INT0 interrupt request flag bit Automatically cleared after it enters INT0 interrupt.	0
0	IT0	RW	INT0 trigger mode control bit 0: INT0 triggered by low level; 1: INT0 triggered by falling edge.	0

Timer/counter 0/1 mode register (TMOD):

Bit	Name	Access	Description	Reset value
7	bT1_GATE	RW	Gate control enable bit. This bit controls whether the Timer1 startup is affected by INT1. 0: Whether the timer/counter 1 is started is independent of INT1. 1: It is started only when the INT1 pin is at high level and TR1 is 1.	0
6	bT1_CT	RW	Timing/counting mode selection bit 0: It works in timing mode. 1: It works in counting mode. Falling edge on T1 pin selected as the clock.	0
5	bT1_M1	RW	Timer/counter 1 mode selection high bit	0
4	bT1_M0	RW	Timer/counter 1 mode selection low bit	0
3	bT0_GATE	RW	Gate control enable bit. This bit controls whether the Timer0 startup is affected by INT0. 0: Whether the timer/counter 0 is started is independent of INT0. 1: It is started only when the INT0 pin is at high level and TR0 is 1	0
2	bT0_CT	RW	Timing/counting mode selection bit 0: It works in timing mode. 1: It works in counting mode. Falling edge on T0 pin selectd as the clock	0
1	bT0_M1	RW	Timer/counter 0 mode selection high bit	0
0	bT0_M0	RW	Timer/counter 0 mode selection low bit	0

Table 12.1.2 Timern working mode selected by bTn_M1 and bTn_M0 (n=0, 1)

bTn_M1	bTn_M0	Timern working mode (n=0, 1)
0	0	Mode 0: 13-bit timer/counter n, the counting unit is composed of the lower 5 bits of TLn and THn, and the higher 3 bits of TLn is invalid. When the counts of all 13 bits change from 1 to 0, set the overflow flag TFn and reset the initial value
0	1	Mode 1: 16-bit timer/counter n, the counting unit is composed of TLn and THn. When the counts of all 16 bits change from 1 to 0, set the overflow flag TFn and reset the initial value
1	0	Mode 2: 8-bit overload timer/counter n, TLn is used for the counting unit, and THn is used as the overload counting unit. When the counts of all 8 bits change from 1 to 0, set the overflow flag TFn and automatically load the initial value from THn
1	1	Mode 3: For timer/counter 0, it is divided into TL0 and TH0. TL0 is used as an 8-bit timer/counter, which occupies all control bits of Timer0. TH0 is also used as an 8-bit timer, which occupies TR1, TF1 and interrupt resources of Timer1. In this case, Timer1 is still available, but the startup control bit (TR1) and the overflow flag bit (TF1) cannot be used. For timer/counter 1, it stops after it enters mode 3.

Timern count low byte (TLn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	TLn	RW	Timern count low byte	xxh

Timern count high byte (THn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	THn	RW	Timern count high byte	xxh

12.2 Timer2

Timer2 is a 16-bit automatic overload timer/counter configured by T2CON and T2MOD registers, with TH2 as the high byte counter of Timer2 and TL2 as the low byte counter of Timer2. Timer2 can be used as the baud rate generator of UART0, and it also has the function of 2-channel signal level capture. The capture count is stored in RCAP2 and T2CAP1 registers.

Table 12.2.1 Timer2 registers

Name	Add:	Description	Reset value
TH2	CDh	Timer 2 counter high byte	00h
TL2	CCh	Timer 2 counter low byte	00h
T2COUNT	CCh	TL2 and TH2 constitute a 16-bit SFR	0000h
T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	xxh
T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	xxh
T2CAP1	CEh	T2CAP1L and T2CAP1H constitute a 16-bit SFR	xxxxh
RCAP2H	CBh	Counting reload/capature 2 data register high byte	00h
RCAP2L	CAh	Counting reload/capature 2 data register low byte	00h

RCAP2	CAh	RCAP2L and RCAP2H constitute a 16-bit SFR	0000h
T2MOD	C9h	Timer2 mode register	00h
T2CON	C8h	Timer2 control register	00h

Timer/counter 2 control register (T2CON):

Bit	Name	Access	Description	Reset value
7	TF2	RW	Timer2 overflow interrupt flag when bT2_CAP1_EN=0 When the Timer2 counts of all 16 bits change from 1 to 0, this overflow flag is set to 1, which requires software to reset. When RCLK=1 or TCLK=1, the bit is not set to 1.	0
7	CAP1F	RW	Timer2 capture 1 interrupt flag when bT2_CAP1_EN=1 It is triggered by the active edge on T2, which requires software to reset.	0
6	EXF2	RW	Timer2 external trigger flag It is triggered by T2EX active edge and set to 1 when EXEN2=1, which requires software to reset.	0
5	RCLK	RW	UART0 receive clock selection 0: Timer1 overflow pulse selected to generate the baud rate. 1: Timer2 overflow pulse selected to generate the baud rate.	0
4	TCLK	RW	UART0 transmit clock selection 0: Timer1 overflow pulse selected to generate the baud rate. 1: Timer2 overflow pulse selected to generate the baud rate.	0
3	EXEN2	RW	T2EX trigger enable bit 0: Ignore T2EX. 1: Reload or capture enabled to be triggered by T2EX active edge	0
2	TR2	RW	Timer2 startup/stop bit Set to 1 to start. Set and cleared by software.	0
1	C_T2	RW	Timer2 clock source selection bit 0: Internal clock selected. 1: Edge count based on falling edge on T2 pin selected.	0
0	CP_RL2	RW	Timer2 function selection bit. This bit should be forced to be 0 if RCLK or TCLK is 1. 0: Timer2 selected as timer/counter to automatically reload the initial value of the count when the counter overflows or T2EX level changes. 1: Timer2 capture 2 function enabled. The active edge on T2EX is captured.	0

Timer/counter 2 mode register (T2MOD):

Bit	Name	Access	Description	Reset value
7	bTMR_CLK	RW	Fastest clock mode enable of T0/T1/T2 timer which has selected fast clock.	0

			1: Fsys without division as the count clock. 0: Divided clock selected. This bit has no effect on the timer that selects the standard clock.	
6	bT2_CLK	RW	Timer2 internal clock frequency selection bit 0: Standard clock selected. Fsys/12 when in timing/counting mode. Fsys/4 when in UART0 clock mode. 1: Fast clock selected. Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1) when in timing/counting mode. Fsys/2 (bTMR_CLK=0) or Fsys (bTMR_CLK=1) when in UART0 clock mode.	0
5	bT1_CLK	RW	Timer1 internal clock frequency selection bit 0: Standard clock selected, Fsys/12. 1: Fast clock selected. Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1).	0
4	bT0_CLK	RW	Timer0 internal clock frequency selection bit 0: Standard clock selected, Fsys/12. 1: Fast clock selected, Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)	0
3	bT2_CAP_M1	RW	Timer2 capture mode high bit Capture mode selection: X0: From falling ege to falling edge. 01: From any edge to any edge, i.e. level change. 11: From rising edge to rising edge.	0
2	bT2_CAP_M0	RW	Timer2 capture mode low bit	0
1	T2OE	RW	Timer2 clock output enable bit 0: Output disabled. 1: T2 pin enabled to output clock. The frequency is the half of the Timer2 overflow rate.	0
0	bT2_CAP1_EN	RW	Capture 1 mode enable when RCLK=0, TCLK=0, CP_RL2=1, C_T2=0 and T2OE=0 1: Capture 1 function enabled. Active edge on T2 is captured. 0: Capture 1 function disabled.	0

Count reload/capature 2 data register (RCAP2):

Bit	Name	Access	Description	Reset value
[7:0]	RCAP2H	RW	High byte of reload value in timing/counting mode. High byte of timer captured by CAP2 in capture mode.	00h
[7:0]	RCAP2L	RW	Low byte of reload value in timing/counting mode. Low byte of timer captured by CAP2 in capture mode.	00h

Timer2 counter (T2COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	TH2	RW	Current counter high byte	00h
[7:0]	TL2	RW	Current counter low byte	00h

Timer2 capture 1 data (T2CAP0):

Bit	Name	Access	Description	Reset value
[7:0]	T2CAP1H	RO	High byte of timer captured by CAP1	xxh
[7:0]	T2CAP1L	RO	Low byte of timer captured by CAP1	xxh

12.3 PWM register

The PWM_DATA register in this section is represented in a generic format: a lowercase "n" represents the serial number of the ports (n=0 ~ 5).

Table 12.3.1 PWMX registers

Name	Address	Description	Reset value
PWM_CK_SE	9Eh	PWM clock setting register	00h
PWM_CTRL	9Dh	PWM control register	02h
PWM_CTRL2	9Fh	PWM extension control register	00h
PWM_DATA0	9Ch	PWM0 data register	xxh
PWM_DATA1	9Bh	PWM1 data register	xxh
PWM_DATA2	9Ah	PWM2 data register	xxh
PWM_DATA3	A3h	PWM3 data register	xxh
PWM_DATA4	A4h	PWM4 data register	xxh
PWM_DATA5	A5h	PWM5 data register	xxh

PWMn data register (PWM_DATAn):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_DATAn	RW	In 8-bit or 6-bit data width mode, these bits store the current data of PWMn. Duty cycle of PWMn output active level =PWM_DATAn/PWM_CYCLE	xxh

In 12-bit data width mode, PWM_DATA5 provides PWM cycle high byte, and PWM_DATA4 provides PWM cycle low byte. PWM_DATA2 provides PWM0 data high byte, and PWM_DATA0 provides PWM0 data low byte. PWM_DATA3 provides PWM1 data high byte, and PWM_DATA1 provides PWM1 data low byte.

PWM control register (PWM_CTRL):

Bit	Name	Access	Description	Reset value
7	bPWM_IE_END	RO	PWM cycle period end interrupt enable: 0: PWM cycle period end interrupt disabled. 1: PWM cycle period end interrupt enabled.	0
6	bPWM1_POLAR	RW	PWM1 output polarity control 0: Low level by default, while active high. 1: High level by default, while active low.	0
5	bPWM0_POLAR	RW	PWM0 output polarity control 0: Low level by default, while active high. 1: High level by default, while active low.	0
4	bPWM_IF_END	RW	PWM cycle period end interrupt flag bit 1: A PWM cycle period end interrupt. Write 1 to reset, or reset when the PWM_DATA0 data is reloaded.	0
3	bPWM1_OUT_EN	RW	PWM1 output enable 1: PWM1 output enabled.	0
2	bPWM0_OUT_EN	RW	PWM0 output enable 1: PWM0 output enabled.	0
1	bPWM_CLR_ALL	RW	1: Empty PWM count and FIFO. It requires software to reset.	1
0	bPWM_MOD_6BIT	RW	PWM data width 6-bit mode: 0: 8-bit (or 12-bit) data selected, and PWM cycle is 256. 1: 6-bit data selected, and PWM cycle is 64.	0

PWM extension control register (PWM_CTRL2):

Bit	Name	Access	Description	Reset value
7	bPWM_MOD_12BIT	RW	PWM data width 12-bit mode: 0: 8-bit (or 6-bit) data mode selected. PWM cycle is 256. 1: 12-bit data mode selected. Only PWM0 and PWM1 are available. The PWM cycle high byte is specified by PWM_DATA5 and low byte is specified by PWM_DATA4.	0
6	bPWM_STAG_STAT	RO	PWM interleaved output state 0: PWM1/PWM3 is in blanking state. 1: PWM0/PWM2 is in blanking state.	0
5	bPWM2_3_STAG_EN	RW	PWM2/PWM3 interleaved output enable: 0: PWM2 and PWM3 output independently; 1: PWM2/PWM3 interleaved output (every other cycle)	0
4	bPWM0_1_STAG_EN	RW	PWM0/PWM1 interleaved output enable: 0: PWM0 and PWM1 output independently; 1: PWM0/PWM1 interleaved output (every other cycle)	0
3	bPWM5_OUT_EN	RW	PWM5 output enable	0

			1: PWM5 output enabled.	
2	bPWM4_OUT_EN	RW	PWM4 output enable 1: PWM4 output enabled.	0
1	bPWM3_OUT_EN	RW	PWM3 output enable 1: PWM3 output enabled.	0
0	bPWM2_OUT_EN	RW	PWM2 output enable 1: PWM2 output enabled.	0

PWM clock setting register (PWM_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_CK_SE	RW	Set PWM clock frequency division factor	00h

12.4 PWM function

CH557 provides 6-channel PWM, and the output duty cycle of PWM can be dynamically modified. After integrating low-pass filtering via simple Resistor-Capacitor (RC), various output voltages can be obtained, which is equivalent to the low speed Digital-to-Analog Converter (DAC). Among them, PWM0 and PWM1 can also select the reserve polarity output and default output polarity as low level or high level, PWM0 and PWM1 also supports 12-bit data width mode.

PWM_CYCLE = bPWM_MOD_12BIT ? PWM_DATA5*256+PWM_DATA4 : (bPWM_MOD_6BIT ? 64 : 256)
Duty cycle of PWMn output =PWM_DATAn / PWM_CYCLE

It supports a range of 0% to 99.6% duty cycle in 8-bit data mode and 0% to 100% duty cycle in 6-bit data mode (if PWM_DATAn value is greater than PWM_CYCLE, it is regarded as 100%).

In practical applications, it is recommended to enable the PWM pin output and set the PWM output pin to push-pull output.

12.5 Timer function

12.5.1 Timer0/1

(1). Set T2MOD to select Timer internal clock frequency. If bTn_CLK(n=0/1) is 0, the corresponding clock of Timer0/1 is Fsys/12. If bTn_CLK is 1, select Fsys/4 or Fsys as the clock based on bTMR_CLK=0 or 1.

(2). Set TMOD to configure the working mode of Timer.

Mode 0: 13-bit timer/counter

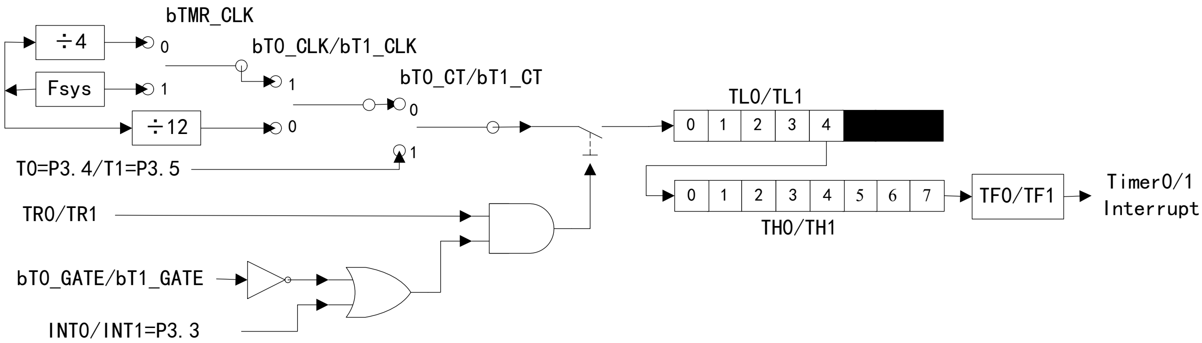


Figure 12.5.1.1 Timer0/1 mode0

Mode 1: 16-bit timer/counter

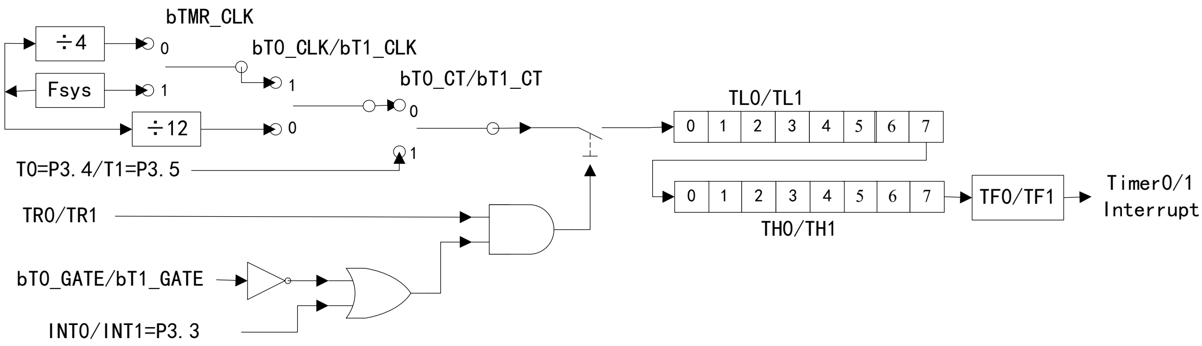


Figure 12.5.1.2 Timer0/1 mode1

Mode 2: Auto reload 8-bit timer/counter

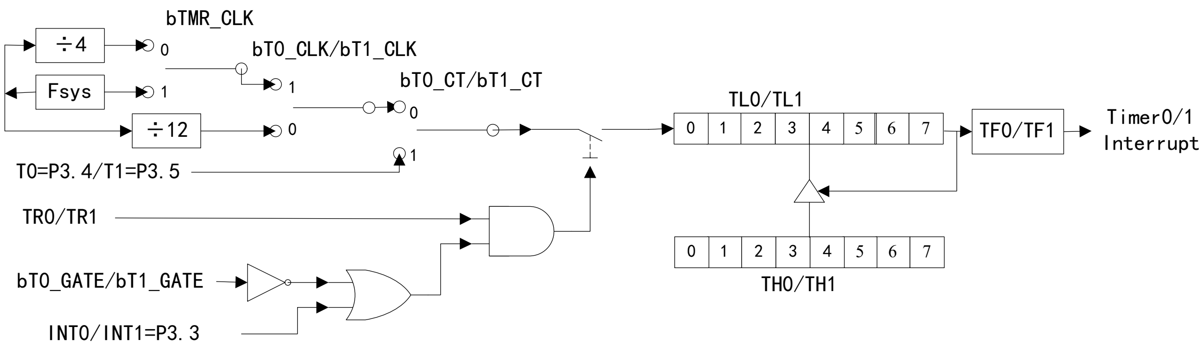


Figure12.5.1.3 Timer0/1 mode2

Mode 3: Timer0 is divided into 2 independent 8-bit timer/counter and borrows the TR1 control bit of Timer1. Timer1 substitutes the borrowed TR1 control bit by whether starting mode 3, and stops running when it enters mode 3.

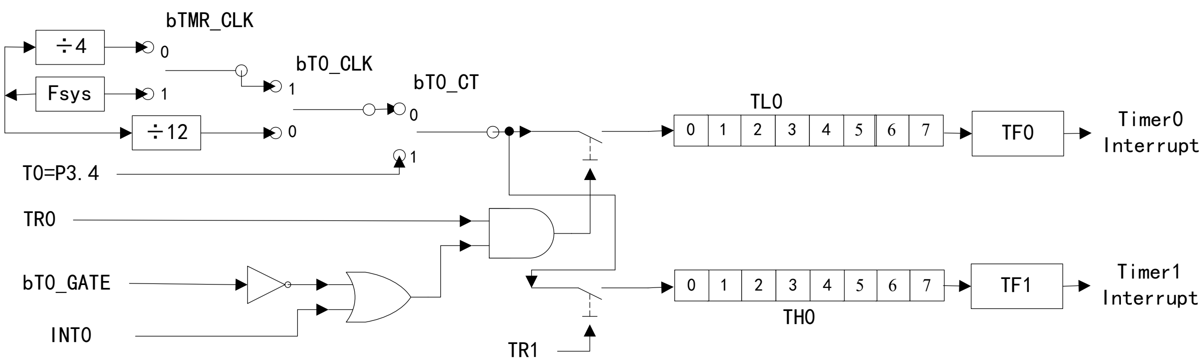


Figure 12.5.1.4 Timer0 mode3

(3). Set initial value TLn and THn(n=0/1) of timer/counter.

(4). Set the TRn bit (n=0/1) in TCON to turn on or stop timer/counter, which can be checked by querying the TFn bit (n=0/1) or by interrupt mode.

12.5.2 Timer2

Timer2 16-bit reload timer/counter mode:

(1). Set the RCLK and TCLK bits in T2CON to 0, to select non-UART baud rate generator mode.
(2). Set the C_T2 bit in T2CON to 0, to select the internal clock, and turn to step (3). Alternatively, set to 1 to select the falling edge on T2 pin as the count clock and skip step (3).
(3). Set T2MOD to select the Timer internal clock frequency. If bT2_CLK is 0, Timer2 clock is Fsys/12. If bT2_CLK is 1, Fsys/4 or Fsys is selected as the clock based on bTMR_CLK=0 or 1.
(4). Set the CP_RL2 bit in T2CON to 0, to select 16-bit reload timer/counter function of Timer2.
(5). Set RCAP2L and RCAP2H as the reload value of timer after overflow. Set TL2 and TH2 as the initial value of the timer (the same as RCAP2L and RCAP2H generally). Set TR2 to 1 to turn on Timer2.
(6). Inquire TF2 or Timer2 interrupt to obtain the current timer/counter state.

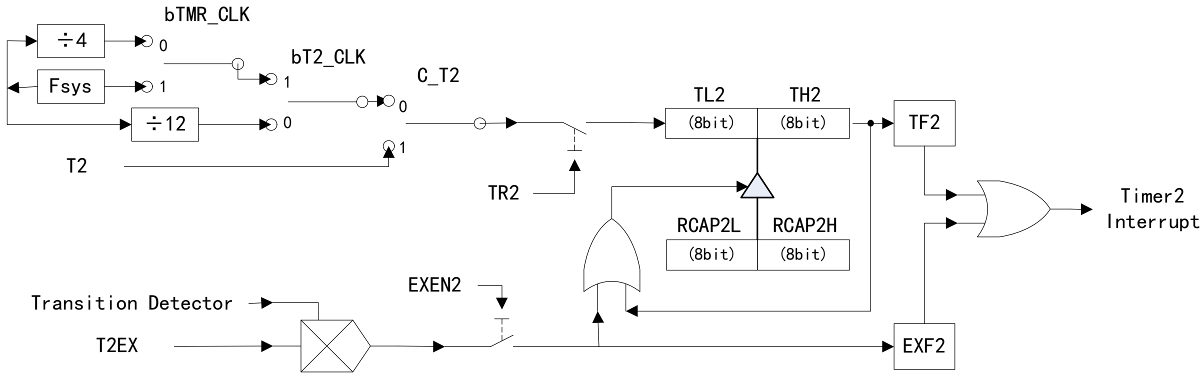


Figure 12.5.2.1 Timer2 16-bit reload timer/counter

Timer2 clock output mode:
Refer to the 16-bit reload timer/counter mode and then set the T2OE bit in T2MOD to 1 to enable the TF2 frequency divided by 2 output from T2 pin.

Timer2 UART0 baud rate generator mode:
(1). Set the C_T2 bit in T2CON to 0, to select the internal clock. Alternatively, set to 1 to select the falling edge on T2 pin as the clock. Set the RCLK and TCLK bits in T2CON to 1, or set one of them to 1 as required, to select UART baud rate generator mode.
(2). Set T2MOD to select Timer internal clock frequency. If bT2_CLK is 0, the clock of Timer2 is Fsys/4. If bT2_CLK is 1, select either Fsys/2 or Fsys as the clock based on bTMR_CLK=0 or 1.
(3). Set RCAP2L and RCAP2H as the reload value of timer after overflow. Set TR2 to 1 to turn on Timer2.

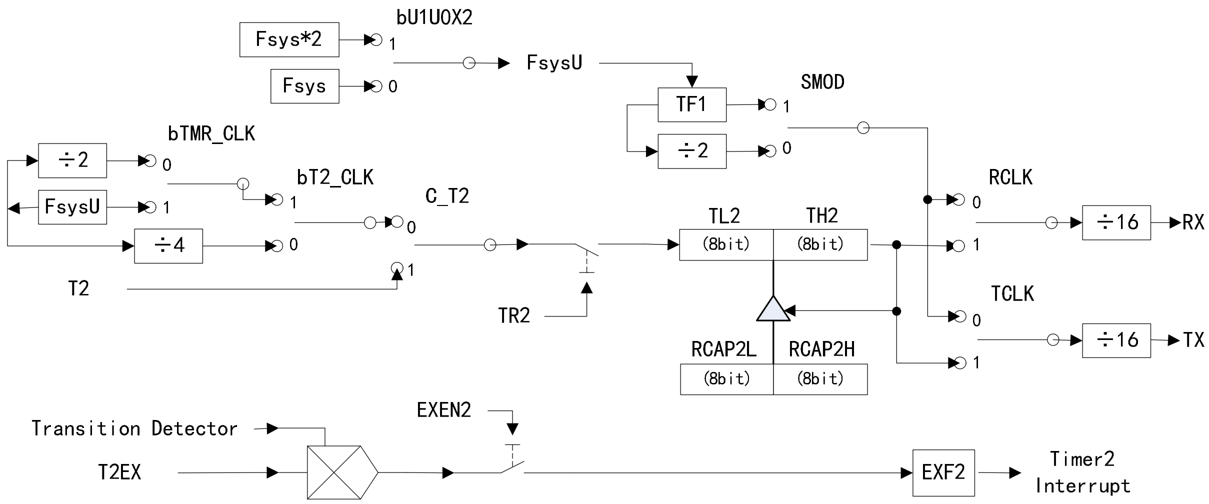


Figure 12.5.2.2 Timer2 UART0 baud rate generator

Timer2 signal channel capture mode:

(1). Set the RCLK and TCLK bits in T2CON to 0, to select non-UART baud rate generator mode.

(2). Set the C_T2 bit in T2CON to 0, to select the internal clock, and turn to step (3). Alternatively, set to 1 to select the falling edge on T2 pin as the count clock and skip step (3).

(3). Set T2MOD to select the Timer internal clock frequency. If bT2_CLK is 0, Timer2 clock is Fsys/12. If bT2_CLK is 1, either Fsys/4 or Fsys is selected as the clock based on bTMR_CLK=0 or 1.

(4). Set the bT2_CAP_M1 and bT2_CAP_M0 bits in T2MOD, to select corresponding edge capture mode.

(5). Set the CP_RL2 bit in T2CON to 1, to select the capture function of Timer2 to T2EX pin.

(6). Set TL2 and TH2 as the initial value of the timer, and set TR2 to 1 to turn on Timer2.

(7). When CAP2 capture is completed, RCAP2L and RCAP2H store the current count values of TL2 and TH2 and set EXF2 to generate an interrupt. The difference between the next captured RCAP2L and RCAP2H and the last captured RCAP2L and RCAP2H is the signal width between the two active edges.

(8). If the C_T2 bit in T2CON is 0, and the bT2_CAP1_EN bit in T2MOD is 1, Timer2 is enabled to capture the T2 pin at the same time. When the CAP1 capture is completed, T2CAP1L and T2CAP1H store the current count values of TL2 and TH2, and set CAP1F to generate an interrupt.

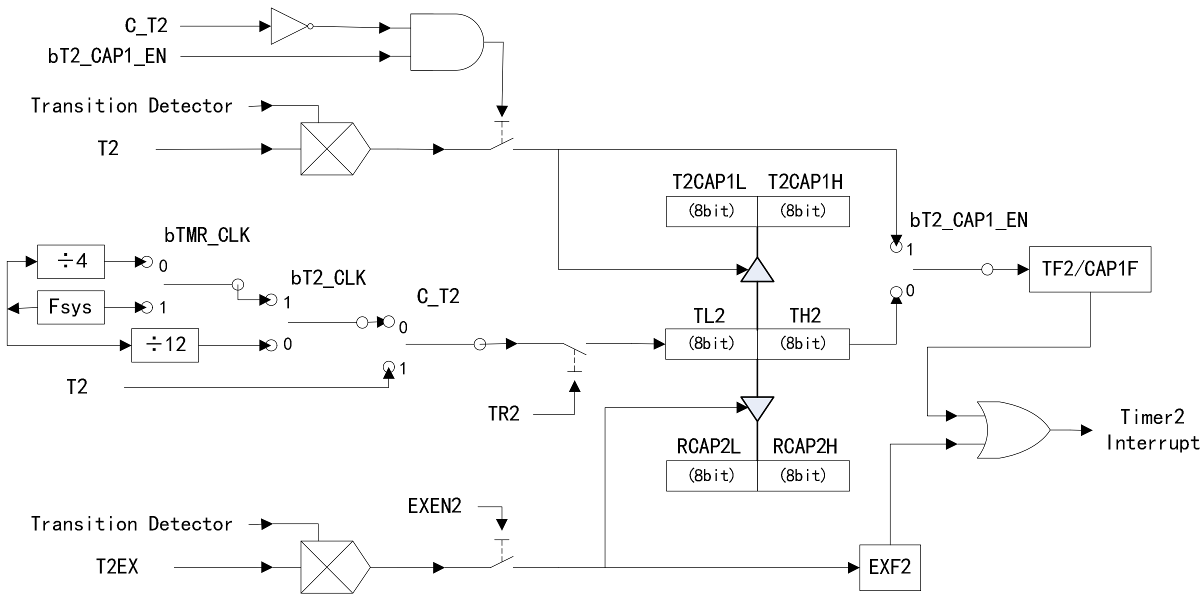


Figure 12.5.2.3 Timer2 Capture Mode

13. Universal asynchronous receiver transmitter (UART)

13.1 UART introduction

CH557 provides 2 full-duplex asynchronous serial ports: UART0 and UART1.

UART0 is a standard MCS51 serial port, whose data reception/transmission is implemented by physically separated receive/transmit registers via SBUF access. The data written to SBUF is loaded into the transmit register. And the receive buffer register is used for read operation on SBUF.

UART1 is a simplified MCS51 serial port, whose data reception/transmission is implemented by physically separated receive/transmit registers via SBUF access. The data written to SBUF1 is loaded into the transmit register. And the receive buffer register is used for read operation on SBUF1. Compared with UART0, UART1 lacks the multi-device communication mode and fixed baud rate, but UART1 has an independent baud rate generator.

13.2 UART register

Table 13.2.1 UART registers

Name	Address	Description	Reset value
SBUF	99h	UART0 data register	xxh
SCON	98h	UART0 control register	00h
SCON1	BCh	UART1 control register	00h
SBUF1	BDh	UART1 data register	xxh
SBAUD1	BEh	UART1 baud rate setting register	xxh
SIF1	BFh	UART1 interrupt status register	00h

13.2.1 UART0 register description

UART0 control register (SCON):

Bit	Name	Access	Description	Reset value
7	SM0	RW	UART0 working mode selection bit 0 0: Select 8-bit data asynchronous communication. 1: Select 9-bit data asynchronous communication.	0
6	SM1	RW	UART0 working mode selection bit 1 0: Fixed baud rate. 1: Variable baud rate, which is generated by timer T1 or T2.	0
5	SM2	RW	UART0 multi-device communication control bit: In mode 2 and mode 3, When SM2=1, If RB8 is 0, RI is not set to 1 and the reception is invalid. If RB8 is 1, RI is set to 1 and the reception is valid. When SM2=0, no matter RB8 is 0 or 1, RI is set when receiving data and the reception is valid. In mode 1, if SM2=1, only when the active stop bit is received can the reception be valid; In mode 0, the SM2 bit must be set to 0.	0
4	REN	RW	UART0 receive enable bit 0: UART0 receive disabled. 1: UART0 receive enabled.	0
3	TB8	RW	The 9^{th} bit of the transmitted data In modes 2 and mode 3, TB8 is used to write the 9^{th} bit of the transmitted data, which can be a parity bit. In multi-device communication, it is used to indicate whether the host sends an address byte or a data byte. Data byte when TB8=0, and address byte when TB8=1.	0
2	RB8	RW	The 9^{th} bit of the received data In mode 2 and 3, RB8 is used to store the 9^{th} bit of the received data.	0

			In mode 1, if SM2=0, RB8 is used to store the received stop bit. In mode 0, RB8 is not used.	
1	TI	RW	Transmit interrupt flag bit Set by hardware at the end of a data byte transmission. It requires software to reset.	0
0	RI	RW	Receive interrupt flag bit Set by hardware at the end of a data byte reception. It requires software to reset.	0

Table 13.2.1.1 UART0 working mode selection

SM0	SM1	Description
0	0	Mode 0, shift register mode. Baud rate is always Fsys/12
0	1	Mode 1, 8-bit asynchronous communication. Variable baud rate, generated by timer T1 or T2
1	0	Mode 2, 9-bit asynchronous communication. Baud rate is Fsys/128(SMOD=0) or Fsys/32(SMOD=1)
1	1	Mode 3, 9-bit asynchronous communication. Variable baud rate, generated by timer T1 or T2.

In mode 1 and mode 3, when RCLK=0 and TCLK=0, UART0 baud rate is generated by timer T1. T1 should be set to mode 2 (auto reload 8-bit timer mode). Both bT1_CT and bT1_GATE must be 0. There are the following cases.

Table 13.2.1.2 Formula of UART0 baud rate generated by T1

bTMR_CLK	bT1_CLK	SMOD	Description (When bU1U0X2=1, the baud rate doubles)
1	1	0	TH1 = 256 - Fsys / 32 / baud rate
1	1	1	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	TH1 = 256 - Fsys / 4 / 16 / baud rate
X	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	TH1 = 256 - Fsys / 12 / 16 / baud rate

In mode 1 and mode 3, when RCLK=1 or TCLK=1, UART0 baud rate is generated by timer T2. T2 should be set as 16-bit automatic reload baud rate generator mode, both C_T2 and CP_RL2 must be 0. There are the following clock types.

Table 13.2.1.3 Formula of UART0 baud rate generated by T2

bTMR_CLK	bT2_CLK	Description (When bU1U0X2=1, the baud rate doubles)
1	1	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate

UART0 data register (SBUF):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF	RW	UART0 data register, including the transmit register and the receive register that are physically separated. The transmit register is used to write data to SBUF. The receive register is used to read data from SBUF.	xxh

13.2.2 UART1 register description

UART1 control register (SCON1):

Bit	Name	Access	Description	Reset value
7	bU1SM0	RW	UART1 working mode selection bit 0: 8-bit data asynchronous communication. 1: 9-bit data asynchronous communication.	0
6	bU1U0X2	RW	UART1/UART0 clock multiplier enable: 0: Multiplier disabled. The clock frequency is Fsys. 1: Multiplier enabled. The clock frequency is 2*Fsys. Communication baud rates of UART1 and UART0 double.	0
5	bU1SMOD	RW	UART1 communication baud rate selection 0: Slow mode. 1: Fast mode.	0
4	bU1REN	RW	UART1 receive enable bit 0: UART1 receive disabled. 1: UART1 receive enabled.	0
3	bU1TB8	RW	The 9^{th} bit of the transmitted data In 9-bit data mode, TB8 is used to write the 9^{th} bit of the transmitted data, which can be a parity bit. In 8-bit data mode, TB8 is ignored	0
2	bU1RB8	RW	The 9^{th} bit of the received data In 9-bit data mode, RB8 is used to store the 9^{th} bit of the received data. In 8-bit data mode, RB8 is used to store the received stop bit	0
1	bU1TIS	WO	Write 1 to preset the transmit interrupt flag bit as 1. For read operation, always return 0.	0
0	bU1RIS	WO	Write 1 to preset the receive interrupt flag bit as 1. For read operation, always return 0.	0

UART1 Baud rate is generated by the SBAUD1 setting, and it can be divided into several cases according to the selection of bU1SMOD:

When bU1SMOD=0, SBAUD1 = 256 - Fsys / 32 / baud rate.

When bU1SMOD=1, SBAUD1 = 256 - Fsys / 16 / baud rate.

When bU1U0X2=1, the above baud rate doubles.

UART1 interrupt status register (SIF1):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU1TI	RW	Transmit interrupt flag bit Set by hardware at the end of a data byte transmission. It requires software to write 1 to reset (writing 0 to this bit is ignored)	0
0	bU1RI	RW	Receive interrupt flag bit Set by hardware at the end of a data byte reception. It requires software to write 1 to reset (writing 0 to this bit is ignored)	0

Note: Writing 1 to the interrupt flag bit to reset can ensure that only the specified flag bit is reset, without affecting other interrupt flags in the same register (other interrupt flags may be 1 before the write operation or may have become 1 during write operation). The same below.

UART1 data register (SBUF1):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF1	RW	UART1 data register, including the transmit register and the receive register that are physically separated. The transmit register is used to write data to SBUF1. The receive register is used to read data from SBUF1.	xxh

13.3 UART applications

UART0 application:

(1). Select UART0 baud rate generator, either from timer T1 or T2, and configure the corresponding counter.

(2). Turn on the timer T1 or T2.

(3). Set SM0, SM1, SM2 of SCON to select the working mode of UART0. Set REN to 1 to enable UART0 receiving.

(4). UART interrupt can be set, or R1 and T1 interrupt state can be inquired.

(5). Read/write to SBUF to implement data reception and transmission of UART, and the allowable baud rate error of UART receive signal is not more than 2%.

UART1 application:

(1). Select bU1SMOD and set SBAUD1 based on the baud rate.

(2). Set bU1SM0 of SCON1 to select the working mode of UART1. Set bU1REN to 1 to enable UART1 receiving.

(3). UART1 interrupt can be set or bU1RI and bU1TI interrupt state can be inquired (only writing 1 to the specified bit can reset it).

(4). Read/write to SBUF1 to implement data reception and transmission of UART1, and the allowable baud rate error of the UART receive signal is not more than 2%.

14. Serial peripheral interface (SPI)

14.1 SPI introduction

CH557 provides 2 SPI interface for high-speed synchronous data transfer with peripherals.

SPI0 features:
(1). Supports master mode and slave mode.
(2). Clock mode: mode 0 and mode 3.
(3). Optional 3-wire full duplex or 2-wire half-duplex mode.
(4). Optional MSB-first or LSB-first.
(5). Clock frequency is adjustable, up to half of the system clock frequency.
(6). Built-in 1-byte receive FIFO and 1-byte transmit FIFO.
(7). Supports the first byte pre-load data in slave mode to facilitate the host to obtain the returned data immediately in the first byte.

SPI1 features:
(1). Only supports master mode, and MSB-first;
(2). Clock mode: mode 0 and mode 3.
(3). Optional 3-wire full duplex or 2-wire half-duplex mode.
(4). Clock frequency is adjustable, up to half of the system clock frequency.

14.2 SPI register

Table 14.2.1 SPI registers

Name	Address	Description	Reset value
SPI0_SETUP	FCh	SPI0 setup register	00h
SPI0_S_PRE	FBh	SPI0 slave mode preset data register	20h
SPI0_CK_SE	FBh	SPI0 clock setting register	20h
SPI0_CTRL	FAh	SPI0 control register	02h
SPI0_DATA	F9h	SPI0 data receive/transmit register	xxh
SPI0_STAT	F8h	SPI0 status register	08h
SPI1_CK_SE	B7h	SPI1 clock setting register	20h
SPI1_CTRL	B6h	SPI1 control register	02h
SPI1_DATA	B5h	SPI1 data receive/transmit register	xxh
SPI1_STAT	B4h	SPI1 status register	08h

14.2.1 SPI0 register description

SPI0 setup register (SPI0_SETUP):

Bit	Name	Access	Description	Reset value
7	bS0_MODE_SLV	RW	SPI0 master/slave mode selection bit 0: Master mode. 1: Slave mode/device mode.	0
6	bS0_IE_FIFO_OV	RW	FIFO overflow interrupt enable bit in slave mode 1: FIFO overflow interrupt enabled. 0: FIFO overflow does not generate interrupt.	0

5	bS0_IE_FIRST	RW	Receive first byte completed interrupt enable bit in slave mode 1: Interrupt triggered when the first data byte is received in slave mode. 0: Interrupt is not generated when the first byte is received.	0
4	bS0_IE_BYTE	RW	Data byte transmit completed interrupt enable bit 1: Data byte transmit completed interrupt enabled. 0: Interrupt is not generated when the byte transmission is completed.	0
3	bS0_BIT_ORDER	RW	Order control bit of data byte 0: MSB first. 1: LSB first.	0
2	Reserved	RO	Reserved	0
1	bS0_SLV_SELT	R0	Chip select activate status bit in slave mode 0: Not selected currently. 1: Being selected currently	0
0	bS0_SLV_PRELOAD	R0	Pre-load data status bit in slave mode 1: Current pre-load state after valid chip select and before the data is not transmitted	0

SPI0 clock setting register (SPI0_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_CK_SE	RW	Set SPI0 clock frequency division factor in master mode	20h

SPI0 preset data register in slave mode (SPI0_S_PRE)

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_S_PRE	RW	Preload first transmission data in slave mode	20h

SPI0 control register (SPI0_CTRL):

Bit	Name	Access	Description	Reset value
7	bS0_MISO_OE	RW	SPI0 MISO output enable 1: SPI0 MISO output enabled. 0: SPI0 MISO output disabled.	0
6	bS0_MOSI_OE	RW	SPI0 MOSI output enable 1 SPI0 MOSI output enabled. 0: SPI0 MOSI output disabled.	0
5	bS0_SCK_OE	RW	SPI0 SCK output enable 1: SPI0 SCK output enabled. 0: SPI0 SCK output disabled.	0
4	bS0_DATA_DIR	RW	SPI0 data direction control bit 0: Output. Only writing to FIFO is regarded as an effective operation, and an SPI transmission is started.	0

			1: Input. Reading/writing to FIFO is regarded as an effective operation, and an SPI transmission is started.	
3	bS0_MST_CLK	RW	SPI0 master clock mode control bit 0: Mode 0. SCK defaults to low level when free. 1: Mode 3. SCK defaults to high level.	0
2	bS0_2_WIRE	RW	2-wire half-duplex mode enable bit of SPI0 0: 3-wire full-duplex mode (SCK, MOSI and MISO). 1: 2-wire half-duplex mode (SCK, MISO).	0
1	bS0_CLR_ALL	RW	1: Empty SPI0 interrupt flag and FIFO. It requires software to reset.	1
0	bS0_AUTO_IF	RW	Enable bit that allows automatic clear of byte receive completed interrupt flag through FIFO effective operation 1: Auto clear the byte receive completed interrupt flag (S0_IF_BYTE) during the effective read and write operation of FIFO	0

SPI0 data receive/transmit register (SPI0_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_DATA	RW	Including the transmit FIFO and the receive FIFO which are physically separated. The receive FIFO is used for read operation. And the transmit FIFO is used for write operation. Effective read/write operation can initiate an SPI transfer.	xxh

SPI0 status register (SPI0_STAT):

Bit	Name	Access	Description	Reset value
7	S0_FST_ACT	R0	1: Currently, reception of the first byte is completed in slave mode.	0
6	S0_IF_OV	RW	FIFO overflow flag bit in slave mode 1: FIFO overflow interrupt. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset. When bS0_DATA_DIR=0, transmit FIFO empty triggers interrupt. When bS0_DATA_DIR=1, receive FIFO full triggers interrupt.	0
5	S0_IF_FIRST	RW	First byte receive completed interrupt flag bit in slave mode 1: The first byte is received. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
4	S0_IF_BYTE	RW	Data byte transmit completed interrupt flag bit 1: One byte transmission is completed. Directly write 0 to reset, or write 1 to the corresponding bit	0

			in the register to reset, or reset by FIFO effective operation when bS0_AUTO_IF=1.	
3	S0_FREE	R0	SPI0 free flag bit 1: No SPI shift at present, usually it is in the free period between the data bytes	1
2	S0_T_FIFO	R0	SPI0 transmit FIFO count. 0 and 1 both are valid.	0
1	Reserved	R0	Reserved	0
0	S0_R_FIFO	R0	SPI0 receive FIFO count. 0 and 1 both are valid.	0

14.2.2 SPI1 register description

SPI1 status register (SPI1_STAT):

Bit	Name	Access	Description	Reset value
[7:5]	Reserved	RO	Reserved	000b
4	bS1_IF_BYTE	RW	Data byte transmit completed interrupt flag bit 1: One byte transmission is completed. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset, or reset by FIFO effective operation when bS1_AUTO_IF=1.	0
3	bS1_FREE	R0	SPI1 free flag bit 1: No SPI shift at present, usually it is in the free period between the data bytes	1
[2:0]	Reserved	RO	Reserved	000b

SPI1 data receive/transmit register (SPI1_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI1_DATA	RW	An SPI data shift register actually. Read operation is used to receive data, and write operation is used to send data,. Effective read/write operation can initiate an SPI transfer.	xxh

SPI1 control register (SPI1_CTRL):

Bit	Name	Access	Description	Reset value
7	bS1_MISO_OE	RW	SPI1 MISO1 output enable 1: SPI1 MISO1 output enabled. 0: SPI1 MISO1 output disabled.	0
6	Reserved	RO	Reserved	0
5	bS1_SCK_OE	RW	SPI1 SCK1 output enable 1: SPI1 SCK1 output enabled. Simultaneously, MOSI1 output enabled when bS1_2_WIRE=0. 0: SPI1 SCK1 output disabled.	0
4	bS1_DATA_DIR	RW	SPI1 data direction control bit 0: Output. Only writing to SPI1_DATA is regarded as an	0

			effective operation, and an SPI transfer is started. 1: Input. Reading/writing to SPI1_DATA is regarded as an effective operation, and an SPI transfer is started.	
3	bS1_MST_CLK	RW	SPI1 clock mode control bit 0: Mode 0. SCK1 defaults to low level when free. 1: Mode 3. SCK1 defaults to high level.	0
2	bS1_2_WIRE	RW	2-wire half-duplex mode enable bit of SPI1 0: 3-wire full-duplex mode (SCK1, MOSI1, MISO1). 1: 2-wire half-duplex mode (SCK1, MISO1).	0
1	bS1_CLR_ALL	RW	1: Empty SPI1 interrupt flag and FIFO. It requires software to reset.	1
0	bS1_AUTO_IF	RW	Enable bit that allows auto clear of byte receive completed interrupt flag through SPI1_DATA effective operation 1: Automatically clear the byte receive completed interrupt flag (bS1_IF_BYTE) during the effective read/write operations of SPI1_DATA	0

SPI1 clock setting register (SPI1_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI1_CK_SE	RW	Set SPI1 clock frequency division factor.	20h

14.3 SPI transfer format

SPI host mode supports two transfer formats, i.e. mode 0 and mode 3, which can be selected by setting the bSn_MST_CLK bit in SPI control register (SPIn_CTRL). CH557 always samples MISO data on the rising edge of CLK. The data transfer formats are shown in the figures below.

Mode 0: bSn_MST_CLK = 0

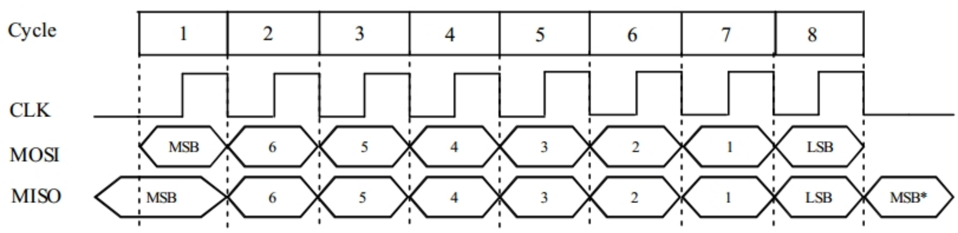


Figure 14.3.1 SPI mode 0 timing diagram

Mode 3: bSn_MST_CLK = 1

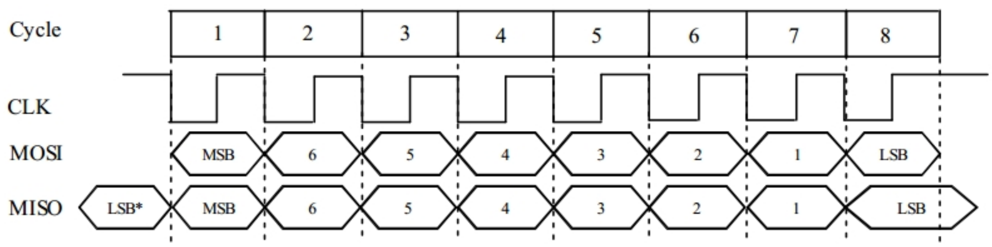


Figure 14.3.2 SPI mode 3 timing diagram

14.4 SPI configuration

14.4.1 Master mode

In SPI master mode, SCK pin output serial clock, and chip select output pin can be specified as any I/O pin.

SPI0 configuration procedure:

(1) Set the SPI clock setting register (SPI0_CK_SE) to configure SPI clock frequency.

(2). Set the bS0_MODE_SLV bit in the SPI setup register (SPI0_SETUP) to 0, to select Master mode.

(3). Set the bS0_MST_CLK bit in the SPI control register (SPI0_CTRL) to select mode 0 or mode 3 as required.

(4). Set the bS0_SCK_OE and bS0_MOSI_OE bits in the SPI control register (SPI0_CTRL) to 1, and set the bS0_MISO_OE bit to 0, to set the P1 port direction bSCK and bMOSI to output, bMISO to input, and chip select pin to output.

Data transmission:

(1). Write to the SPI0_DATA register, write data to FIFO to automatically initiate an SPI transfer..

(2). Wait for S0_FREE to be 1, it indicates that the transmission is completed and the transmission of the next byte can be proceeded.

Data reception:

(1). Write to the SPI0_DATA register, write any data to FIFO, e.g. 0FFh to initiate an SPI transfer.

(2). Wait for S0_FREE to be 1, it indicates that the reception is completed and SPI0_DATA can be read to obtain the received data.

(3). If bS0_DATA_DIR is set to 1 previously, the above read operation still can initiate the next SPI transfer, otherwise it will not start.

14.4.2 Slave mode

Only SPI0 supports Slave mode. In Slave mode, SCK pin is used to receive the serial clock of the connected SPI host.

(1). Set the bS0_MODE_SLV bit in the SPI0 setup register (SPI0_SETUP) to 1, to select Slave mode.

(2). Set the bS0_SCK_OE and bS0_MOSI_OE bits in the SPI0 control register (SPI0_CTRL) to 0, and set the bS0_MISO_OE bit to 1, to set the P1 port direction bSCK, bMOSI, bMISO and chip select pin to input. When SCS is active (low level), MISO output is automatically enabled. In this case, it is recommended to set MISO pin to high impedance input (P1_MOD_OC[6]=0, P1_DIR_PU[6]=0), so that MISO does not output during invalid chip select, which is convenient for sharing SPI bus.

(3). Optionally, set the preset data register in SPI slave mode (SPI0_S_PRE), to be automatically loaded into the buffer for the first time after chip select for external output. After 8 serial clocks, that is, the first byte data transfer and exchange is completed, CH557 obtains the first byte of data (possibly command code) sent by the external SPI host, and the external SPI host obtains the preset data (possibly the status value) in SPI0_S_PRE through exchange. The bit7 in the SPI0_S_PRE register is automatically loaded into the MISO pin during the low level period of SCK after the SPI chip select is active. For SPI mode 0, if the bit7 in SPI0_S_PRE is preset by CH557, the external SPI host obtains the preset value of bit7 in SPI0_S_PRE by inquiring the MISO pins when the SPI chip select is valid but there is no data transfer, thereby the value of bit7 in SPI0_S_PRE can be obtained only by the valid SPI chip select.

Data transmission:
Inquire S0_IF_BYTE or wait for interrupt. After each SPI data byte transfer, write to the SPI0_DATA register, and write the data to be sent to FIFO. Or wait for S0_FREE to be changed from 0 to 1, and the transmission of the next byte can be proceeded.

Data reception:
Inquire S0_IF_BYTE or wait for interrupt. After each SPI data byte transfer, read the SPI0_DATA register to obtain the received data from FIFO. Inquire S0_R_FIFO to know whether there are remaining bytes in FIFO.

15. Analog-to-digital converter (ADC) and Touch Key (TKEY)

15.1 Introduction to ADC and CMP

CH557 provides a 12-bit analog-to-digital converter, including an analog-to-digital converter module (ADC) and a voltage comparator module (CMP).

This ADC 14 has 14 external analog signal input channels and 2 internal input channels (reference voltage), which supports time-sharing acquisition and supports analog input voltage that ranges from 0 to VDD.

There are two input options for the positive phase input of CMP: when bCMP_PIN=1, select to connect to the ADC analog input channel via resistor divided voltage. When bCMP_PIN=0, select to input VDD power supply via resistor divided voltage. The inverted input is selected by MASK_CMP_VREF for the reference voltage. Generally the CMP is mainly used for supply voltage monitor and DC-DC control. Refer to Section 7.2.

15.2 ADC register

Table 15.2.1 ADC registers

Name	Address	Description	Reset value
ADC_CTRL	F3h	ADC control and status register	xxh
ADC_DAT_H	F5h	ADC result data high byte (read only)	0xh
ADC_DAT_L	F4h	ADC result data low byte (read only)	xxh
ADC_DAT	F4h	ADC_DAT_L and ADC_DAT_H constitute a 16-bit SFR	0xxxh
TKEY_CTRL	F5h	Touch key charging pulse width control register (write only)	00h
ADC_CHAN	F6h	ADC analog signal channel selection register	00h

ADC control and status register (ADC_CTRL):

Bit	Name	Access	Description	Reset value
7	bTKEY_ACT	RO	Touch-key detection activity 1: The capacitor is being charged and the ADC is being measured.	0
6	Reserved	RO	Reserved	0
5	bADC_IF	RW	ADC conversion completed interrupt flag 1: An ADC conversion is completed.	0

			Write 1 to reset, or write to ADC_CHAN to reset, or write to TKEY_CTRL to reset.	
4	bADC_START	RW	ADC startup control bit Set to 1 to start an ADC conversion. The bit is reset automatically after the ADC conversion is completed	0
3	bADC_EN	RW	ADC power enable bit 0: ADC power supply OFF. It enters the sleep state. 1: ADC power supply ON.	0
2	Reserved	RO	Reserved	0
1	bADC_CLK1	RW	ADC reference clock frequency selection high bit	0
0	bADC_CLK0	RW	ADC reference clock frequency selection low bit	0

Table 15.2.2 ADC reference clock frequency selection table

bADC_CLK1	bADC_CLK0	ADC reference clock frequency	Time required to complete an ADC	Applicable scope
0	0	750KHz	512 Fosc cycles	Rs<=20KΩ or Cs>=0.08uF
0	1	1.5MHz	256 Fosc cycles	Rs<=10KΩ or Cs>=0.08uF
1	0	3MHz	128 Fosc cycles	VDD>=3V and (Rs<=5KΩ or Cs>=0.08uF)
1	1	6MHz	64 Fosc cycles	VDD>=4.5V and (Rs<=2KΩ or Cs>=0.08uF)

Notes: VDD refers to power voltage. Cs refers to capacitance in parallel to signal source. Rs refers to internal resistance in series with signal source (the sampling time is only 4 reference clocks)

ADC analog signal channel selection register (ADC_CHAN):

Bit	Name	Access	Description	Reset value
[7:4]	Reserved	RO	Reserved	0000b
[3:0]	MASK_ADC_CHAN	RW	When bADC_EN=1, select the signal source of the analog signal channel. When bADC_EN=0, the analog signal channel is closed.	0000b

Table 15.2.1 Voltage comparator (CMP) positive phase input and ADC/TKEY input external signal channel selection table

bADC_EN	ADC_CHAN	Select the signal source of the analog signal channel
0	xxxxb	Disconnect the internal and external signal channel (AIN0 to AIN13), suspended
1	0000b	Connect to external signal: AIN0 (P1.0)
1	0001b	Connect to external signal:AIN1 (P1.1)
1	0010b	Connect to external signal: AIN2 (P1.2)
1	0011b	Connect to external signal: AIN3 (P1.3)
1	0100b	Connect to external signal: AIN4 (P1.4)
1	0101b	Connect to external signal: AIN5 (P1.5)

1	0110b	Connect to external signal: AIN6 (P1.6)
1	0111b	Connect to external signal: AIN7 (P1.7)
1	1000b	Connect to external signal: AIN8 (P0.0)
1	1001b	Connect to external signal: AIN9 (P0.1)
1	1010b	Connect to external signal: AIN10 (P0.2)
1	1011b	Connect to external signal: AIN11 (P0.3)
1	1100b	Connect to external signal: AIN12 (P0.4)
1	1101b	Connect to external signal: AIN13 (P0.5)
1	1110b	Connect to internal reference voltage: V33 voltage
1	1111b	Connect to internal reference voltage: 1.8V voltage VREF18 (there may be noise)

ADC data register (ADC_DAT):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_DAT_H	RO	High byte of ADC sampling result data	0xh
[7:0]	ADC_DAT_L	RO	Low byte of ADC sampling result data	xxh

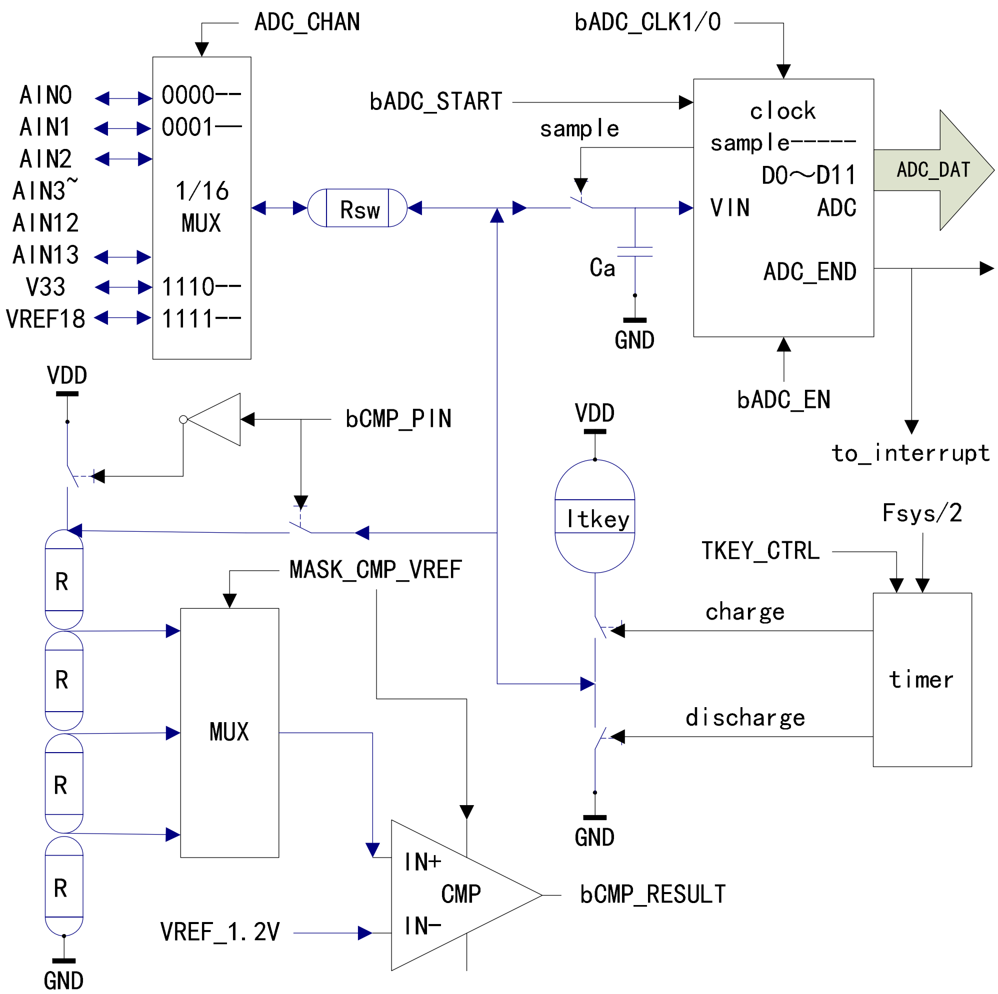


Figure 15.2.1 ADC/TKEY structure diagram (Blue lines represent analog signals)

15.3 TKEY register

Table 15.3.1 TKEY register

Name	Address	Description	Reset value
TKEY_CTRL	F5h	Touch key charging pulse width control register (write only)	00h

Touch key charging pulse width control register (TKEY_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	TKEY_CTRL	WO	Touch key charging pulse width value Only the lower 7 bits are valid. Count in the unit of (2/Fsys). It automatically initates ADC to measure the voltage on the capacitor when the timing is up.	00h

15.4 ADC and Touch-Key functions

ADC sampling mode configuration procedure:

(1). Set the bADC_EN bit in ADC_CTRL to 1, to enable ADC module, and set the bADC_CLK0/1 to select frequency.

(2). Set the ADC_CHAN register to select external signal channel or internal signal channel.

(3). Optional, clear the bADC_IF interrupt flag. Optional, if the interrupt mode is used, the interrupt needs to be enabled here.

(4). Set bADC_START in ADC_CTRL register to start an ADC conversion.

(5). Wait for bADC_START to be changed into 0, or wait for bADC_IF to be set to 1 (if reset before), it indicates that ADC conversion is completed and the result data can be read through ADC_DAT. This data is the value of the input voltage relative to 4095 equal parts of the VDD supply voltage, for example, if the result data is 475, it indicates that the input voltage is approximate to 475/4095 of the VDD voltage. If the VDD supply voltage is also uncertain, another determined reference voltage value can be measured, and the measured input voltage value and the VDD supply voltage value can be calculated proportionally.

(6). If bADC_START is set again, the next ADC conversion can be started.

(7). If the ADC reference clock frequency is high and it results in a short sampling time or high internal resistance of signal source in series, or large Rsw internal resistance due to the low supply voltage, then it is possible that Ca could not sample enough signal voltage and affect the ADC result. The solution is to discard the first ADC data, immediately start the second ADC and use its ADC result data, namely sample twice.

(7). In case of high accuracy requirement, it is recommended to calibrate before use and eliminate the inherent deviation with software.

Touch-Key detection procedure:

(1). Set the bADC_EN bit in ADC_CTRL register to 1, to enable ADC module, and set the bADC_CLK0/1 to select frequency.

(2). Set the ADC_CHAN register to select touch key signal channel.

(3). Select the appropriate charging pulse width according to the actual capacitance of the touch key, and write into the TKEY_CTRL register. The simple calculation formula is as follows (assume that: the external capacitance of the touch key Ckey=25pF, VDD=5V, Fsys=12MHz, rough calculation):

count=(Ckey+Cint)*0.7VDD/ITKEY/(2/Fsys)=(25p+15p)*0.35*5*12M/50u=17

TKEY_CTRL=count > 127 ? 127 : count

(4). Optional, if the interrupt mode is used, the interrupt needs to be enabled here.

(5). When the capacitor charge timing of the touch key is reached, CH557 automatically sets bADC_START to start ADC to measure the voltage on the capacitor

(6). Wait for bTKEY_ACT to be changed into 0, or wait for bADC_IF to be set to 1, it indicates the completion of charging and ADC conversion and the result data can be read through ADC_DAT. The software then compares this value with that without any key, and determines whether the touch key is pressed or not according to the change in capacitance.

(7). Shift to step (2) as required and select another touch key signal channel for detection.

For the above selected external analog signal channel, the GPIO pin where it's located must be set in either high-impedance input mode or open-drain output mode and in output 1 state (equivalent to high-impedance input), Pn_DIR_PU[x]=0, and turn off the pull-up resistor and pull-down resistor.

16. USB controller

16.1 Introduction

CH557 is integrated with a USB host controller, supporting full-speed (12Mbps) and low-speed (1.5Mbps) USB transfer. It is integrated with a default USB device controller, supporting full speed and low speed, and supporting up to 64 bytes of data packet.

The USB host controller manages 4 USB devices (The 0# device connected to port hub0, the 1# device connected to port hub1, the 2# device connected to port hub2, and the 3# device connected to port hub3) through 4 root-hub ports.

Main features of CH557 USB controller:

(1). Supports USB Host functions and USB Device functions;

(2). Supports USB 2.0 full speed (12Mbps) and low speed (1.5Mbps);

(3). Supports USB control transfer, bulk transfer, interrupt transfer, synchronous/simultaneous transfer;

(4). Supports data packet of up to 64 bytes, built-in FIFO, interrupts and DMA;

(5). Built-in root-hub for 4 ports, USB host can manage 4 USB devices simultaneously via the root-hub.

The USB registers of CH557 are divided into 3 categorys, some of which are multiplexed in the host and device modes.

(1). USB global register.

(2). USB device controller register.

(3). USB host controller and root hub register.

16.2 Global register

Table 16.2.1 USB global registers (that marked in grey is controlled by bUC_RESET_SIE reset)

Name	Addres	Description	Reset value
USB_INT_FG	D8h	USB interrupt flag register	0000 0000b
USB_INT_ST	D9h	USB interrupt status register (read only)	0011 xxxxb

USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
USB_RX_LEN	DBh	USB reception length register (read only)	0xxx xxxxb
USB_INT_EN	21E2h	USB interrupt enable register	0000 0000b
USB_CTRL	E2h	USB control register	0000 0110b
USB_DEV_AD	E3h	USB device address register	0000 0000b

USB interrupt flag register (USB_INT_FG):

Bit	Name	Access	Description	Reset value
7	U_IS_NAK	RO	In USB device mode, 1: NAK busy response is received during current USB transfer. 0: Non-NAK response is received.	0
6	U_TOG_OK	RO	Current USB transmit DATA0/1 synchronization flag match state 1: Synchronization and the data is valid. 0: Desynchrony and the data may be invalid	0
5	Reserved	RO	Reserved	0
4	UIF_FIFO_OV	RW	USB FIFO overflow interrupt flag bit 1: FIFO overflow interrupt. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	0
3	UIF_HST_SOF	RW	SOF timing interrupt flag bit in USB host mode 1: SOF timing interrupt, triggered by SOF packet transfer completion. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	0
2	UIF_SUSPEND	RW	USB bus suspend/wakeup event interrupt flag bit 1: There is an interrupt, triggered by USB suspend event or wakeup event. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	0
1	UIF_TRANSFER	RW	USB transfer completed interrupt flag bit 1: There is an interrupt, triggered by a USB transfer completion. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	0
0	UIF_DETECT	RW	USB device connection or disconnection event interrupt flag bit in USB host mode 1: There is an interrupt, triggered by detecting a USB device connection or disconnection.	0

			0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	
0	UIF_BUS_RST	RW	USB bus reset event interrupt flag bit in USB device mode 1: There is an interrupt, triggered by USB bus reset event. 0: No interrupt. Directly write 0 to reset, or reset by writing 1 to the corresponding bit in the register.	0

USB interrupt status register (USB_INT_ST):

Bit	Name	Access	Description	Reset value
7	bUIS_SETUP_ACT	RO	In the USB device mode, when this bit is 1, 8-byte SETUP request packet has been successfully received. SETUP token does not affect bUIS_TOG_OK and bUIS_TOKEN1/0, MASK_UIS_ENDP or USB_RX_LEN.	0
6	bUIS_TOG_OK	RO	Current USB transmit DATA0/1 synchronization flag match state 1: Synchronization. 0: Desynchrony. The same as U_TOG_OK	0
5	bUIS_TOKEN1	RO	The token PID high bit of the current USB transfer service in device mode	1
4	bUIS_TOKEN0	RO	The token PID low bit of the current USB transfer service in device mode	1
[3:0]	MASK_UIS_ENDP	RO	The endpoint serial number of the current USB transfer service in USB device mode 0000: Endpoint 0; ...; 1111: Endpoint 15	xxxxb
[3:0]	MASK_UIS_H_RES	RO	The response PID of the current USB transfer service in USB host mode, 0000: Device has no response or timeout. Other values: Response PID	xxxxb

BUIS_TOKEN1 and bUIS_TOKEN0 constitute MASK_UIS_TOKEN, which is used to identify the token PID of the current USB transfer service in USB device mode. 00: OUT packet. 01: SOF packet. 10: IN packet. 11: Free.

When MASK_UIS_TOKEN is not free and bUIS_SETUP_ACT is 1, it is required to process the former first, clear UIF_TRANSFER after the former is processed to make the former enter free state, and then process the latter, and finally clear UIF_TRANSFER again.

USB miscellaneous status register (USB_MIS_ST):

Bit	Name	Access	Description	Reset value
7	bUMS_SOF_PRES	RO	SOF packet predictive status bit in USB host mode. If	x

			this bit is 1, SOF packet is to be sent, and it is automatically delayed if there are other USB data packets.	
6	bUMS_SOF_ACT	RO	SOF packet transfer status in USB host mode 1: SOF packet is being transmitted. 0: The transmission is completed, or idle.	x
5	bUMS_SIE_FREE	RO	Free status bit of USB protocol processor 0: Busy, and USB transfer is in progress. 1: USB is free.	1
4	bUMS_R_FIFO_RDY	RO	USB receive FIFO data ready status bit 0: Receive FIFO is null. 1: Receive FIFO is not null	0
3	bUMS_BUS_RESET	RO	USB bus reset status bit 0: No USB bus reset at present. 1: USB bus reset is in progress.	1
2	bUMS_SUSPEND	RO	USB suspend status bit 0: There is USB activity at present. 1: There has been no USB activity for some time, request to be suspended.	0
1	bUMS_DM_LEVEL	RO	In USB host mode, record the state of DM pin when the USB device is just connected to the hub0 port 0: Low level. 1: High level. Used to judge full speed or low speed	0
0	bUMS_DEV_ATTACH	RO	USB device connection state bit of hub0 port in USB host mode 1: The hub0 port has been connected to the USB device. 0: The hub0 port is not connected to the USB device.	0

USB reception length register (USB_RX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUSB_RX_LEN	RO	The number of bytes of the data received by the USB endpoint currently	xxh

USB interrupt enable register (USB_INT_EN):

Bit	Name	Access	Description	Reset value
7	bUIE_DEV_SOF	RW	1: Receive SOF packet interrupt in USB device mode enabled. 0: Receive SOF packet interrupt in USB device mode disabled.	0
6	bUIE_DEV_NAK	RW	1: Receive NAK interrupt in USB device mode enabled. 0: Receive NAK interrupt in USB device mode disabled.	0

5	Reserved	RO	Reserved	0
4	bUIE_FIFO_OV	RW	1: FIFO overflow interrupt enabled. 0: FIFO overflow interrupt disabled.	0
3	bUIE_HST_SOF	RW	1: SOF timing interrupt in USB host mode enabled. 0: SOF timing interrupt in USB host mode disabled.	0
2	bUIE_SUSPEND	RW	1: USB bus suspend/wakeup event interrupt enabled. 0: USB bus suspend/wakeup event interrupt disabled.	0
1	bUIE_TRANSFER	RW	1: USB transfer completed interrupt enabled. 0: USB transfer completed interrupt disabled.	0
0	bUIE_DETECT	RW	1: USB device connection/disconnection event interrupt in USB host mode enabled. 0: USB device connection/disconnection event interrupt in USB host mode disabled.	0
0	bUIE_BUS_RST	RW	1: USB bus reset event interrupt in USB device mode enabled. 0: USB bus reset event interrupt in USB device mode disabled.	0

USB control register (USB_CTRL)L

Bit	Name	Access	Description	Reset value
7	bUC_HOST_MODE	RW	USB working mode selection bit 0: USB device mode selected. 1: USB host mode selected.	0
6	bUC_LOW_SPEED	RW	USB bus signal transfer rate selection bit 0: Full speed, 12Mbps. 1: Low speed, 1.5Mbps.	0
5	bUC_DEV_PU_EN	RW	In USB device mode, USB device enable and internal pull-up resistor control bit. If this bit is 1, enable USB device transfer and enable internal 1.5K pull-up resistor	0
4	bUC_DEV_EN	RW	In USB device mode, USB device enable control bit. If the bit is 1, enable USB device transfer, but not enable internal pull-up resistor (external resistor is supported)	0
5	bUC_SYS_CTRL1	RW	USB system control high bit	0
4	bUC_SYS_CTRL0	RW	USB system control low bit	0
3	bUC_INT_BUSY	RW	Auto pause enable bit before the USB transfer completed interrupt flag is not cleared 1: Automatically pause before the UIF_TRANSFER interrupt flag is cleared. It will reply to the busy NAK in device mode. Automatically pause subsequent transfer in host mode . 0: Not pause	0
2	bUC_RESET_SIE	RW	USB protocol processor software reset control bit. If this bit is 1, forced to reset the USB protocol processor	1

			and most of the USB control registers. It requires software to reset.	
1	bUC_CLR_ALL	RW	If the bit is 1, empty USB interrupt flag and FIFO. It requires software to reset.	1
0	Reserved	RO	Reserved	0

bUC_HOST_MODE, bUC_SYS_CTRL1 and bUC_SYS_CTRL0 constitute the USB system control combination:

bUC_HOST_MODE	bUC_SYS_CTRL1	bUC_SYS_CTRL0	USB system control description
0	0	0	Disable USB device function, turn off internal pull-up resistor
0	0	1	Enable USB device function, turn off internal pull-up, and external pull-up needs to be added
0	1	X	Enable USB device function, turn on internal 1.5KΩ pull-up resistor This pull-up resistor has priority over the pull-down resistor, which also can be used in GPIO mode
1	0	0	Select USB host mode, normal working state
1	0	1	Select USB host mode, compulsory DP/DM output SE0 state
1	1	0	Select USB host mode, compulsory DP/DM output J state
1	1	1	Select USB host mode, compulsory DP/DM output K state/wake up

USB device address register (USB_DEV_AD):

Bit	Name	Access	Description	Reset value
7	bUDA_GP_BIT	RW	USB general purpose flag bit User-defined. Reset and set by software.	0
[6:0]	MASK_USB_ADDR	RW	Address of the USB device being operated in host mode. Address of the USB device in device mode.	00h

16.3 USB device register

In USB device mode, CH557 provides 5 sets of bidirectional endpoints (endpoint 0, endpoint 1, endpoint 2, endpoint 3, and endpoint 4). The maximum data packet length of all endpoints is 64 bytes.

Endpoint 0 is the default endpoint and supports control transfer. The transmission and the reception share a 64-byte data buffer.

Endpoint 1, endpoint 2, endpoint 3 each includes a transmission endpoint (IN) and a reception endpoint (OUT). The transmission and the reception each has a separate 64-byte or double 64-byte data buffer respectively, supporting control transfer, bulk transfer, interrupt transfer, and simultaneous/synchronous transfer.

Endpoint 4 includes a transmission endpoint IN and a reception endpoint OUT. The transmission and the reception each has a separate 64-byte data buffer respectively, supporting control transfer, bulk transfer, interrupt transfer, and simultaneous/synchronous transfer.

Each endpoint has a control register (UEPn_CTRL) and a transmission length register (UEPn_T_LEN, n=0/1/2/3/4), which are used to set the synchronization trigger bit of the endpoint, the response to OUT transactions and IN transactions, and the length of data to be sent.

As the necessary USB bus pull-up resistor of USB device, it can be set whether to be enabled by software at any time. When bUC_DEV_PU_EN in the USB control register (USB_CTRL) is set to 1, CH557 will internally connect the pull-up resistor with the DP pin or DM pin of the USB bus based on bUD_LOW_SPEED and enable the USB device function.

When a USB bus reset, or USB bus suspend/wakeup event is detected, or when the USB successfully processes data transmission/reception, the USB protocol processor sets the corresponding interrupt flag and generates an interrupt request. The application program can directly query, or it can query and analyze the interrupt flag register (USB_INT_FG) in the USB interrupt service program, and perform corresponding processing according to UIF_BUS_RST and UIF_SUSPEND. In addition, if UIF_TRANSFER is valid, it is required to continue to analyze the USB interrupt status register (USB_INT_ST), and perform the corresponding processing according to the current endpoint number (MASK_UIS_ENDP) and the current transaction token PID (MASK_UIS_TOKEN). If the synchronization trigger bit (bUEP_R_TOG) of OUT transaction of each endpoint is set in advance, you can judge whether the synchronization trigger bit of the data packet received currently matches the synchronization trigger bit of the endpoint through U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data is valid. If the data is not synchronized, the data should be discarded. Every time the USB transmit/receive interrupt is processed, the synchronization trigger bit of corresponding endpoint should be modified correctly to synchronize the data packet sent next time and detect whether the data packet received next time is synchronized. In addition, bUEP_AUTO_TOG can be set to automatically toggle the corresponding synchronization trigger bit after successful transmission/reception.

The data to be sent by each endpoint is in their own buffer, and the length of the data to be sent is independently set in UEPn_T_LEN. The data received by each endpoint is in their own buffer, but the length of the data received is in the USB reception length register (USB_RX_LEN), and it can be distinguished according to the current endpoint serial number when the USB is receiving an interrupt.

Table 16.3.1 USB device registers (those marked in grey are controlled by RB_UC_RESET_SIE reset)

Name	Address	Description	Reset value
UDEV_CTRL	D1h	USB device physical port control register	0000 0000b
UEP1_CTRL	D2h	Endpoint 1 control register	0000 0000b
UEP1_T_LEN	D3h	Endpoint 1 transmission length register	0000 0000b
UEP2_CTRL	D4h	Endpoint 2 control register	0000 0000b
UEP2_T_LEN	D5h	Endpoint 2 transmission length register	0000 0000b
UEP3_CTRL	D6h	Endpoint 3 control register	0000 0000b
UEP3_T_LEN	D7h	Endpoint 3 transmission length register	0000 0000b
UEP0_CTRL	DCh	Endpoint 0 control register	0000 0000b
UEP0_T_LEN	DDh	Endpoint 0 transmission length register	0000 0000b
UEP4_CTRL	DEh	Endpoint 4 control register	0000 0000b

UEP4_T_LEN	DFh	Endpoint 4 transmission length register	0000 0000b
UEP0_DMA_H	EDh	Endpoint 0 and 4 buffer start address high byte	000x xxxxb
UEP0_DMA_L	ECh	Endpoint 0 and 4 buffer start address low byte	xxxx xxxxb
UEP0_DMA	ECh	UEP0_DMA_L and UEP0_DMA_H constitute a 16-bit SFR	xxxxh
UEP1_DMA_H	EFh	Endpoint 1 buffer start address high byte	000x xxxxb
UEP1_DMA_L	EEh	Endpoint 1 buffer start address low byte	xxxx xxxxb
UEP1_DMA	EEh	UEP1_DMA_L and UEP1_DMA_H consistute a 16-bit SFR	xxxxh
UEP2_DMA_H	E5h	Endpoint 2 buffer start address high byte	000x xxxxb
UEP2_DMA_L	E4h	Endpoint 2 buffer start address low byte	xxxx xxxxb
UEP2_DMA	E4h	UEP2_DMA_L and UEP2_DMA_H consistute a 16-bit SFR	xxxxh
UEP3_DMA_H	E7h	Endpoint 3 buffer start address high byte	000x xxxxb
UEP3_DMA_L	E6h	Endpoint 3 buffer start address low byte	xxxx xxxxb
UEP3_DMA	E6h	UEP3_DMA_L and UEP3_DMA_H consistute a 16-bit SFR	xxxxh
UEP4_1_MOD	21E0h	Endpoint 1, endpoint 4 mode control register	0000 0000b
UEP2_3_MOD	21E1h	Endpoint 2, endpoint 3 mode control register	0000 0000b

USB device physical port control register (UDEV_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
[7:4]	Reserved	RO	Reserved	0000b
3	bUD_PD_EN	RW	USB device port DP/DM pin internal pull-down resistor enable bit 1: The internal pull-down resistor enabled. 0: The internal pull-down resistor disabled. This bit also can be used in GPIO mode to provide a pull-down resistor.	0
2	bUD_LOW_SPEED	RW	USB device physical port low-speed mode enable bit 1: Low speed mode, 1.5Mbps. 0: Full speed mode, 12Mbps.	0
1	bUD_GP_BIT	RW	USB device mode general purpose flag bit User-defined. Reset and set by software.	0
0	bUD_PORT_EN	RW	USB device physical port enable bit 1: Physical port enabled. 0: Physical port disabled.	0

Endpoint n control register (UEPn_CTRL):

Bit	Name	Access	Description	Reset value
7	bUEP_R_TOG	RW	Synchronization trigger bit expected by the receiver of USB endpoint n (handle SETUP/OUT transactions).	0

			0: Expect DATA0. 1: Expect DATA1.	
6	bUEP_T_TOG	RW	Synchronization trigger bit prepared by the transmitter of USB endpoint n (handle IN services). 0: Transmit DATA0. 1: Transmit DATA1.	0
5	Reserved	RO	Reserved	0
4	bUEP_AUTO_TOG	RW	Synchronization trigger bit auto toggle enable control bit 1: Auto toggle the corresponding synchronization trigger bit after sucessful transmission/reception. 0: No auto toggle, but manual switch is allowed. Only for endpoint 1/2/3.	0
3	bUEP_R_RES1	RW	Receiver of endpoint n to SETUP/OUT transactions response control high bit	0
2	bUEP_R_RES0	RW	Receiver of endpoint n to SETUP/OUT transactions response control low bit	0
1	bUEP_T_RES1	RW	Transmitter of endpoint n to IN transactions response control high bit	0
0	bUEP_T_RES0	RW	Transmitter of endpoint n to IN transactions response control low bit	0

MASK_UEP_R_RES, consisting of bUEP_R_RES1 and bUEP_R_RES0, is used to control the response of the receiver of endpoint n to the SETUP/OUT transactions. 00: represents reply ACK or ready. 01 represents timeout/no response, it is used for simultaneous/synchronous transfer of non-endpoint 0. 10 represents reply NAK or busy. 11 represents reply STALL or error.

MASK_UEP_T_RES, consisting of bUEP_T_RES1 and bUEP_T_RES0, is used to control the response of the transmitter of endpoint n to the IN transactions. 00 represents reply DATA0/DATA1 or data ready or expected ACK. 01 represents reply DATA0/DATA1 and expected no response, which is used for simultaneous/synchronous transfer of non-endpoint 0. 10 represents reply NAK or busy. 11 represents reply STALL or error.

Endpoint n transmission length register (UEPn_T_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUEPn_T_LEN	RW	Set the number of data bytes that USB endpoint n is ready to transmit	00h

USB endpoint 1, endpoint 4 mode control register (UEP4_1_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP1_RX_EN	RW	0: Endpoint 1 reception disabled. 1: Endpoint 1 reception enabled (OUT).	0
6	bUEP1_TX_EN	RW	0: Endpoint 1 transmission disabled.	0

			1: Endpoint 1 transmission enabled (IN).	
5	Reserved	RO	Reserved	0
4	bUEP1_BUF_MOD	RW	Endpoint 1 data buffer mode control bit	0
3	bUEP4_RX_EN	R0	0: Endpoint 4 reception disabled. 1: Endpoint 4 reception enabled (OUT).	0
2	bUEP4_TX_EN	RW	0: Endpoint 4 transmission disabled. 1: Endpoint 4 transmission enabled (IN).	0
[1:0]	Reserved	RO	Reserved	00b

The data buffer modes of USB endpoint 0 and endpoint 4 are controlled by a combination of bUEP4_RX_EN and bUEP4_TX_EN, refer to the following table.

Table 16.3.2 Endpoint 0 and endpoint 4 buffer modes

bUEP4_RX_EN	bUEP4_TX_EN	Structure description: arrange from low to high with UEP0 DMA as the start address
0	0	Endpoint 0 single 64-byte receive/transmit shared buffers (IN and OUT)
1	0	Endpoint 0 single 64-byte receive/transmit shared buffers. Endpoint 4 single 64-byte receive buffers (OUT)
0	1	Endpoint 0 single 64-byte receive/transmit shared buffers. Endpoint 4 single 64-byte transmit buffers (IN)
1	1	Endpoint 0 single 64-byte receive/transmit shared buffers. Endpoint 4 single 64-byte receive buffers (OUT). Endpoint 4 single 64-byte transmit buffers (IN). All 192 bytes are arranged as follows: UEP0_DMA+0 address: endpoint 0 receive/transmit. UEP0_DMA+64 address: endpoint 4 receive. UEP0_DMA+128: endpoint 4 transmit

USB endpoint 2, endpoint 3 mode control register (UEP2_3_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP3_RX_EN	RW	0: Endpoint 3 reception disabled. 1: Endpoint 3 reception enabled (OUT).	0
6	bUEP3_TX_EN	RW	0: Endpoint 3 transmission disabled. 1: Endpoint 3 transmission enabled (IN).	0
5	Reserved	RO	Reserved	0
4	bUEP3_BUF_MOD	RW	Endpoint 3 data buffer mode control bit	0
3	bUEP2_RX_EN	R0	0: Endpoint 2 reception disabled. 1: Endpoint 2 reception enabled (OUT).	0
2	bUEP2_TX_EN	RW	0: Endpoint 2 transmission disabled. 1: Endpoint 2 transmission enabled (IN).	0
1	Reserved	RO	Reserved	0
0	bUEP2_BUF_MOD	RW	Endpoint 2 data buffer mode control bit	0

The data buffer modes of USB endpoint 1, endpoint 2 and endpoint 3 are controlled by a combination of bUEPn_RX_EN, bUEPn_TX_EN and bUEPn_BUF_MOD(n=1/2/3) respectively, refer to the following table. In the double-64-byte buffer mode, the first 64-byte buffer is selected based on bUEP_*_TOG=0 and the last 64-byte buffer is selected based on bUEP_*_TOG=1 during USB data transfer to implement automatic switch.

Table 16.3.3 Endpoint n buffer modes (n=1/2/3)

bUEPn_RX_EN	bUEPn_TX_EN	bUEPn_BUF_MOD	Structure description: arrange from low to high with UEPn_DMA as the start address
0	0	x	Endpoint is disabled, and the UEPn_DMA buffer is not used.
1	0	0	Single 64-byte receive buffer (OUT)
1	0	1	Double 64-byte receive buffer, selected by bUEP_R_TOG.
0	1	0	Single 64-byte transmit buffer (IN)
0	1	1	Double 64-byte transmit buffer, selected by bUEP_T_TOG.
1	1	0	Single 64-byte receive buffer Single 64-byte transmit buffer
1	1	1	Double 64-byte receive buffer, selected by bUEP_R_TOG. Double 64-byte transmit buffer, selected by bUEP_T_TOG. All 256 bytes are arranged as follows: UEPn_DMA+0 address: endpoint receive when bUEP_R_TOG=0; UEPn_DMA+64 address: endpoint receive when bUEP_R_TOG=1; UEPn_DMA+128 address: endpoint transmit when bUEP_T_TOG=0; UEPn_DMA+192 address: endpoint transmit when bUEP_T_TOG=1

USB endpoint n buffer start address (UEPn_DMA) (n=0/1/2/3):

Bit	Name	Access	Description	Reset value
[7:0]	UEPn_DMA_H	RW	Endpoint n buffer start address high byte, only the lower 5 bits are valid, and the higher 3 bits are always 0.	xxh
[7:0]	UEPn_DMA_L	RW	Endpoint n buffer start address low byte	xxh

Note: The length of the receive buffer >= min (maximum data packet length possibly received + 2 bytes, 64 bytes)

16.4 Host and root hub register

In USB host mode, CH557 provides 1 set of bidirectional host endpoint, including a transmission endpoint OUT and a reception endpoint IN. The maximum data packet length is 64 bytes. The endpoint supports control transfer, bulk transfer, interrupt transfer, and simultaneous/synchronous transfer.

Each USB transaction initiated by host endpoint automatically sets the interrupt flag (UIF_TRANSFER) after processing. The application program can directly query, or query and analyze the interrupt flag register (USB_INT_FG) in the USB interrupt service program, and perform corresponding processing according to each interrupt flag. In addition, if UIF_TRANSFER is valid, it is required to continue to analyze the USB interrupt status register (USB_INT_ST), and perform the corresponding processing according to the response PID (MASK_UIS_H_RES) of the current USB transfer transaction.

If the synchronization trigger bit (bUH_R_TOG) of IN transaction of host reception endpoint is set in advance, you can judge whether the synchronization trigger bit of the data packet received matches the synchronization trigger bit of the endpoint through U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data is valid. If the data is not synchronized, the data should be discarded. Every time the USB transmit or receive interrupt is processed, the synchronization trigger bit of corresponding host endpoint should be modified correctly to synchronize the data packet sent next time and detect whether the data packet received next time is synchronized. In addition, bUEP_AUTO_TOG can be set to automatically toggle the corresponding synchronization trigger bit after successful transmission/reception.

USB host token setting register (UH_EP_PID) is a multiplexing of the USB endpoint 2 control register in USB device mode, which is used to set the endpoint number of the target device being operated and the token PID of the USB transfer transaction. The data corresponding to the SETUP token and OUT token is provided by the host transmission endpoint. The data to be sent is in the UH_TX_DMA buffer, and the length of the data to be sent is set in UH_TX_LEN. The data corresponding to the IN token is returned by the target device to the host reception endpoint, the received data is stored in the UH_RX_DMA buffer, and the received data length is stored in USB_RX_LEN.

Table 16.4.1 USB host registers (those marked in grey are controlled by RB_UC_RESET_SIE reset)

Name	Address	Description	Reset value
UHOST_CTRL	D1h	USB host physical port control register	0000 0000b
UHUB01_CTRL	D1h	USB host root hub0 and hub1 port control register	0000 0000b
UHUB23_CTRL	E1h	USB host root hub2 and hub3 port control register	0000 0000b
UH_SETUP	D2h	USB host auxiliary setup register	0000 0000b
UH_RX_CTRL	D4h	USB host reception endpoint control register	0000 0000b
UH_EP_PID	D5h	USB host token setup register	0000 0000b
UH_TX_CTRL	D6h	USB host transmission endpoint control register	0000 0000b
UH_TX_LEN	D7h	USB host transmission length register	0000 0000b
UH_RX_DMA_H	E5h	USB host receive buffer start address high byte	000x xxxxb
UH_RX_DMA_L	E4h	USB host receive buffer start address low byte	xxxx xxxxb
UH_RX_DMA	E4h	UH_RX_DMA_L and UH_RX_DMA_H constitute a 16-bit SFR	xxxxh
UH_TX_DMA_H	E7h	USB host transmit buffer start address high byte	000x xxxxb
UH_TX_DMA_L	E6h	USB host transmit buffer start address low byte	xxxx xxxxb
UH_TX_DMA	E6h	UH_TX_DMA_L and UH_TX_DMA_H constitute a 16-bit SFR	xxxxh
UH_EP_MOD	21E1h	USB host endpoint mode control register	0000 0000b

USB host physical port control register (UHOST_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
[7:4]	Reserved	RO	Reserved	0000b
3	bUH_PD_EN	RW	USB host port DP/DM/HP0/HM0 pin internal	0

			pull-down resistor enable bit 1: Internal pull-down resistor enabled. 0: Internal pull-down resistor disabled. This bit also can be used in GPIO mode to provide a pull-down resistor	
2	bUH_LOW_SPEED	RW	USB host port low-speed mode enable bit 1: Low speed mode, 1.5Mbps. 0: Full speed mode, 12Mbps.	0
1	bUH_BUS_RESET	RW	USB host port bus reset control bit 1: Force the host port to output USB bus reset. 0: End the output.	0
0	bUH_PORT_EN	RW	USB host port enable bit 0: Host port disabled. 1: Host port enabled. The bit is cleared automatically when the USB device is disconnected.	0

USB host root hub0 and hub1 port control register (UHUB01_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
7	bUH1_PD_EN	RW	USB host hub1 port HP1/HM1 pin internal pull-down resistor enable bit 1: Internal pull-down resistor enabled. 0: Internal pull-down resistor disabled. This bit also can be used in GPIO mode to provide pull-down resistor	0
6	bUH1_LOW_SPEED	RW	USB host hub1 port low speed mode enable bit 1: Low speed mode, 1.5Mbps. 0: Full speed mode, 12Mbps.	0
5	bUH1_BUS_RESET	RW	USB host hub1 port bus reset control bit 1: Force the hub1 port to output USB bus reset. 0: End the output	0
4	bUH1_PORT_EN	RW	USB host hub1 port enable bit 0: Hub1 port disabled. 1: Hub1 port enabled. The bit is cleared automatically when the USB device is disconnected	0
3	bUH0_PD_EN	RW	USB host hub0 port HP0/HM0 pin internal pull-down resistor enable bit 1: Internal pull-down resistor enabled. 0: Internal pull-down resistor disabled. This bit also can be used in GPIO mode to provide pull-down resistor	0
2	bUH0_LOW_SPEED	RW	USB host hub0 port low speed mode enable bit 1: Low speed mode, 1.5Mbps.	0

			0: Full speed mode, 12Mbps.	
1	bUH0_BUS_RESET	RW	USB host hub0 port bus reset control bit 1: Force the hub0 port to output USB bus reset. 0: End the output	0
0	bUH0_PORT_EN	RW	USB host hub0 port enable bit 0: Hub0 port disabled. 1: Hub0 port enabled. This bit is cleared automatically when the USB device is disconnected.	0

USB host root hub2 and hub3 port control register (UHUB23_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
7	bUH3_PD_EN	RW	USB host hub3 port HP3/HM3 pin internal pull-down resistor enable bit 1: Internal pull-down resistor enabled. 0: Internal pull-down resistor disabled. This bit also can be used in GPIO mode to provide pull-down resistor	0
6	bUH3_LOW_SPEED	RW	USB host hub3 port low speed mode enable bit 1: Low speed mode, 1.5Mbps. 0: Full speed mode, 12Mbps.	0
5	bUH3_BUS_RESET	RW	USB host hub3 port bus reset control bit 1: Force the hub3 port to output USB bus reset. 0: End the output	0
4	bUH3_PORT_EN	RW	USB host hub3 port enable bit 0: Hub3 port disabled. 1: Hub3 port enabled. This bit is cleared automatically when the USB device is disconnected	0
3	bUH2_PD_EN	RW	USB host hub2 port HP2/HM2 pin internal pull-down resistor enable bit 1: Internal pull-down resistor enabled. 0: Internal pull-down resistor disabled. This bit also can be used in GPIO mode to provide pull-down resistor	0
2	bUH2_LOW_SPEED	RW	USB host hub2 port low speed mode enable bit 1: Low speed mode, 1.5Mbps. 0: Full speed mode, 12Mbps.	0
1	bUH2_BUS_RESET	RW	USB host hub2 port bus reset control bit 1: Force the hub2 port to output USB bus reset. 0: End the output	0
0	bUH2_PORT_EN	RW	USB host hub2 port enable bit 0: Hub1 port disabled. 1: Hub2 port enabled.	0

			This bit is cleared automatically when the USB device is disconnected.	

USB host auxiliary setup register (UH_SETUP):

Bit	Name	Access	Description	Reset value
7	bUH_PRE_PID_EN	RW	Low speed preamble packet PRE PID enable bit 1: USB host enabled to communicate with the low-speed USB device via external HUB. 0: Low speed preamble packet disabled, and there should be no HUB between the USB host and low-speed USB device.	0
6	bUH_SOF_EN	RW	SOF packet auto generate enable bit 1: USB host automatically generates the SOF packet. 0: SOF packet is not generated automatically, but can be generated manually.	0
[5:0]	Reserved	RO	Reserved	00h

USB host reception endpoint control register (UH_RX_CTRL):

Bit	Name	Access	Description	Reset value
7	bUH_R_TOG	RW	Synchronization trigger bit expected by the receiver of USB host (handle IN services). 0: Expect DATA0. 1: Expect DATA1.	0
[6:5]	Reserved	RO	Reserved	00b
4	bUH_R_AUTO_TOG	RW	Auto toggle bUH_R_TOG enable control bit 1: Auto toggle the bUH_R_TOG flag after successfully received by the USB host. 0: No auto toggle, but manual switch is allowed.	0
3	Reserved	RO	Reserved	0
2	bUH_R_RES	RW	Response control bit of USB host receiver for IN transaction 0: Reply ACK or ready. 1: No reponse, which is used for simultaneous/synchronous transfer with non-endpoint 0 of the target device	0
[1:0]	Reserved	RO	Reserved	00b

USB host token setup register (UH_EP_PID):

Bit	Name	Access	Description	Reset value
[7:4]	MASK_UH_TOKEN	RW	Set the token PID of this USB transfer transaction	0000b
[3:0]	MASK_UH_ENDP	RW	Set the endpoint serial number of the target device	0000b

			being operated this time	

USB host transmission endpoint control register (UH_TX_CTRL):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUH_T_TOG	RW	Synchronization trigger bit prepared by the transmitter of USB host (handle SETUP/OUT transactions). 0: Transmit DATA0. 1: Transmit DATA1	0
5	Reserved	RO	Reserved	0
4	bUH_T_AUTO_TOG	RW	Auto toggle bUH_T_TOG enable control bit 1: Auto toggle the bUH_T_TOG flag after successfully transmitted by the USB host. 0: No auto toggle, but manual switch is allowed.	0
[3:1]	Reserved	RO	Reserved	000b
0	bUH_T_RES	RW	Response control bit of USB host transmitter for SETUP/OUT transaction 0: Expect reply ACK or ready. 1: Expect no reponse, which is used for simultaneous/synchronous transfer with non-endpoint 0 of the target device.	0

USB host transmission length register (UH_TX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	UH_TX_LEN	RW	Set the number of data bytes that USB host transmission endpoint is ready to send	00h

USB host endpoint mode control register (UH_EP_MOD):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUH_EP_TX_EN	RW	0: USB host transmission endpoint disabled to transmit data. 1: USB host transmission endpoint enabled to transmit data (SETUP/OUT)	0
5	Reserved	RO	Reserved	0
4	bUH_EP_TBUF_MOD	RW	USB host transmission endpoint data buffer mode control bit	0
3	bUH_EP_RX_EN	RO	0: USB host reception endpoint disabled to receive data. 1: USB host reception endpoint enabled to receive data (IN)	0

[2:1]	Reserved	RO	Reserved	00b
0	bUH_EP_RBUF_MOD	RW	USB host reception endpoint data buffer mode control bit	0

The data buffer modes of USB host transmission endpoint are controlled by a combination of bUH_EP_TX_EN and bUH_EP_TBUF_MOD, refer to the following table.

Table 16.4.2 Host transmit buffer modes

bUH_EP_TX_EN	bUH_EP_TBUF_MOD	Structure description: Take UH_TX_DMA as the start address
0	x	Endpoint is disabled, and the UH_TX_DMA buffer is not used
1	0	Single 64-byte transmit buffers (SETUP/OUT)
1	1	Double 64-byte transmit buffers, selected by bUH_T_TOG: When bUH_T_TOG=0, select the first 64-byte buffer. When bUH_T_TOG=1, select the last 64-byte buffer.

The data buffer modes of USB host reception endpoint are controlled by a combination of bUH_EP_RX_EN and bUH_EP_RBUF_MOD, refer to the following table.

Table 16.4.3 Host receive buffer modes

bUH_EP_RX_EN	bUH_EP_RBUF_MOD	Structure description: Take UH_RX_DMA as the start address
0	x	Endpoint is disabled, and the UH_RX_DMA buffer is not used
1	0	Single 64-byte receive buffers (IN)
1	1	Double 64-byte receive buffers, selected by bUH_R_TOG: When bUH_R_TOG=0 select the first 64-byte buffer. When bUH_R_TOG=1, select the last 64-byte buffer.

USB host receive buffer start address (UH_RX_DMA)

Bit	Name	Access	Description	Reset value
[7:0]	UH_RX_DMA_H	RW	USB host receive buffer start address high byte. Only the lower 5 bits are valid, and the higher 3 bits are always 0.	xxh
[7:0]	UH_RX_DMA_L	RW	USB host receive buffer start address low byte	xxh

USB host transmit buffer start address (UH_TX_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	UH_TX_DMA_H	RW	USB host transmit buffer start address high byte. Only the lower 5 bits are valid, and the higher 3 bits are always 0.	xxh
[7:0]	UH_TX_DMA_L	RW	USB host transmit buffer start address low byte	xxh

17. Inter-integrated circuit (I2C) interface

17.1 I2C introduction

CH557 provides I2C master (I2CM) and I2C slave (I2CS) interfaces. The main features are as follows:

(1). I2C general master controller (master), supporting interrupt, with adjustable clock frequency.

(2). I2C slave controller is mainly used for DDC/EDID slave or external analog EEPROM memory 24CXX chip.

(3). I2C slave controller supports continuous reading as well as DMA and interrupt.

(4). I2C slave controller can preset local slave address, and support broadcast address.

(5). All I2C interface pins are built with controllable pull-up resistor, and no external pull-up resistor is required for the medium- and low- speed applications.

17.2 I2C global and master register

Table 17.2.1 I2C global and I2CM registers

Name	Address	Description	Reset value
I2CX_INT	B3h	I2C, PWMX and RGB LED interrupt request register	0000 0000b
I2CS_INT_ST	BBh	Mapping of I2CS slave status register I2CS_STAT	0000 1100b
I2CM_CTRL	21C0h	I2CM control register	000x 0000b
I2CM_CK_SE	21C1h	I2CM clock setting register	0000 0000b
I2CM_START	21C2h	I2CM start register	xxxx xxxxb
I2CM_DATA	21C3h	I2CM data register	xxxx xxxxb
I2CM_STAT	21C4h	I2CM status register	0000 0000b

I2C, PWMX and RGB LED interrupt request register (I2CX_INT):

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	Reserved	00b
5	bI2CS_INT_ACT	RO	I2CS interrupt request status 0: Idle, and there is no interrupt request. 1: I2CS is requesting an interrupt.	0
4	bI2CM_INT_ACT	RO	I2CM interrupt request status 0: Idle, and there is no interrupt request. 1: I2CM is requesting an interrupt.	0
[3:2]	Reserved	RO	Reserved	00b
1	bLED_INT_ACT	RO	RGB LED interrupt request state 0: Idle, and there is no interrupt request. 1: RGB LED is requesting an interrupt	0
0	bPWMX_INT_ACT	RO	PWMX interrupt request status 0: Idle, and there is no interrupt request. 1: PWMX is requesting an interrupt	0

I2CS status register mapping (I2CS_INT_ST), I2CS status register (I2CS_STAT):

Bit	Name	Access	Description	Reset value
7	bI2CS_IF_STASTO	RW	Receive START or STOP condition interrupt flag bit 1: There is an interrupt. START or STOP is further determined according to MASK_I2CS_STAT. 0: No interrupt. Write 1 to reset.	0
6	bI2CS_IF_BYTE	RW	A data byte transfer completed interrupt flag bit 1: There is an interrupt, triggered after one byte is received/transmitted. 0: No interrupt. Write 1 to reset.	0
5	bI2CS_IF_ADDR	RW	Receive data unit address interrupt flag bit 1: There is an interrupt, triggered after the data address is received. 0: No interrupt. Write 1 to reset.	0
4	bI2CS_IF_DEV_A	RW	Receive slave device address interrupt flag bit 1: There is an interrupt, triggered after the slave address is received, no matter the address matches or not. 0: No interrupt. Write 1 to reset.	0
[3:0]	MASK_I2CS_STAT	RO	I2CS slave current state: 0000: Idle, or is receiving slave address. 0001: Reply the received slave address. 0010: Is receiving data unit address. 0011: Reply the received data unit address. 0100: Is receiving data byte. 0101: Reply the received data byte. 0110: Is transmitting data byte. 0111: Is waiting and checking the response after the data is transmitted. 1100: In STOP condition. XXXX: Unknown status.	1100b

I2CM control register (I2CM_CTRL):

Bit	Name	Access	Description	Reset value
7	bI2CM_IE	RW	I2CM operation completed interrupt enable bit 1: I2CM enabled to transmit interrupt. 0: I2CM disabled to request an interrupt.	0
[6:5]	Reserved	RO	Reserved	00b
4	bI2CM_DEV_ACK	RO	Recently received I2C slave acknowledge state 1: No acknowledge.	x

			0: Valid acknowledge (SDA=0)	
3	bI2CM_EN	RW	I2CM master enable 0: Disabled, and clear I2CM master. 1: I2CM master enabled.	0
2	Reserved	RO	Reserved	0
[1:0]	MASK_I2CM_CMD	RW	I2CM master operation command, automatically return 00 after the operation: 00: Idle, or no operation; 01: STOP condition generated; 10: Receive one byte and reply ACK; 11: Receive one byte, no reply, STOP condition generated	00b

I2CM status register (I2CM_STAT):

Bit	Name	Access	Description	Reset value
7	bI2CM_IF	RW	I2CM operation completed interrupt flag bit. If this bit is 1, operation is completed. Write 1 to reset, or reset when the new operation is executed (write to I2CM_CTRL, or write to I2CM_START, or write to I2CM_DATA)	0
[6:4]	MASK_I2CM_STAT	RO	Current status of I2CM master: 000: Odle, or operation is completed; 001/010/011: In the 3 steps of START or STOP; 100/101/110/111: Is receiving or transmitting byte data or processing the 4 steps of reply	000b
[3:0]	MASK_I2CM_CNT	RO	Current operation step and data bit counting status of I2CM master	0000b

I2CM clock setting register (I2CM_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	I2CM_CK_SE	RW	Set I2C master clock frequency division factor, and then used for MSCL after divided by 4.	00h

I2CM start register (I2CM_START):

Bit	Name	Access	Description	Reset value
[7:0]	I2CM_START	RW	Writing one byte automatically generates the START condition. This byte is transmitted as the first data and receives the reply, which is stored in bI2CM_DEV_ACK. The first data is ususally a 7-bit slave address and a 1-bit read-write command	xxh

I2CM data register (I2CM_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	I2CM_DATA	RW	I2CM data register includes a transmit register and a receive register that are physically separated. Writing one byte will automatically send such byte data, receive reply and store it in bI2CM_DEV_ACK. Reading this register will return to the data in the serial shift register, usually the recently received byte data	xxh

17.3 I2C slave register

Table 17.3.1 I2CS slave registers

Name	Address	Description	Reset value
I2CS_CTRL	2232h	I2CS control register	0000 0x00b
I2CS_DEV_A	2233h	I2CS device address register	0000 0000b
I2CS_ADDR	2235h	I2CS data address register (read-only)	xxxx xxxxb
I2CS_DATA	2236h	I2CS data receive/transmit register	xxxx xxxxb
I2CS_STAT	223Ah	I2CS status register	0000 1100b
I2CS_DMA_L	2139h	I2CS slave buffer start address low byte	xxxx xxxxb
I2CS_DMA_H	2138h	I2CS slave buffer start address high byte	000x xxxxb

I2CS control register (I2CS_CTRL):

Bit	Name	Access	Description	Reset value
7	bI2CS_IE_TRAN	RW	I2CS transmit data interrupt enable bit 1: Interrupt triggered after one data byte is transmitted. 0: Interrupt not triggered	0
6	bI2CS_IE_RECV	RW	I2CS receive data interrupt enable bit 1: Interrupt triggered after one data byte is received. 0: Interrupt not triggered.	0
5	bI2CS_IE_ADDR	RW	I2CS receive data address interrupt enable bit 1: Interrupt triggered after the data address is received. 0: Interrupt not triggered.	0
4	bI2CS_IE_DEV_A	RW	I2CS receive slave address interrupt enable bit 1: Interrupt triggered after the slave address is received. 0: Interrupt not triggered. If the bit is 1, it will enable the broadcast address, otherwise it will not support the broadcast address.	0
3	bI2CS_IE_STASTO	RW	I2CS receive START or STOP condition interrupt enable bit	0

			1: Interrupt triggered after START or STOP condition is received. 0: Interrupt not triggered.	
2	bI2CS_SDA_IN	RO	Current SDA0 pin status after synchronization: 0: Low level. 1: High level.	x
1	bI2CS_DMA_EN	RW	I2CS read data DMA enable 1: DMA enabled, only support DMA to read data. When the data is read by the external I2C host, it is automatically obtained via DMA before being sent. 0: DMA disabled, and the data can be exchanged by reading/writing to I2CS_DATA.	0
0	bI2CS_EN	RW	I2CS slave enable 0: Disabled, and reset I2CS slave. 1: I2CS slave enabled.	0

I2CS device address register (I2CS_DEV_A):

Bit	Name	Access	Description	Reset value
[7:1]	MASK_I2CS_DEV_A	RW	I2CS slave device address value 0: Broadcast address. Other values: Assigned slave device addresses that need to be matched	00h
0	bI2CS_DA_4BIT	RW	I2CS slave device address mode: 0: 7-bit slave address mode, I2CS_ADDR is actually 8 bits. 1: 4-bit slave address mode, only the higher 4 bits of the slave device address need to be matched other than the lower 3 bits. The lower 3 bits of the target address are stored in MASK_I2CS_AH. When DMA is reading data, the actual extension of I2CS_ADDR is 11 bits, whose higher 3 bits are from MASK_I2CS_AH.	0

I2CS data address register (I2CS_ADDR):

Bit	Name	Access	Description	Reset value
[7:0]	I2CS_ADDR	RO	Store the data unit address specified by the external I2C master, which is automatically increased after each byte during a sequential read-write operation.	xxh

I2CS slave data receive/transmit register (I2CS_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	I2CS_DATA	RW	I2CS slave data receive/transmit register includes a transmit	xxh

			register and a receive register that are physically separated. The data written into this register is sent for the external I2C master to read, or it can be read by DMA instead. Reading this register will return to the data in the receive buffer, ussually the data that is recently written by the external I2C master.	

I2CS status register (I2CS_STAT), refer to I2CS_INT_ST in Section 17.2.

I2CS buffer start address (I2CS_DMA_H, I2CS_DMA_L):

Bit	Name	Access	Description	Reset value
[7:0]	I2CS_DMA_H	RW	I2CS slave buffer start address higher byte, only the lower 5 bits are valid. When bI2CS_DA_4BIT=0, the higher 3 bits are 0; when bI2CS_DA_4BIT=1, read the higher 3 bits and return to MASK_I2CS_AH	xxh
[7:5]	MASK_I2CS_AH	RO	When bI2CS_DA_4BIT=1, store the lower 3 bits of the received target slave device address, and the higher 3 bits as the data unit address are used for DMA	xxxb
[7:0]	I2CS_DMA_L	RW	I2CS slave buffer start address lower byte	xxh

When bI2CS_DA_4BIT=0, current data DMA address = I2CS_DMA + I2CS_ADDR.
When bI2CS_DA_4BIT=1, current data DMA address = I2CS_DMA + { MASK_I2CS_AH, I2CS_ADDR }.

18. RGB LED controller

18.1 RGB LED Introduction

CH557 is built with RGB LED controller. The main features are as follows:

(1). 3*8=24 channels of PWM and 1/16 dynamic scanning, support 384 single-color LEDs or 128 groups of RGB tri-color LEDs.

(2). Optional, 7-bit or 8-bit color PWM, the maximum 3*8-bit color PWM supports 16777216 combined colors.

(3). Optional, 6-bit or 7-bit or 8-bit brightness PWM supports level-256 grayscale;

(4). Multistage adjustable blanking time, support color PWM repeated framing, and support 1/2 to 1/16 dynamic scanning.

(5). Dedicated DMA mode that supports loading the preset fixed data from Flash-ROM or the edited data from xRAM.

The following is the RGB LED driver structure of CH557, which supports 384 single color LEDs, for reference only.

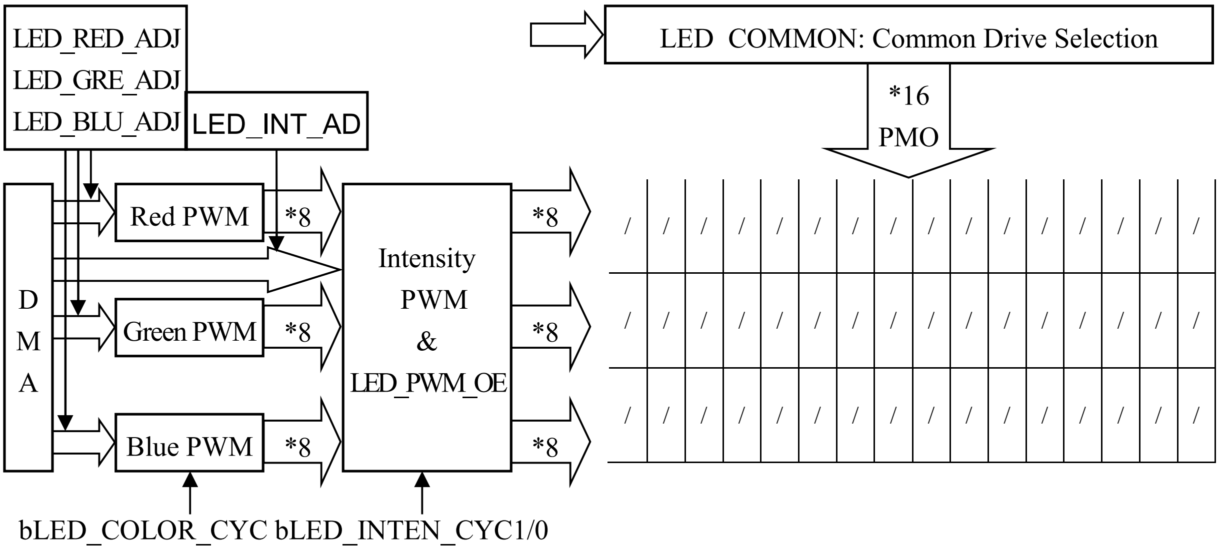


Table 18.1.1 RGB LED registers

Name	Address	Description	Reset value
LED_CTRL	21D1h	RGB LED control register	0000 0000b
LED_CYCLE	21D2h	RGB LED cycle configuration register	0000 0000b
LED_FRAME	21D3h	RGB LED frame configuration register	0000 0000b
LED_PWM_OE	A7h	RGB LED drive PWM pin enable register	0000 0000b
LED_COMMON	A6h	RGB LED drive COMMON pin selection register	0000 0000b
LED_STATUS	F7h	RGB LED status register	0001 xxxxb
LED_DMA_H	C7h	RGB LED buffer current address high byte	xxxx xxxxb
LED_DMA_L	C6h	RGB LED buffer current address low byte	xxxx xxxxb
LED_DMA	C6h	LED_DMA_L and LED_DMA_H constitute a 16-bit SFR	xxxxh
LED_INT_ADJ	21D8h	RGB LED brightness adjustment register	0000 0000b
LED_RED_ADJ	21D9h	RGB LED red adjustment register	0000 0000b
LED_GRE_ADJ	21DAh	RGB LED green adjustment register	0000 0000b
LED_BLU_ADJ	21DBh	RGB LED blue adjustment register	0000 0000b
LED_FRA_STA	21DCh	RGB LED frame status register (read only)	0000 0000b
LED_COL_CNT	21DDh	RGB LED color counter register (read only)	0000 0000b

RGB LED control register (LED_CTRL):

Bit	Name	Access	Description	Reset value
7	bLED_IE_INHIB	RW	RGB LED frame end interrupt enable bit 1: Interrupt triggered at the end of one PWM. 0: Interrupt not triggered.	0
6	bLED_BLUE_EN	RW	Blue PWM pin group BLU0~BLU7 output enable 0: Blue PWM output disabled. 1: Blue PWM output enabled.	0
5	bLED_GREEN_EN	RW	Green PWM pin group GRE0~GRE7 output enable	0

			0: Green PWM output disabled. 1: Green PWM output enabled.	
4	bLED_RED_EN	RW	Red PWM pin group RED0~RED7 output enable 0: Red PWM output disabled. 1: Red PWM output enabled.	0
3	bLED_COM_AHEAD	RW	RGB LED scanning driver pre-charging mode: 0: Normally start PMOS; 1: Start PMOS one clock in advance to allow its gate to charge	0
2	bLED_PWM_INHIB	RW	RGB LED automatic blanking mode: 0: Keep PWM output during scanning switch; 1: Automatically reset bLED_PWM0_OE at the end of the frame to automatically disable PWM output during scanning switch;	0
1	Reserved	RO	Reserved	0
0	bLED_EN	RW	RGB LED enable 0: Disabled, and reset RGB LED. 1: RGB LED clock enabled.	0

RGB LED cycle configuration register (LED_CYCLE):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bLED_COLOR_CYC	RW	Select the color PWM data width and PWM cycle: 0: 8 bits, 256 brightness PWM cycles. 0: 7 bits, 128 brightness PWM cycles.	0
[5:4]	MASK_LED_INT_CYC	RW	Select the brightness PWM data width and PWM cycle: 00: 8 bits, 256 reference clocks. 01: 7 bits, 128 reference clocks. 10/11: 6 bits, 64 reference clocks.	00b
[3:2]	Reserved	RO	Reserved	00b
[1:0]	MASK_LED_CLK_FREQ	RW	Select RGB LED and brightness PWM reference clock: 00: Fsys. 01: Fsys/2. 10: Fsys/3. 11: Fsys/4.	00b

RGB LED frame configuration register (LED_FRAME):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
[6:4]	MASK_LED_INH_TMR	RW	Select the scanning switch time with the brightness PWM cycle as the unit: 000~011: 1~ 4 brightness PWM cycles	000b

			respectively. 100: 6 brightness PWM cycles. 101: 8 brightness PWM cycles. 110: 10 brightness PWM cycles. 111: 12 brightness PWM cycles.	
3	Reserved	RO	Reserved	0
[2:0]	MASK_LED_PWM_REPT	RW	Select the number of color PWM repetitions in a PWM frame, 000~111: Repeat 1 ~ 8 times respectively.	000b

RGB LED drive PWM pin enable register (LED_PWM_OE):

Bit	Name	Access	Description	Reset value
7	bLED_PWM7_OE	RW	PWM7 pin group output enable 0: PWM7 group output disabled. 1: PWM7 group output enabled.	0
6	bLED_PWM6_OE	RW	PWM6 pin group output enable 0: PWM6 group output disabled. 1: PWM6 group output enabled.	0
5	bLED_PWM5_OE	RW	PWM5 pin group output enable 0: PWM5 group output disabled. 1: PWM5 group output enabled.	0
4	bLED_PWM4_OE	RW	PWM4 pin group output enable 0: PWM4 group output disabled. 1: PWM4 group output enabled.	0
3	bLED_PWM3_OE	RW	PWM3 pin group output enable 0: PWM3 group output disabled. 1: PWM3 group output enabled.	0
2	bLED_PWM2_OE	RW	PWM2 pin group output enable 0: PWM2 group output disabled. 1: PWM2 group output enabled.	0
1	bLED_PWM1_OE	RW	PWM1 pin group output enable 0: PWM1 group output disabled. 1: PWM1 group output enabled.	0
0	bLED_PWM0_OE	RW	PWM0 pin group and global PWM output enable 0: PWM0 group and global PWM output disabled. 1: PWM0 group output enabled. When bLED_PWM_INHIB=1, this bit is automatically cleared at the end of each PWM frame to implement automatic blanking during scanning switch	0

RGB LED drive COMMON pin selection register (LED_COMMON):

Bit	Name	Access	Description	Reset value
[7:0]	LED_COMMON	RW	Select the dynamically scanned COMMON pin. Only the lower 5 bits are active: 01110: Select COM14, P7.0. 01111: Select COM15, P7.1. 10000~10111: COM16~COM23, P0.0~P0.7 respectively. 11000~11111: COM24~COM31, P3.0~P3.7 respectively.	00h

RGB LED status register (LED_STATUS):

Bit	Name	Access	Description	Reset value
7	bLED_IF	RW	RGB LED frame end interrupt flag bit. If this bit is 1, an end of frame has occurred. Write 1 to reset, or reset when writing to LED_COMMON (scanning switch)	0
6	bLED_IF_SET	WO	Write 1 to force bLED_IF to set 1, so as to enter the interrupt service program	0
5	Reserved	RO	Reserved	0
4	bLED_INHIB	RO	RGB LED frame status 1: Idle, or in scanning switch period that allows scanning switch and loading new data. 0: In normal PWM drive period	1
[3:0]	MASK_LED_INTEN	RO	Higher 4 bits of brightness PWM counter	xxxx

RGB LED buffer current address (LED_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	LED_DMA_H	RW	RGB LED data buffer current address high byte	xxh
[7:0]	LED_DMA_L	RW	RGB LED data buffer current address low byte	xxh

RGB LED brightness adjustment register (LED_INT_ADJ), RGB LED red adjustment register (LED_RED_ADJ), RGB LED green adjustment register (LED_GRE_ADJ), RGB LED blue adjustment register (LED_BLU_ADJ):

Bit	Name	Access	Description	Reset value
[7:0]	LED_INT_ADJ	RW	RGB LED brightness adjustment value, -128~127. The highest bit represents symbol. The adjustment value is automatically added to the brightness PWM when the brightness data is loaded	00h
[7:0]	LED_RED_ADJ	RW	RGB LED red adjustment value, -128~127. The highest bit represents symbol. The adjustment value is automatically added to the red PWM when the red data is loaded	00h

[7:0]	LED_GRE_ADJ	RW	RGB LED green adjustment value, -128~127. The highest bit represents symbol. The adjustment value is automatically added to the green PWM when the green data is loaded	00h
[7:0]	LED_BLU_ADJ	RW	RGB LED blue adjustment value, -128~127. The highest bit represents symbol. The adjustment value is automatically added to the blue PWM when the blue data is loaded	00h

RGB LED frame status register (LED_FRA_STA):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
[6:4]	MASK_LED_REPEAT	RO	The repeated counting value of the current color PWM within the PWM frame	000b
[3:0]	MASK_LED_INHIB	RO	Current counting value of the scanning switch time with the brightness PWM cycle as the unit	0000b

RGB LED color counter register (LED_COL_CNT):

Bit	Name	Access	Description	Reset value
[7:0]	LED_COL_CNT	RO	Color PWM counter	00h

19. Parameters

19.1 Absolute maximum ratings

Operating in critical ratings or exceeding the absolute maximum ratings may cause the chip to work abnormally or even be damaged.

Symbol	Parameter description		Min.	Max.	Unit
TA	Operating ambient temperature	Fsys<40MHz	-40	85	℃
		Fsys=48MHz (bLDO_CORE_VOL=1 if necessary)	-40	70	℃
		Fsys=48MHz (it is recommended that bLDO_CORE_VOL=0)	-20	70	℃
TAROM	Ambient temperature when performing erase/write operation on Flash-ROM/EEPROM (recommended)		-20	85	℃
TS	Storage ambient temperature		-55	125	℃
VDD	Supply voltage (VDD is connected to power, GND to ground)		-0.4	7.0	V
V33	Internal USB supply voltage		-0.4	VDD+0.4	V
VIO	Voltage on input/output pins		-0.4	VDD+0.4	V
VIOP6	Voltage on P6 pin		-0.4	V33+0.4	V
VIOU	Voltage on DP/DM/HP*/HM*		-0.4	V33+0.4	V

19.2 Electrical characteristics (5V)

Test conditions: TA=25°C, VDD=5V, Fsys=12MHz.

Symbol	Parameter description		Min.	Typ.	Max.	Unit
VDD5	VDD pin supply voltage	V33 is only connected to an external capacitor	3.7	5	6.6	V
V33	Internal power regulator output voltage (Automatically shorted to VDD during sleep)	TA=-15～65°C	3.23	3.3	3.52	V
		TA=-40～85°C	3.2	3.3	3.55	V
ICC32M5	Total supply current when Fsys=32MHz			6.2		mA
ICC12M5	Total supply current when Fsys=12MHz			3.4		mA
ICC750K5	Total supply current when Fsys=750KHz			1.5		mA
ISLP5	Total supply current after standby/normal sleep			1.1	1.4	mA
ISLP5L	bLDO_3V3_OFF=1, turn off LDO, Total supply current after power off/deep sleep			6	15	uA
IADC5	ADC operating current			200	600	uA
ICMP5	ADC operating current			70	100	uA
ITKEY5	Voltage comparator operating current		30	50	70	uA
VIL5	Low level input voltage		0		1.2	V
VIH5	High level input voltage		2.6		VDD	V
VIHP6	High level input voltage on P6 pin		2.1		V33	V
VOL5	Low level output voltage (20mA sunk current)				0.4	V
VOH5	High level output voltage (10mA sourced current)		VDD-0.4			V
VOLP6	Low level output voltage on P6 pin (8mA sunk current)				0.4	V
VOHP6	High level output voltage on P6 pin (8mA sourced current)		V33-0.4			V
VOH5U	High level output voltage on USB pins (8mA sourced current)		V33-0.4			V
IIN	Sunk current of input without pull-up resistor		-5	0	5	uA
IUP5	Sunk current of input with pull-up resistor except P6		35	70	110	uA
IUP5X	Sunk current of input with pull-up resistor from low to high except P6		250	400	600	uA
IUP5I	Sunk current of input of I2C pin with pull-up resistor		330	660	1000	uA
Rdn5	P2.0～P2.3 pin pull-down resistance		18	26	35	KΩ
Rsw5	ON resistance of the analog switch of ADC and other modules		500	700	1350	Ω
Vpot	Power on reset threshold		2.3	4.0	4.6	V

19.3 Electrical characteristics (3.3V)

Test Conditions: TA=25℃, VDD=V33=3.3V, Fsys=12MHz.

Symbol	Parameter description		Min.	Typ.	Max.	Unit
VDD3	Supply voltage on VDD pin	V33 is shorted to VDD, with USB ON	3.0	3.3	3.6	V
		V33 is shorted to VDD, with USB OFF	2.6	3.3	3.6	V
ICC32M3	Total supply current when Fsys=32MHz			6.0		mA
ICC12M3	Total supply current when Fsys=12MHz			3.3		mA
ICC750K3	Total supply current when Fsys=750KHz			1.5		mA
ISLP3	Total supply current after standby/normal sleep			1.1	1.3	mA
ISLP3L	bLDO_3V3_OFF=1, turn off LDO, Total supply current after power off/deep sleep			3	12	uA
IADC3	ADC operating current			180	500	uA
ICMP3	Voltage comparator operating current			60	100	uA
ITKEY3	Touch key capacitance charging current		30	50	70	uA
VIL3	Low level input voltage		0		0.8	V
VIH3	High level input voltage		2.0		VDD	V
VIHP6	High level input voltage on P6 pin		2.1		V33	V
VOL3	Low level output voltage (12mA sunk current)				0.4	V
VOH3	High level output voltage (6mA sourced current)		VDD-0.4			V
VOLP6	Low level output voltage on P6 pin (8mA sunk current)				0.4	V
VOHP6	High level output voltage on P6 pin (8mA sourced current)		V33-0.4			V
VOH3U	High level output voltage on USB pins (8mA sourced current)		V33-0.4			V
IIN	Sunk current of input without pull-up resistor		-5	0	5	uA
IUP3	Sunk current of input with pull-up resistor except P6		15	30	50	uA
IUP3X	Sunk current of input with pull-up resistor during from low to high Except P6		100	170	260	uA
IUP3I	Sunk current of input of I2C pin with the pull-up resistor		140	280	440	uA
Rdn3	P2.0～P2.3 pin pull-down resistance		18	26	35	KΩ
Rsw3	ON resistance of the analog switch of ADC and other modules		600	1000	2500	Ω
Vpot	Power on reset threshold		2.3	2.7	3.0	V

19.4 Timing parameters

Test conditions: TA=25°C, VDD=5V or VDD=V33=3.3V, Fsys=12MHz

Symbol	Parameter description		Min.	Typ.	Max.	Unit
Fxt	External crystal frequency or XI input clock frequency		6	24	24	MHz
Fosc	Internal clock frequency after calibration when VDD>=3V	TA=-15～65°C	23.64	24	24.36	MHz
		TA=-40～85°C	23.5	24	24.5	MHz
Fosc3	Internal clock frequency after calibration when VDD<3V		23.28	24	24.72	MHz
Fpll	Internal PLL multiplier clock frequency		24	96	96	MHz
Fsys	System clock frequency (VDD>=3V)		0.1	12	48	MHz
	System clock frequency (VDD<3V)		0.1	12	24	MHz
Tpor	Power on reset delay		8	11	15	mS
Trst	External input valid reset signal width		2			uS
Trdl	Thermal reset delay		20	30	50	uS
Twdc	Watchdog overflow cycle / timing cycle calculation formula		131072 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	USB auto suspended time in USB host mode		2	3	4	mS
	USB auto suspended time in USB device mode		4	5	6	mS
Twaksb	Time to wake up from standby/normal sleep		0.5	0.8	3	uS
Twakdp	Time to wake up from power down/deep sleep		120	200	1000	uS

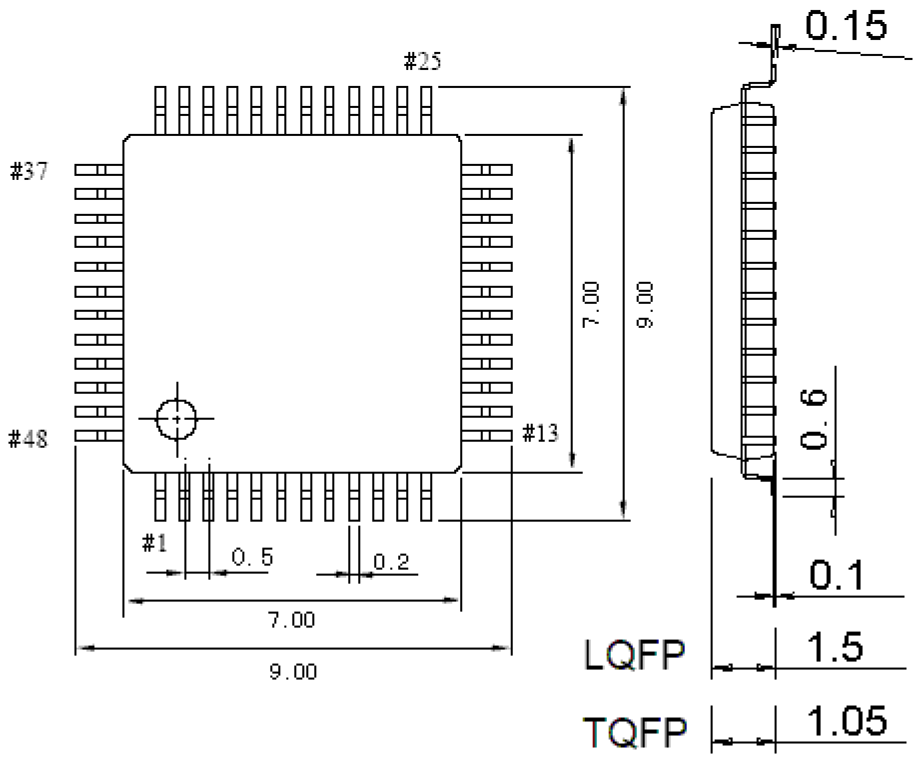
19.5 Other parameters

Test conditions: TA=25°C, VDD=4.5V～5.5V or VDD=V33=3.0V～3.6V

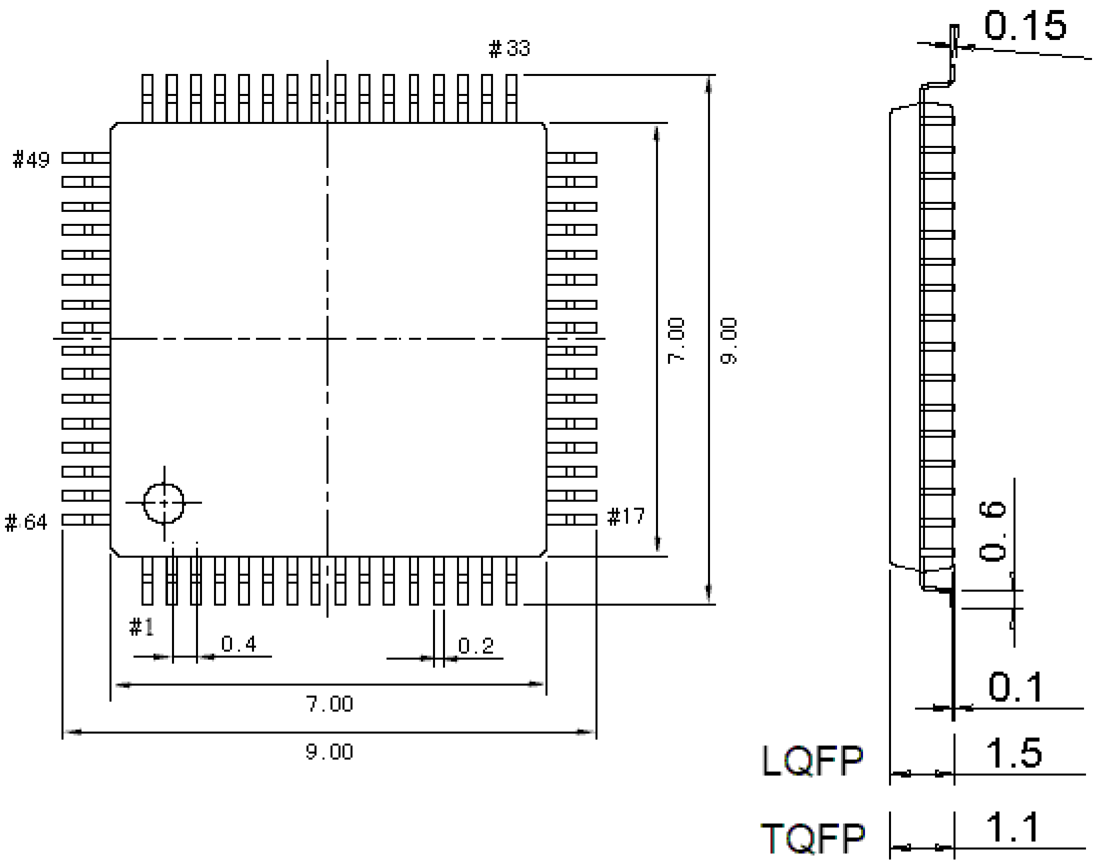
Symbol	Parameter description	Min.	Typ.	Max.	Unit
TERPG	Time to perform single erase/ program operation on Flash-ROM/EEPROM	2	5	8	mS
NEPCE	Erase/program cycle endurance	10K	Not guaranteed 100K		times
TDR	Data hold capability of Flash-ROM/EEPROM	10			years
VESD	ESD voltage on I/O pins	4K	Not guaranteed 8K		V

20. Package information

20.1 LQFP48-7*7



20.2 LQFP64-7*7



21. Revision history

Revision	Date	Description
V0.95	October 25, 2019	First release
V1.0	December 20, 2019	Official release
V1.1	January 15, 2020	CH557 in LQFP48 package deleted.
V1.2	May 19, 2020	Parameters modified in Section 19.2.
V1.3	March 15, 2021	Description added in Table 10.2.5 that the USB 1.5K pull-up must be replaced with the 7.5K pull-up during sleep
V1.4	October 13, 2021	Exchange bI2CS_IE_TRAN and bI2CS_IE_RECV. The system clock frequency does not exceed 48MHz. Note that no external resistors are connected in series with USB pins.
V1.5	December 28, 2021	Access of MASK_I2CM_CMD corrected to be RW.
V1.6	January 6, 2022	Description about bit reset optimized: Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.