CH7034B HDTV/VGA/LVDS Encoder

FEATURES

- Supports multiple output display formats – including Component YPrPb(HDTV), LVDS and analog RGB (VGA)
- Three 10-bit high speed DACs
- HDTV output support up to 1080p
- Analog RGB (VGA) support up to 1920x1080 resolution
- Single channel LVDS 18-bit transmitter supports input resolution up to 1366x768
- Support scaled and bypassed video streams output from VGA/HDTV and LVDS interfaces simultaneously
- Supports panel protection, power sequencing and backlight on/off. PWM is available for controlling LCD brightness
- TV/Monitor connection detect capability. DACs can be switched off through programming internal registers
- On-chip SDRAM frame buffer to support frame rate conversion.
- Programmable adaptive de-flickering filter
- Supports 8/12/16/18/24-bit parallel interface inputs for either RGB format or YCbCr format (ITU-R 656 or ITU-R 601). 80/86 MPU interface and DE only mode are also supported.
- Wide range of input resolutions support for up to 1366x768 (i.e. 640x480 720x480, 720x576, 800x600, 1024x600, 1024x768, 1280x800, and etc.)
- Image display rotation support at 90/180/270 degree or flipped in horizontal/vertical position
- Pixel-level color enhancement for brightness, contrast, hue and saturation adjustment for HDTV
- Horizontal/vertical position adjusted through serial port programming
- Pixel clock input frequency support for up to 165 MHz
- Flexible crystal or oscillator clock input frequency (2.3MHz – 64MHz)
- IO Supply Voltages from 1.2V to 3.3V and SPC/SPD Supply Voltages from 1.8V to 3.3V.
- Programmable power management
- Device fully programmable through serial port or can automatically load firmware from Chrontel Boot ROM (CH9904)
- Offered in a 88-pin QFN package

GENERAL DESCRIPTIONS

Chrontel CH7034B is specifically designed for a portable system that requires connections to LCD display, High Definition Television (HDTV) or RGB (VGA) monitor. With its advanced video encoder, flexible scaling engine and easy-to-configure video interface, the CH7034B satisfies manufactures' product display requirements and reduces their costs of development and time-to-market.

The CH7034B provides analog RGB and YPrPb outputs that allow a system to display high definition media content to HDTV/RGB monitors. The device is compliant with EIA770-3 and SMPTE 274M/293M /296M standards and supports HDTV resolution up to 1080p. The 3 high-performance, 10-bit DACs can be used for either HDTV display or VGA output. The CH7034B has the ability to generate composite syncs if required by the RGB monitor.

To support portable computer with LCD display, the CH7034B has incorporated an one-channel, 18-bit output LVDS transmitter. On-chip dithering function is available to convert 24-bit color to 18-bit color LCD panels. Two popular LVDS standards, the OpenLDI and the VESA SPWG are supported by the CH7034B LVDS driver. The preferred standard and its display timing can be configured through devices' registers when system is powered on.

The CH7034B is equipped with panel protection mechanism to switch off the LCD instantly if input data is missing or unstable. The panel on/off sequences and backlight control can be configured through programming internal registers. In addition, a built-in PWM function can be used to achieve digital dimming for LCD panel.

The CH7034B converts a wide range of input formats to HDTV/VGA outputs and LVDS display. RGB data format such as 16-bit 5:6:5, 18-bit 6:6:6 or 24-bit 8:8:8 enters through the device's 24-bit bus. In YCrCb format, either 24-bit 4:4:4 data or 16-bit 4:2:2 is supported by the CH7034B's color space converter. The device's video capture block also has an option to support 80/86 MPU interface. The input video signal can be either interlaced or non-interlaced data formats.

With its embedded high speed SDRAM, the CH7034B can help manufactures design their products to achieve simultaneous LVDS and HDTV/VGA display. Thanks to the sophisticated scaler, the input LCD data with low resolution or reduced-frame rate can be covert to high

APPLICATION

- Mobile Internet Devices
- Smartbook / Electronic Book
- Tablet Device
- Portable DVD Players
- Docking Station

quality HDTV or VGA display without extra loading on the processor. Also, by taking the advantage of the framebuffer, the scaler can perform other image manipulations including resizing and rotation.

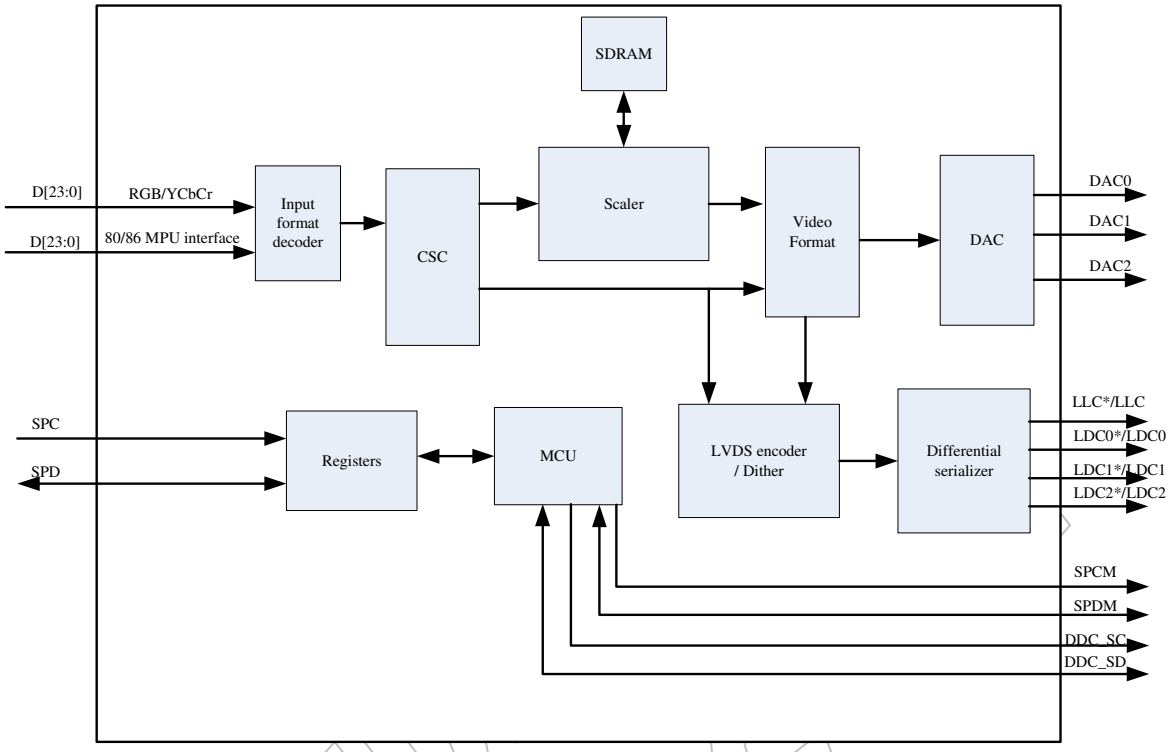

Figure 1: Functional Block Diagram

1.0 PIN ASSIGNMENT

1.1 Package Diagram

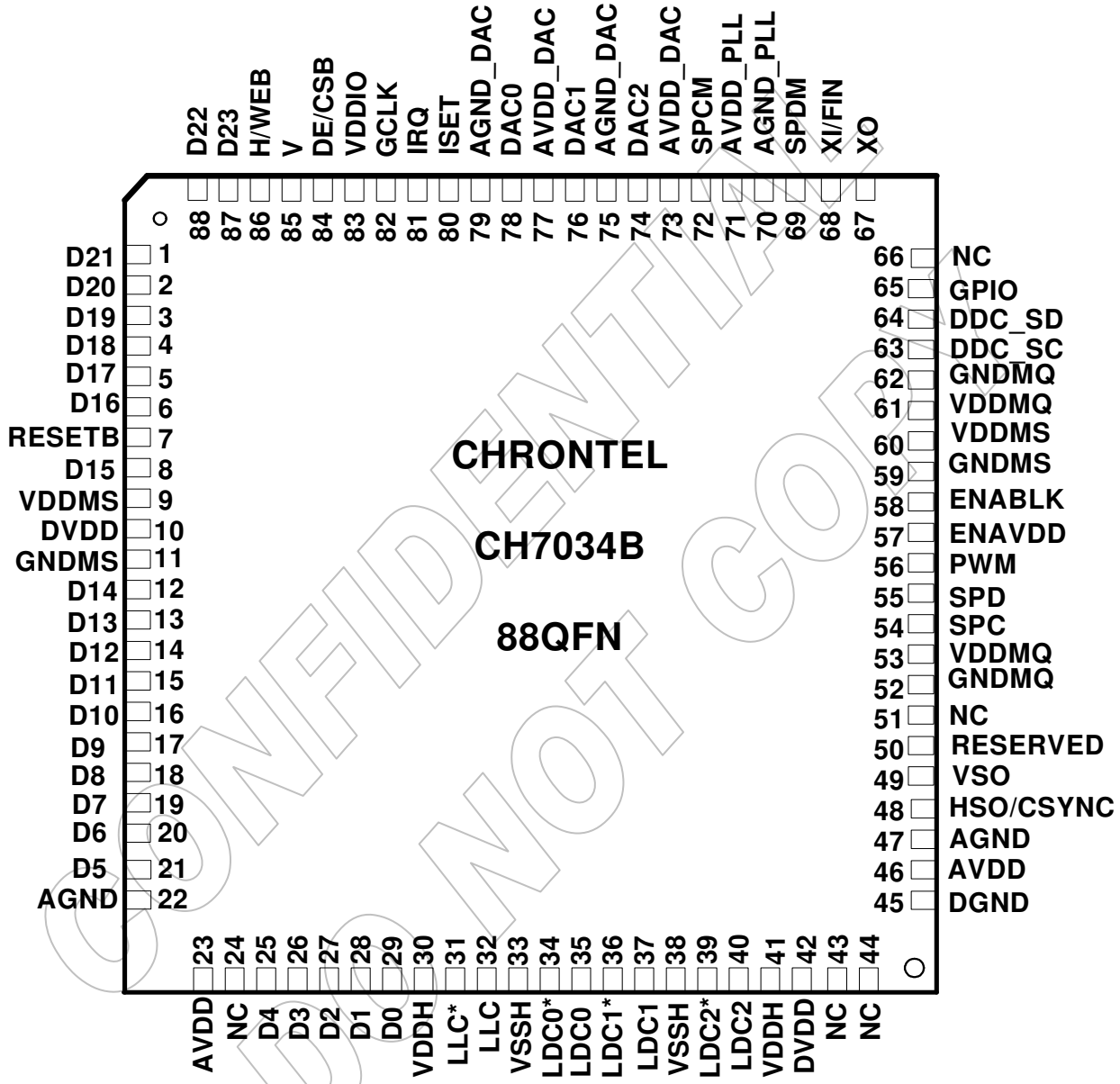

Figure 2: 88 pin QFN Package (Top View)

1.2 Pin Description

Table 1: Pin Name Descriptions (QFN88 pin Package)

Pin #	Type	Symbol	Description
1~6,8, 12~21, 25~29, 87~88,	In	D[23:0]	**Data Input** These pins accept 24 data input lines from a digital video port of a graphics controller. The swing is defined by VDDIO. All the unused data input pins should be pulled low with 10 KΩ resistors or shorted to Ground directly.
7	In	RESETB	**Reset Input** When this pin is low, the device is held in the power-on reset status. When this pin is high, reset is controlled through the serial port.
31,32	Out	LLC*,LLC[1]	**LVDS Clock Outputs** These pins provide the differential clock output for the LVDS.
34,35	Out	LDC0*,LDC0[1]	**LVDS Data Channel 0 Outputs** These pins provide the LVDS differential outputs for data channel 0.
36,37	Out	LDC1*,LDC1[1]	**LVDS Data Channel 1 Outputs** These pins provide the LVDS differential outputs for data channel 1.
39,40	Out	LDC2*,LDC2[1]	**LVDS Data Channel 2 Outputs** These pins provide the LVDS differential outputs for data channel 2.
48	Out	HSO/CSYNC	**Horizontal sync signal output** The amplitude of this pin is from 0 to AVDD. It also functions as a Composite sync output
49	Out	VSO	**Vertical sync signal output** The amplitude of this pin is from 0 to AVDD.
50	N/A	RESERVED	**Reserved** This pin should be left open or pulled low with a 10 KΩ resistor in the application.
54	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required.
55	In/out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required.
56	Out	PWM	**Backlight brightness adjustment**
57	Out	ENAVDD	**Panel Power Enable** Enable LCD panel VDD
58	Out	ENABLK	**Back Light Enable** Enable back light of LCD panel
63	Out	DDC_SC	**Routed Serial Port Clock Output to DDC** This pin functions as the clock bus of the serial port to DDC receiver. This pin will require a pull-up resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused.
64	In/out	DDC_SD	**Routed Serial Port Data to DDC** This pin functions as the bi-directional data pin of the serial port to DDC receiver. This pin will require a pull-up resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused
65	In/ out	GPIO	**General Purpose Input Output**
67	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
68	In	XI/FIN	**Crystal Input / External Reference Input** A parallel resonance crystal should be attached between this pin and

			XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
69	In/Out	SPDM	**Routed Serial Port Data to CH9904 BOOT ROM** This pin functions as the bi-directional data pin of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10K to ground if unused.
72	Out	SPCM	**Routed Serial Port Clock Output to CH9904 BOOT ROM** This pin functions as the clock bus of the serial port to CH9904 BOOT ROM. This pin will require a pull-up 6.8 KΩ resistor to the desired voltage level. A pull-low resistor 10 KΩ to ground if unused.
74	Out	DAC2	**YpbPr or Analog RGB output** Full swing is up to 1.3V
76	Out	DAC1	**YpbPr or Analog RGB output** Full swing is up to 1.3V
78	Out	DAC0	**YpbPr or Analog RGB output** Full swing is up to 1.3V
80	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 1.2 KΩ, 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
81	Output	IRQ	**Programmed Interrupt output.**
82	In	GCLK	**External Clock Inputs** The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data.
84	In	DE/CSB	**Data Input Indicator** When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also a CSB signal input of CPU interface The amplitude will be 0 to VDDIO.
85	In/Out	V	**Vertical Sync Input/Output** When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
86	In/Out	H/WEB	**Horizontal Sync Input / Output** When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU interface.
24,43,44, 51,65, 66	N/A	NC	**Not Connect** These pins should be left open.
9,60	Power	VDDMS	**SDRAM Power Supply (3.3V)**
59,11	Power	GNDMS	**SDRAM Ground**
10,42	Power	DVDD	**Digital Power Supply (1.8V)**
45	Power	DGND	**Digital Ground**
23,46	Power	AVDD	**Analog Power Supply (2.5V-3.3V)**
22,47	Power	AGND	**Analog Ground**
30,41	Power	VDDH	**LVDS Power Supply (3.3V)**
33,38	Power	VSSH	**LVDS Ground**

53,61	Power	VDDMQ	**SDRAM output buffer Power Supply (3.3V)**
52,62	Power	GNDMQ	**SDRAM output buffer Ground**
71	Power	AVDD_PLL	**PLL Power Supply (1.8V)**
70	Power	AGND_PLL	**PLL Ground**
77,73	Power	AVDD_DAC	**DAC Power Supply (2.5V-3.3V)**
75,79	Power	AGND_DAC	**DAC Ground**
83	Power	VDDIO	**IO Power Supply (1.2-3.3V)**

Notes:

1. The clock/data order and the polarity of the 4 output channels are programmable.

2.0 PACKAGE DIMENSIONS

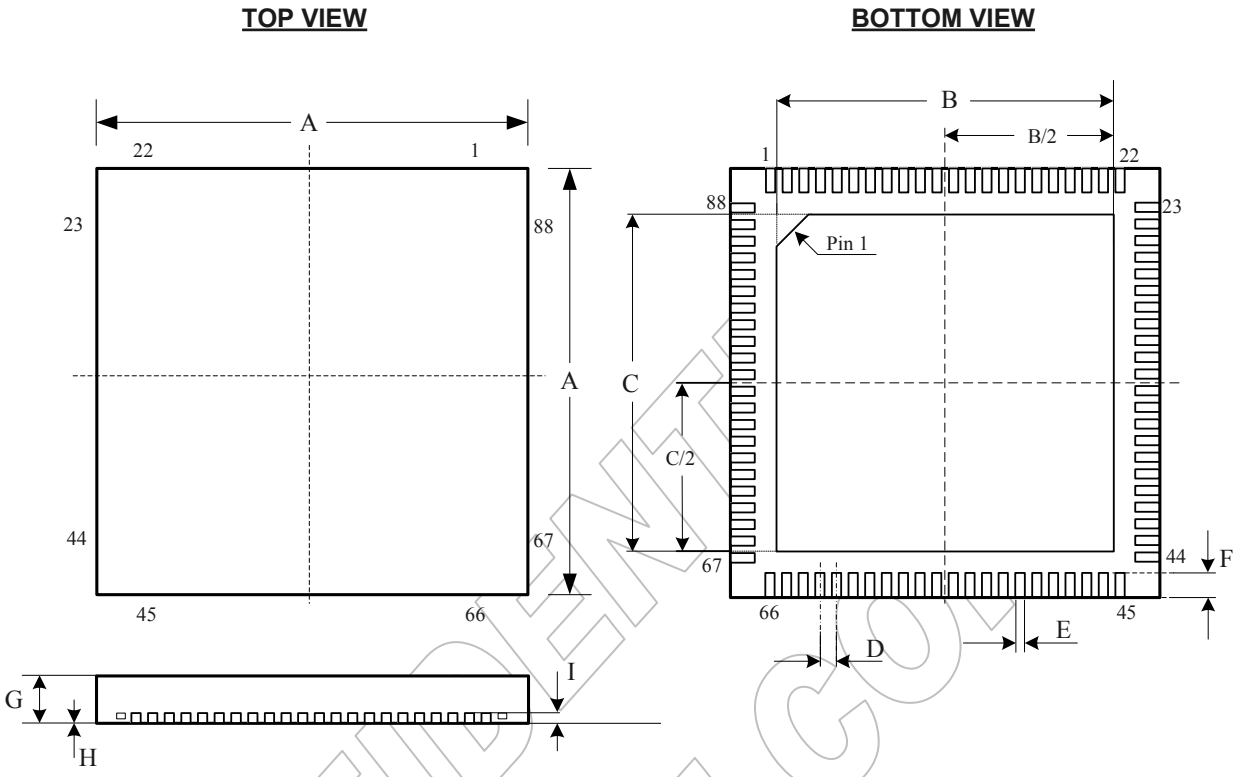

Figure 3: 88 Pin QFN Package (10 x 10 mm)

Table of Dimensions

No. of Leads		SYMBOL								
88 (10 X 10 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	9.90	6.60	6.60	0.4	0.15	0.35	0.8	0	0.20
	MAX	10.10	6.90	6.90		0.25	0.60	0.9	0.05	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION

Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity
CH7034B-BF	88QFN, Lead-free	Commercial : -20 to 70°C	168 pcs/Tray
CH7034B-BFI	88QFN, Lead-free	Industrial : -40 to 85°C	168 pcs/Tray

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