

CH7101A HDMI to VGA Converter

FEATURES

- HDMI Receiver compliant with HDMI 1.4 specification
- Analog RGB output for VGA with Triple 9-bit DAC up to 200MHz pixel rate. Sync signals can be provided in separated or composite manner. Support VESA and CEA timing standards up to WUXGA 1920x1200@60Hz and 1920x1080@60Hz
- On-chip Audio encoder which support 2 channel IIS/ S/PDIF audio output
- VGA output is compliant with VESA VSIS v1r2 specification
- MCU embedded to handle the control logic
- Support device boot up by automatically loading firmware from on-chip flash Boot ROM
- Integrated EDID Buffer
- Crystal Free architecture
- VGA connection detection supported
- HDMI input detection supported
- Support Auto Power Saving mode and low stand-by current
- Support YCC to RGB conversion in ITU-R BT.601 and 709 color space
- IIC slave interface and HDMI DDC interface are available for debug and firmware update.
- Low power architecture
- RoHS compliant and Halogen free package
- Offered in 40-Pin QFN package (5 x 5 mm)

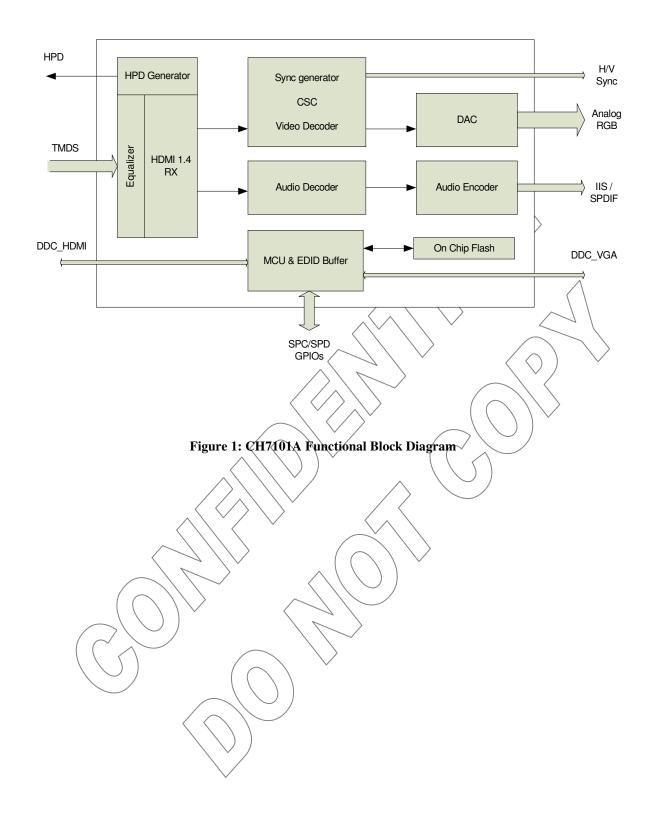
APPLICATION

- Notbook/Ultrabook
- Tablet Device
- Handheld/Portable Device
- Digital Video Systems
- HDMI to VGA Adapter/Docking Station
- Car Entertainment Device

GENERAL DESCRIPTION

Chrontel's CH7101A is a low-cost, low-power semiconductor device that consists of HDMI receiver, three separate 9-bit video Digital-to-Analog Converters (DACs) and audio encoder, which can convert HDMI signals into VGA outputs at a maximum conversion rate of 200 MHz with IIS or SPDIF audio output.

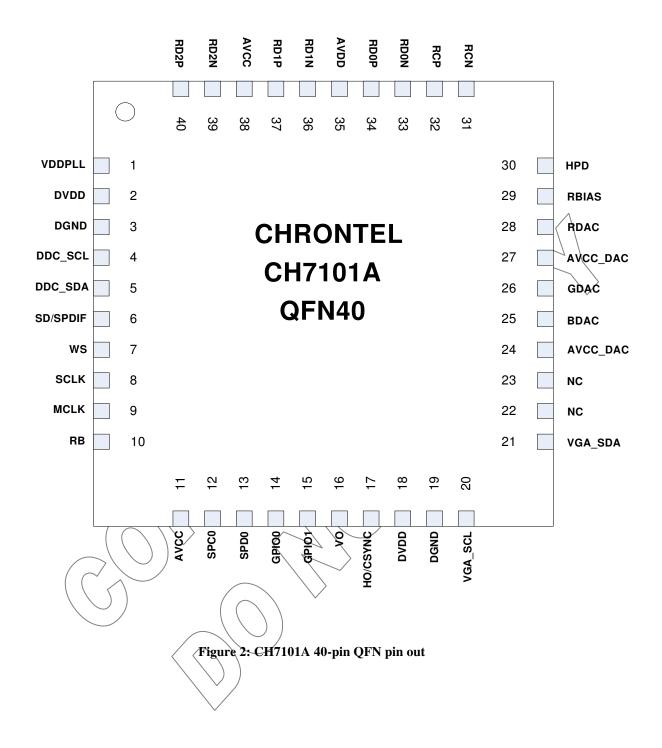
The HDMI Receiver integrated is compliant with HDMI 1.4b. The DACs are based on current source architecture. And the VGA output meet VESA VSIS v1r2 clock jitter target. With sophisticated MCU and the Boot ROM embedded, CH7101A support auto-boot and EDID buffer. Take the advantage of Firmware auto loaded from the embedded Boot ROM, CH7101A can support HDMI input detection, DAC connection detection and determine to enter into Power saving mode automatically.



2 209-1000-048 Rev 0.6 2012-11-23

1.0 PIN-OUT

1.1 Package Diagram



209-1000-048 Rev 0.6 2012-11-23 3

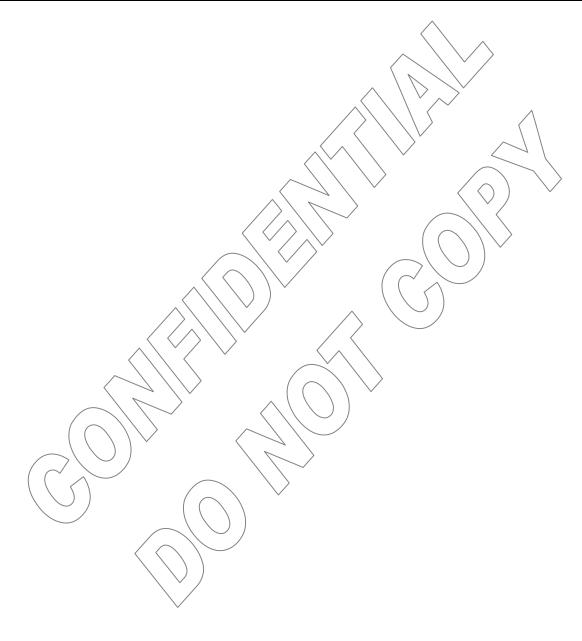
1.2 Pin Description

Table 1: Pin Name Descriptions

In DDC_SCL Serial Port Clock to HDMI/DVI Transmitter This pin functions as the clock bus of the serial port to HDMI or DVI DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level.	Pin#	Type	Symbol	Description			
DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level.	4	In	DDC_SCL	Serial Port Clock to HDMI/DVI Transmitter			
desired voltage level.				This pin functions as the clock bus of the serial port to HDMI or DVI			
In/out DDC_SDA Serial Port Data to HDMI/DV1 Transmitter This pin functions as the data bus of the serial port to HDMI or DV1 DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level.							
This pin functions as the data bus of the serial port to HDMI or DVI DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level. 6 Out SD/SPDIF 12S Serial Data or SPDIF Output 7 Out WS 12S Word Select 8 Out SCLK 12S Continuous Serial Clock 9 Out MCLK 12S System Clock 10 In RB Chip Reset Low to 0V for reset. Typical High level is 3.3V 12 In SPCO Serial Port Clock Input This pin functions as the clock pin of the serial port-External pull-up 6.8 kΩ resister is required 13 In/out SPDO Serial Port Data Input/Output This pin functions as the bi-directional data pin of the serial port External pull-up 6.8 kΩ resister is required 14.15 In/Out GPIO General Purpose Input/Output The amplitude of this pin is from 0 to AVCC It also Vancious as a Composite sync output The amplitude of this pin is from 0 to AVCC It also Vancious as a Composite sync output 12 In/Out VGA SCL Serial Port Clock Output to VGA Receiver The pin should be compected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 20 Out VGA SCL Serial Port Clock Output to VGA Receiver The pin should be compected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 21 In/Out VGA SDA Serial Port Data (a VGA) Receiver The pin should be compected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 22 In X0 Crystal Input A parallel resonance crystal should be attached between this pin and X1. If an external CMOS clock is injected to X1, XO should be left open. 23 Out GDAC VGA Green Component DAC output This pin sets the DAC current. A10 kΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD III IMIN Receiver Hot Plug output							
DDC transmitter. This pin requires a pull-up 47 kΩ resistor to the desired voltage level.	5	In/out	DDC_SDA				
desired voltage level.				This pin functions as the data bus of the serial port to HDMI or DVI			
Out SD/SPDIF 12S Serial Data or SPDIF Output				DDC transmitter. This pin requires a pull-up 4/ k\O2 resistor to the			
7	6	Out	SD/SPDIF				
SCLK I2S Continuous Serial Clock							
Out MCLK I2S System Clock							
10							
Low to 0V for reset. Typical High level is 3.3V	9	Out	MCLK				
In SPC0 Serial Port Clock Input This pin functions, as the clock pin of the serial port-External pull-up 6.8 KΩ resister is required Serial Port Data Input / Output	10	In	RB				
This pin functions as the clock pin of the serial port-External pull-up 6.8 KΩ resister is required Serial Port Data Input / Output This pin functions as the bi-directional data pin of the serial port External pull-up 6.8 KΩ resister is required 14,15 In/Out GPIO Generál Purpose Input/Output 16 Out VO Vertical Sync Signal Output The amplitude of this pin is from 0 to AVCC It also functions as a Confiposite sync output Serial Port Clock Output to VGA Receiver The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 21 In/Out VGA_SDA Serial Port Data to VGA Receiver The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 22 In XI Crystal Imput A parallel resonance crystal should be attached between this pin and XO. Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. 25 Out BDAC VGA Red Component DAC output VGA Green Component DAC output VGA Green Component DAC output This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output HDMI Receiver Hot Plug output				Low to 0V for reset. Typical High level is 3.3V			
13 In/out SPD0 Serial Port Data Input / Output	12	In	SPC0				
In/out SPD0 Serial Port Data Input / Output							
This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required 14,15 In/Out GPIO General Purpose Input/Output 16 Out VO Vertical Sync Signal Output The amplitude of this pin is from 0 to AVCC 17 Out HO/CSYNC Horizontal Sync Signal Output The amplitude of this pin is from 0 to AVCC It also functions as a Composite sync output 20 Out VGA SCL Serial Port Clock Output to VGA Receiver The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 21 In/Out VGA SDA Serial Port Data (o VGA) Receiver The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 22 In XI Crystal Input A parallel resonance crystal should be attached between this pin and XO. 23 Out XO Crystal Output A-parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. 25 Out BDAC VGA Blue Component DAC output 26 Out GDAC VGA Rec Component DAC output 27 VGA Rec Component DAC output 28 Out RDAC VGA Red Component DAC output 29 In RBIAS Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output							
External pull-up 6.8 KΩ resister is required	13	In/out	SPD0				
14,15 In/Out GPIO General Purpose Input/Output 16 Out VO Vertical Sync Signal Output The amplitude of this pin is from 0 to AVCC 17 Out HO/CSYNC Horizontal Sync Signal Output The amplitude of this pin is from 0 to AVCC 18 In/Out VGA SCL Serial Port Clock Output to VGA Receiver The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ-resistor) to the desired voltage level 21 In/Out VGA SDA STA Serial Port Data to VGA Receiver The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 22 In Crystal Input, A parallel resonance crystal should be attached between this pin and XO. 23 Out XO Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. 25 Out BDAC VGA Blue Component DAC output 26 Out GDAC VGA Green Component DAC output 27 VGA Blue Component DAC output 28 Out RDAC VGA Receiver The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 28 Out BDAC Crystal Output This pin sets the DAC output Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output							
16 Out VO Vertical Sync Signal Output The amplitude of this pin is from 0 to AVCC It also functions as a Composite sync output 20 Out VGA SCI Serial Port Clock Output to VGA Receiver The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 21 In/Out VGA SDA Serial Port Data to VGA Receiver The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 22 In XI Crystal Input A parallel resonance crystal should be attached between this pin and XO. 23 Out XO Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. 25 Out BDAC VGA Blue Component DAC output 26 Out GDAC VGA Red Component DAC output 27 VGA Red Component DAC output 28 Out RDAC VGA Red Component DAC output Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 27 HDMI Receiver Hot Plug output 18 J1,32,33, In RDJ2:0]P/N HDMI TMDS Input		7 10	~~~				
The amplitude of this pin is from 0 to AVCC	14,15	In/Out					
17 Out HO/CSYNC Horizontal Sync Signal Output The amplitude of this pin is from 0 to AVCC It also functions as a Composite sync output 20 Out VGA SCL Serial Port Clock Output to VGA Receiver The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 21 In/Out VGA SDA Serial Port Data to VGA Receiver The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 22 In XI Crystal Input A parallel resonance crystal should be attached between this pin and XO. 23 Out XO Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. 25 Out BDAC VGA Blue Component DAC output 26 Out GDAC VGA Red Component DAC output 27 VGA Red Component DAC output 28 Out RDAC VGA Red Component DAC output 29 In RBIAS Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input	16	Out	VO				
The amplitude of this pin is from 0 to AVCC It also functions as a Composite sync output 20 Out VGA SCL Serial Port Clock Output to VGA Receiver The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 21 In/Out VGA SDA Serial Port Data to VGA Receiver The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level 22 In XI Crystal Input A parallel resonance crystal should be attached between this pin and XO. 23 Out XO Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. 25 Out BDAC VGA Blue Component DAC output 26 Out GDAC VGA Red Component DAC output 27 VGA Red Component DAC output 28 Out RDAC VGA Red Component DAC output 29 In RBIAS Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input				The amplitude of this pin is from 0 to AVCC			
Serial Port Clock Output to VGA Receiver	17	Out	HO/CSYNC				
Out VGA_SCL Serial Port Clock Output to VGA Receiver The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level			\wedge	The amplitude of this pin is from 0 to AVCC			
The pin should be connected to clock signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level Serial Port Data to VGA Receiver The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level In XI Crystal Input A parallel resonance crystal should be attached between this pin and XO. Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. VGA Blue Component DAC output VGA Green Component DAC output VGA Red Component DAC output This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces Out HPD HDMI Receiver Hot Plug output HDMI TMDS Input							
Product Pro	20	Out	VGA_SCL V				
In/Out VGA SDA Serial Port Data to VGA Receiver The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level							
The pin should be connected to data signal of VGA DDC. This pin requires a pull-up 10 kΩ resistor to the desired voltage level Crystal Input A parallel resonance crystal should be attached between this pin and XO. Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. Dut BDAC VGA Blue Component DAC output VGA Red Component DAC output RDAC VGA Red Component DAC output This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces HDMI Receiver Hot Plug output HDMI TMDS Input This pin sty	21	In/Out	VCA CBA				
Trequires a pull-up 10 kΩ resistor to the desired voltage level	21	In/Out	VGA_SDA				
In XI Crystal Input A parallel resonance crystal should be attached between this pin and XO.							
A parallel resonance crystal should be attached between this pin and XO. Crystal Output A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. Dut BDAC VGA Blue Component DAC output VGA Green Component DAC output VGA Red Component DAC output PGA Red Component DAC output RDAC VGA Red Component DAC output Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces HDMI Receiver Hot Plug output HDMI TMDS Input HDMI TMDS Input	22	In (W				
XO. XO. Crystal Output	22	\ \					
A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. 25 Out BDAC VGA Blue Component DAC output 26 Out GDAC VGA Green Component DAC output 28 Out RDAC VGA Red Component DAC output 29 In RBIAS Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input							
A parallel resonance crystal should be attached between this pin and XI. If an external CMOS clock is injected to XI, XO should be left open. 25 Out BDAC VGA Blue Component DAC output 26 Out GDAC VGA Green Component DAC output 28 Out RDAC VGA Red Component DAC output 29 In RBIAS Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input	23	Out	XO /	Crystal Output			
Open.							
25 Out BDAC VGA Blue Component DAC output 26 Out GDAC VGA Green Component DAC output 28 Out RDAC VGA Red Component DAC output 29 In RBIAS Current Set Resistor Input				XI. If an external CMOS clock is injected to XI, XO should be left			
26 Out GDAC VGA Green Component DAC output 28 Out RDAC VGA Red Component DAC output 29 In RBIAS Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input				1 /			
28 Out RDAC VGA Red Component DAC output 29 In RBIAS Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input	25	Out	BDAC	VGA Blue Component DAC output			
29 In RBIAS Current Set Resistor Input This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input	26	Out	GDAC \	VGA Green Component DAC output			
This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input	28	Out	RDAC	VGA Red Component DAC output			
This pin sets the DAC current. A10 KΩ, 1% tolerance resistor should be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input	29	In	RBIAS	Current Set Resistor Input			
be connected between this pin and AVSS using short and wide traces 30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input							
30 Out HPD HDMI Receiver Hot Plug output 31,32,33, In RD[2:0]P/N HDMI TMDS Input							
	30	Out	HPD				
	31,32,33,	In	RD[2:0]P/N	HDMI TMDS Input			
	34,36,37,			HDMI differential clock and data input pairs			

4 209-1000-048 Rev 0.6 2012-11-23

39,40			
1	Power	VDDPLL	PLL Power Supply (1.2V)
2,18	Power	DVDD	Digital IO Power Supply (1.2V)
3,19	Power	DGND	Digital Ground
11, 38	Power	AVCC	Analog Power Supply (3.3V)
24,27	Power	AVCC_DAC	Analog DAC Power Supply (3.3V)
35	Power	AVDD	HDMI Receiver Analog Power Supply (1.2V)
Pad	Power	GND	Power Supply Ground



209-1000-048 Rev 0.6 2012-11-23 5

2.0 PACKAGE DIMENSION

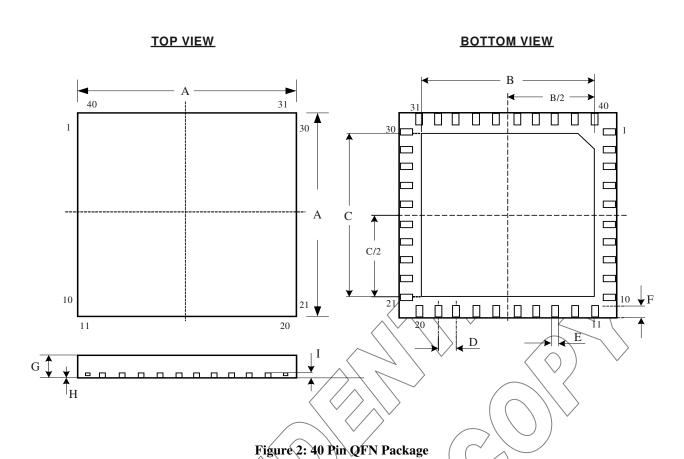


Table 2: Table of Dimensions

No. of Leads			SYMBOL							
40 (5 X	5 mm)	A	B	C	D	E	> F	G	Н	I
Milli-	MIN	4.90	3.20	3.20	0.4	0.15	0.35	0.7	0	0.20
meters	MAX	5.10	3.75	3.75	\ U-4\	0.25	0.55	0.8	0.05	0.203

Notes:

Conforms to JEDEC standard JESD-30 MO-220.

6 209-1000-048 Rev 0.6 2012-11-23

Disclaimer

This document provides technical information for the user. Chrontel reserves the right to make changes at any time without notice to improve and supply the best possible product and is not responsible and does not assume any liability for misapplication or use outside the limits specified in this document. We provide no warranty for the use of our products and assume no liability for errors contained in this document. The customer should make sure that they have the most recent data sheet version. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Chrontel, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Chrontel PRODUCTS ARE NOT AUTHORIZED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS OR NUCLEAR FACILITY APPLICATIONS WITHOUT THE SPECIFIC WRITTEN CONSENT OF Chrontel. Life support systems are those intended to support or sustain life and whose failure to perform when used as directed can reasonably expect to result in personal injury or death.

ORDERING INFORMATION						
Part Number	Package Type	Operating Temperature Range	Minimum Order Quantity			
CH7101A-BF	40 QFN, Lead-free	Commercial: 20 to 70°C	490/Tray			
CH7101A-BFI	40 QFN, Lead-free	Industrial: 40 to 85°C	490(Tray			

Chrontel

Chrontel International Limited

129 Front Street, 5th floor, Hamilton, Bermuda HM12

www.chrontel.com E-mail: sales@chrontel.com

@2012 Chrontel - All Rights Reserved.

209-1000-048 Rev 0.6 2012-11-23 7