CH7308B SDVO[1] LVDS Transmitter

Features

- Single/Dual LVDS Transmitter up to 165Mpixels/s
- Support resolutions up to 1600x1200 (1920x1200 with reduced blanking)
- LVDS low jitter PLL accepts spread spectrum input
- LVDS 18-bit and 24-bit outputs
- 2D dither engine
- Panel protection and power sequencing
- High-speed SDVO[1] serial (1G~2Gbps) AC-coupled differential RGB inputs
- Low voltage interface support to graphics device
- Programmable power management
- Fully programmable through serial port
- Configuration through OpCodes[1]
- Complete Windows driver support
- Boundary scan support
- Offered in a 64-pin LQFP package

[1]Intel Proprietary

General Description

The CH7308B is a display controller device, which accepts digital graphics input signals, upscales, encodes, and transmits data through an LVDS transmitter to a LCD panel. This device accepts one channel of RGB data over three pairs of serial data ports.

The LVDS Transmitter includes a low jitter PLL to generate a high frequency serialized clock and all circuitry required to upscale, encode, serialize and transmit data. The CH7308B supports a maximum pixel rate of 165MP/s.

The LVDS transmitter includes a panel fitting up-scaler and a programmable dither function to support 18-bit LCD panels. Data is encoded into commonly used formats, including those specified in the OpenLDI and SPWG specifications. Serialized data is outputted on three to eight differential channels.

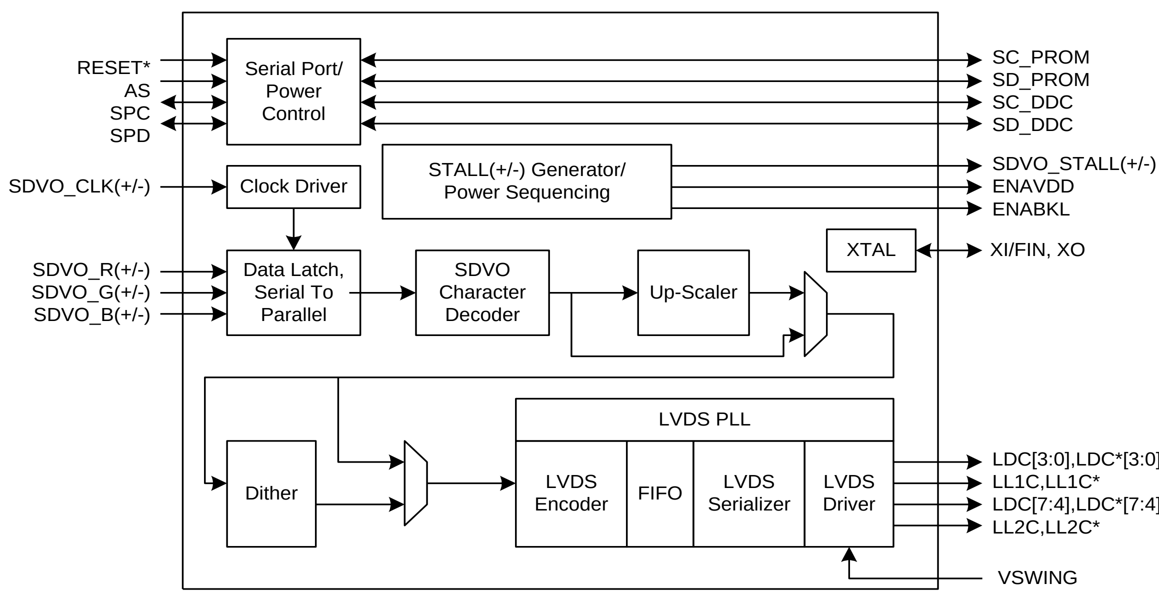

Figure 1: Functional Block Diagram

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1.0 Pin Assignment

1.1 Package Diagram

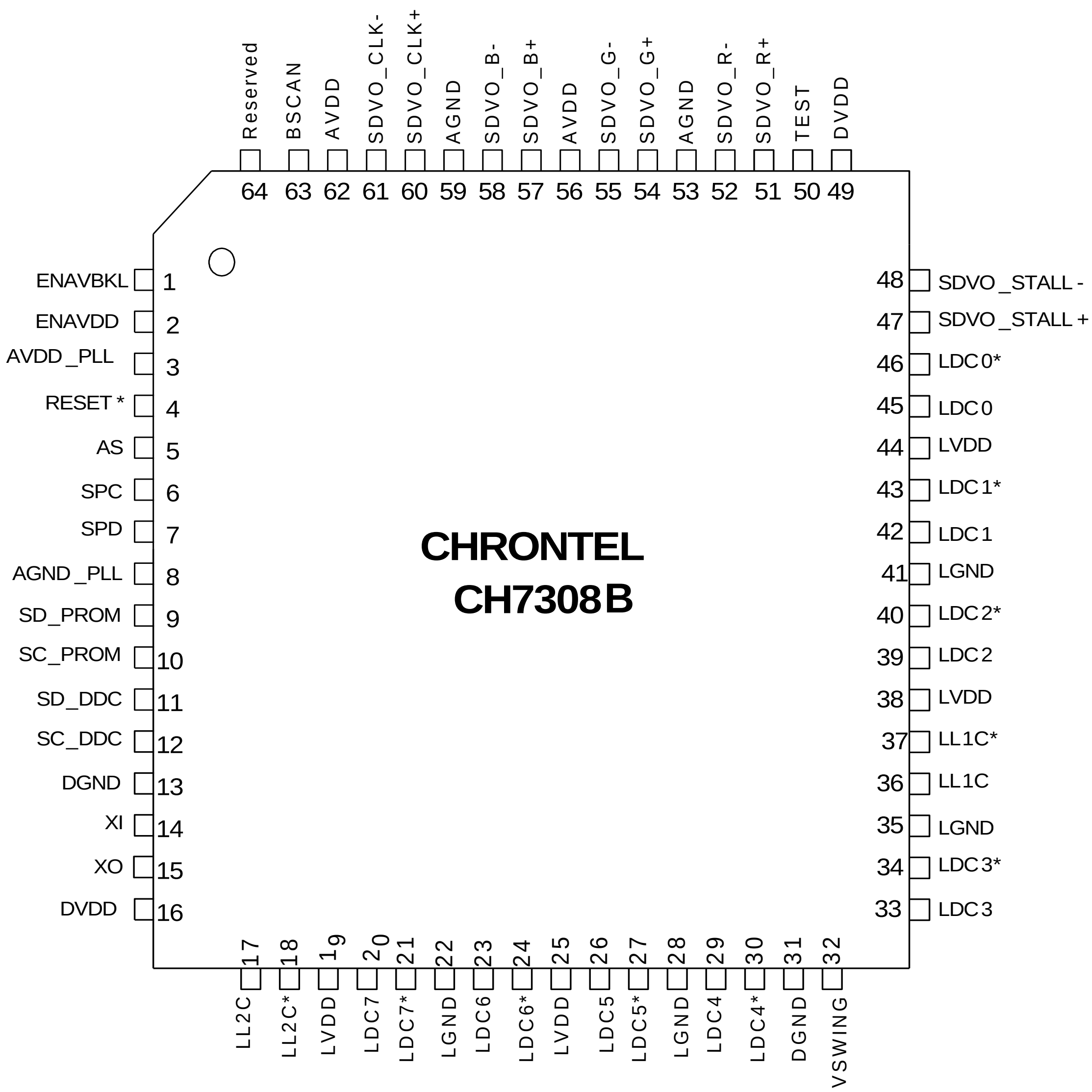

Figure 2: 64 Pin LQFP Pin Out (Top View)

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
4	In	RESET*	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port interface.
5	In	AS	**Address Select (Internal pull-up)** This pin determines the serial port address of the device (0,1,1,1,0,0,AS*,0).
6	In/Out	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port interface and operates with from 0 to 2.5V. This pin requires an external 4kΩ - 9kΩ pull up resistor to 2.5V
7	In/Out	SPD	**Serial Port Data Input/Output** This pin functions as the bi-directional data pin of the serial port interface and operates with inputs from 0 to 2.5V. Outputs are driven from 0 to 2.5V. This pin requires an external 4kΩ - 9kΩ pull up resistor to 2.5V.
9	In/Out	SD_PROM	**Routed Data Output to PROM** This pin functions as the bi-directional data pin of the serial port interface for the external 5V serial EEPROM used for ADD2 card designs. This pin requires an external 5.6K pull-up resistor to the desired high state voltage. Leave open if unused.
10	In/Out	SC_PROM	**Routed Clock Output to PROM** This pin functions as the clock bus of the serial port interface for the external 5V serial EEPROM used for ADD2 card designs. This pin requires an external 5.6K pull-up resistor to the desired high state voltage. Leave open if unused.
11	In/Out	SD_DDC	**Routed Serial Port Data Output to DDC** This pin functions as the bi-directional data pin of the serial port to the DDC of the receiver. This pin requires an external 4–9kΩ pull-up resistor to the desired high state voltage. Leave open if unused.
12	In/Out	SC_DDC	**Routed Serial Port Clock Output to DDC** This pin functions as the clock bus of the serial port to the DDC of the receiver. This pin requires an external 4–9kΩ pull-up resistor to the desired high state voltage. Leave open if unused.
2	Out	ENAVDD	**Panel Power Enable** Enable LCD panel VDD (2.5V).
1	Out	ENABKL	**Backlight Enable** Enable backlight of LCD panel (2.5V).
63	In	BSCAN	**BSCAN (internal pull low**) This pin should be left open or be pulled low with 10kΩ resistor.
50	Out	TEST	**TEST** Internal test pin to monitor the state of the ENEXBUF (External Buffer Enable) signal. See TB49 for details. If the ENEXBUF signal does not need to be monitored, this pin may be left open.
64	In	Reserved	**Reserved** This pin should be left open

Pin#	Type	Symbol	Description
51, 52, 54, 55, 57, 58	In	SDVO_R+/- SDVO_G+/- SDVO_B+/-	**SDVO Data Channel Inputs** These pins accept 3 AC-coupled differential pair of inputs from the digital video port of a graphics controller. These 3 pairs of inputs can be R, G, B. The differential p-p input voltage has a maximum value of 1.2V, with a minimum value of 175mV.
60, 61	In	SDVO_CLK+/-	**Differential Clock Input associated with SDVO Data Channel (SDVO_R+/-, SDVO_G+/-, SDVO_B+/-)** The range of this clock pair is 100~200MHz. For specific pixel rates in specific modes, this clock pair will run at an integer multiple of the pixel rate. Refer to section 2.1.2 for details.
47, 48	Out	SDVO_STALL+/-	**Stall Signal Pair associated with SDVO Data Channel (SDVO_R+/-, SDVO_G+/-, SDVO_B+/-)** This differential pair is used as a stall indication for a VGA controller, which is capable of driving out SDVO_R+/-, SDVO_G+/-, SDVO_B+/- data. When toggling between 100MHz and 200MHz, the stall indication state is asserted (‘1’ value); when not toggling at all the state is de-asserted (‘0’ value). The differential p-p output voltage has a maximum value of 1.2V, with a minimum value of 175mV.
36, 37	Out	LL1C, LL1C*	**LVDS Differential Clock Channel 1**
17, 18	Out	LL2C, LL2C*	**LVDS Differential Clock Channel 2**
33, 39, 42, 45, 34, 40, 43, 46	Out	LDC[3:0], LDC*[3:0]	**LVDS Differential Data[3:0]**
20, 23, 26, 29, 21, 24, 27, 30	Out	LDC[7:4], LDC*[7:4]	**LVDS Differential Data [7:4]**
32	In	VSWING	**LVDS Swing Control** This pin sets the swing level of the LVDS outputs. A 2.4KOhm resistor should be connected between this pin and LGND using short and wide traces.
14	In	XI/FIN	**Crystal Input/External Reference Input** A parallel resonant 14.31818 MHz crystal (+/-1000 ppm) should be attached between this pin and XO. Alternatively, an external CMOS compatible clock may be used to drive the XI/FIN input.
15	Out	XO	**Crystal Output** A parallel resonant 14.31818 MHz crystal (+/-1000 ppm) should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
16, 49	Power	DVDD	**Digital Supply Voltage (2.5V)**
13, 31	Power	DGND	**Digital Ground**
19, 25, 38, 44	Power	LVDD	**LVDS Supply Voltage (3.3V)**
22, 28, 35, 41	Power	LGND	**LVDS Ground**
56, 62	Power	AVDD	**Analog Supply Voltage (2.5V)**
53, 59	Power	AGND	**Analog Ground**
3	Power	AVDD_PLL	**LVDS PLL Supply Voltage (3.3V)**
8	Power	AGND_PLL	**LVDS PLL Ground**

2.0 Functional Description

2.1 Input Interface

One pair of differential clock signals and three differential pairs of signals (R/G/B) form one channel data. The input data is 10-bit serialized data. Input data operates from 1GHz~2GHz and is a 10x multiple of the clock rate (SDVO_CLK+/-). The CH7308B first de-serializes the input into 10-bit parallel data with synchronization and alignment then the 10-bit characters are mapped into 8-bit color data or control data (Hsync, Vsync, DE).

2.1.1 Interface Voltage Levels

All differential SDVO pairs are AC coupled differential signals. Therefore, there is not a specified DC signal level for the signals to operate at. The minimum differential p-p input voltage is 175mVand the maximum differential p-p input voltage is 1.2V. The minimum differential p-p output voltage is 0.247V and the maximum differential p-p output voltage is 0.453V.

2.1.2 Input Clock and Data Timing

A data character is transmitted least significant bit first. The beginning of a character is noted by the falling edge of the SDVO_CLK+ edge. The skew among input lanes is required to be no larger than 2ns.

The clock rate must be between 100MHz~200MHz. The pixel rate can be 25MP/s~165MP/s. The pixel rate and the clock rate do not have to be equal. The clock rate is a multiple of the pixel rate (1x, 2x or 4x depending on the pixel rate) such that the clock rate remains within the 100MHz~200MHz range. In the condition that the clock rate is running at a multiple of the pixel rate, there isn't enough pixel data to fill the data channels. Dummy fill characters ('0001111010') are used to stuff the data stream. The CH7308B supports the following clock rate multipliers and fill patterns shown in **Table 2**.

Table 2: CH7308B supported Pixel Rates, Clock Rates, Data Transfer Rates and Fill Patterns

Pixel Rate	Clock Rate – Multiplier	Stuffing Format	Data Transfer Rate - Multiplier
CH7308B			
25~50 MP/s	100~200 MHz – 4xPixel Rate	Data, Fill, Fill, Fill	1.00~2.00 GHz – 10xClock Rate
50~100 MP/s	100~200 MHz – 2xPixel Rate	Data, Fill	1.00~2.00 GHz – 10xClock Rate
100~165 MP/s	100~200 MHz – 1xPixel Rate	Data	1.00~2.00 GHz – 10xClock Rate

2.1.3 Synchronization

Synchronization and channel-to-channel deskewing is facilitated by the transmission of special characters during the blank period. The CH7308B synchronizes during the initialization period and subsequently uses the blank periods to re-synch to the data stream.

2.1.4 LVDS-Output

Table 3: Signal Mapping for Single LVDS Channel

	18-bit SPWG / 18-bit OpenLDI	24-bit SPWG / 24-bit OpenLDI
LDC[0](1)	R0 / R0	R0 / R2
LDC[0](2)	R1 / R1	R1 / R3
LDC[0](3)	R2 / R2	R2 / R4
LDC[0](4)	R3 / R3	R3 / R5
LDC[0](5)	R4 / R4	R4 / R6
LDC[0](6)	R5 / R5	R5 / R7
LDC[0](7)	G0 / G0	G0 / G2
LDC[1](1)	G1 / G1	G1 / G3
LDC[1](2)	G2 / G2	G2 / G4
LDC[1](3)	G3 / G3	G3 / G5
LDC[1](4)	G4 / G4	G4 / G6

LDC[1](5)	G5 / G5	G5 / G7
LDC[1](6)	B0 / B0	B0 / B2
LDC[1](7)	B1 / B1	B1 / B3
LDC[2](1)	B2 / B2	B2 / B4
LDC[2](2)	B3 / B3	B3 / B5
LDC[2](3)	B4 / B4	B4 / B6
LDC[2](4)	B5 / B5	B5 / B7
LDC[2](5)	HSYNC / HSYNC	HSYNC / HSYNC
LDC[2](6)	VSYNC / VSYNC	VSYNC / VSYNC
LDC[2](7)	DE / DE	DE / DE
LDC[3](1)		R6 / R0
LDC[3](2)		R7 / R1
LDC[3](3)		G6 / G0
LDC[3](4)		G7 / G1
LDC[3](5)		B6 / B0
LDC[3](6)		B7 / B1
LDC[3](7)		RES / RES

Table 4: Signal Mapping for Dual LVDS Channel

	18-bit SPWG / 18-bit OpenLDI	24-bit SPWG / 24-bit OpenLDI
LDC[0](1)	Ro0 / Ro0	Ro0 / Ro2
LDC[0](2)	Ro1 / Ro1	Ro1 / Ro3
LDC[0](3)	Ro2 / Ro2	Ro2 / Ro4
LDC[0](4)	Ro3 / Ro3	Ro3 / Ro5
LDC[0](5)	Ro4 / Ro4	Ro4 / Ro6
LDC[0](6)	Ro5 / Ro5	Ro5 / Ro7
LDC[0](7)	Go0 / Go0	Go0 / Ro2
LDC[1](1)	Go1 / Go1	Go1 / Ro3
LDC[1](2)	Go2 / Go2	Go2 / Go4
LDC[1](3)	Go3 / Go3	Go3 / Go5
LDC[1](4)	Go4 / Go4	Go4 / Go6
LDC[1](5)	Go5 / Go5	Go5 / Go7
LDC[1](6)	Bo0 / Bo0	Bo0 / Bo2
LDC[1](7)	Bo1 / Bo1	Bo1 / Bo3
LDC[2](1)	Bo2 / Bo2	Bo2 / Bo4
LDC[2](2)	Bo3 / Bo3	Bo3 / Bo5
LDC[2](3)	Bo4 / Bo4	Bo4 / Bo6
LDC[2](4)	Bo5 / Bo5	Bo5 / Bo7
LDC[2](5)	HSYNC / HSYNC	HSYNC / HSYNC
LDC[2](6)	VSYNC / VSYNC	VSYNC / VSYNC
LDC[2](7)	DE / DE	DE / DE
LDC[3](1)		Ro6 / Ro0
LDC[3](2)		Ro7 / Ro1
LDC[3](3)		Go6 / Ro0
LDC[3](4)		Go7 / Go1
LDC[3](5)		Bo6 / Bo0
LDC[3](6)		Bo7 / Bo1
LDC[3](7)		RES / RES
LDC[4](1)	Re0 / Re0	Re0 / Re2
LDC[4](2)	Re1 / Re1	Re1 / Re3
LDC[4](3)	Re2 / Re2	Re2 / Re4
LDC[4](4)	Re3 / Re3	Re3 / Re5
LDC[4](5)	Re4 / Re4	Re4 / Re6
LDC[4](6)	Re5 / Re5	Re5 / Re7
LDC[4](7)	Ge0 / Ge0	Ge0 / Ge2

LDC[5](1)	Ge1 / Ge1	Ge1 / Ge3
LDC[5](2)	Ge2 / Ge2	Ge2 / Ge4
LDC[5](3)	Ge3 / Ge3	Ge3 / Ge5
LDC[5](4)	Ge4 / Ge4	Ge4 / Ge6
LDC[5](5)	Ge5 / Ge5	Ge5 / Ge7
LDC[5](6)	Be0 / Be0	Be0 / Be2
LDC[5](7)	Be1 / Be1	Be1 / Be3
LDC[6](1)	Be2 / Be2	Be2 / Be4
LDC[6](2)	Be3 / Be3	Be3 / Be5
LDC[6](3)	Be4 / Be4	Be4 / Be6
LDC[6](4)	Be5 / Be5	Be5 / Be7
LDC[6](5)	HSYNC / LCTLE	HSYNC / LCTLE
LDC[6](6)	VSYNC / LCTLF	VSYNC / LCTLF
LDC[6](7)	DE / LA6RL	DE / LA6RL
LDC[7](1)		Re6 / Re0
LDC[7](2)		Re7 / Re1
LDC[7](3)		Ge6 / Re0
LDC[7](4)		Ge7 / Re1
LDC[7](5)		Be6 / Be0
LDC[7](6)		Be7 / Be1
LDC[7](7)		RES

2.2 Automatic Panel-Fitting

Serialized input data, sync and clock signals are input to the CH7308B from the graphics controller's serial digital video output port. Input is through three differential data pairs and one differential clock pair. The data rate is in the range of 1.0~2.0GHz. The clock rate, independent from the pixel rate, is 1/10 of the data rate, resulting in the range of 100M~200MHz. Horizontal sync and vertical sync information are embedded in the data stream.

Given the panel information (output timing information), the CH7308B can automatically fit the output timing to the panel. The up-scaler in the CH7308B supports but is not limited to the following LVDS panel sizes:

Table 5: Popular Panel Sizes

WUXGA	1920x1200 (Reduced Blanking)
UXGA	1600x1200
Wide SXGA+	1680x1050
SXGA+	1400x1050
	1360x1024
WSXGA	1440x900
SXGA	1280x1024
	1280x960
WXGA	1366x768
XGA	1024x768
	1024x600
SVGA	800x600

The CH7308B is capable of up-scaling images containing 1400 active horizontal pixels or less to the native resolution of the supported LVDS panel. For resolutions containing more than 1400 horizontal pixels, no up-scaling will be done. The up-scaler periodically sends a pair of SDVO_STALL(+/-) signals to the graphics controller to halt the transmission of one line of active video data. When the SDVO_STALL(+/-) signals toggle between 100MHz and 200MHz, this is interpreted as asking for next line of video data to be "stalled"; not toggling at all is considered as asking for the next line of video data to be sent. The Up-scaler performs 2D interpolation of the graphics input data and does not change the pixel rate between the input and the output. The 2D interpolation consists of programmable non-linear functions. The maximum pixel rate supported by the Up-scaler is 200MP/s.

2.3 Emission Reduction Clock

LVDS output can support a ±2.5% spreading in the output clock to reduce EMI emissions. The frequency and the amplitude of the spreading triangle waveform can be programmed via opcode commands.

2.4 Dithering

The dither engine in the CH7308B converts 24-bit per pixel RGB data to 18-bit per pixel RGB data before sending the data to the LVDS encoder. The maximum pixel rate supported is 165MP/s. This feature supports 18-bit LVDS panels only.

2.5 Power Sequencing

The CH7308B conforms to the SPWG requirements on power sequencing. The timing specification shown in figure 4 is a superset of the requirements dictated by the SPWG specification. The timing parameters can be programmed to different values via opcode commands to suit the timing requirements defined by the particular panel specifications to be used.

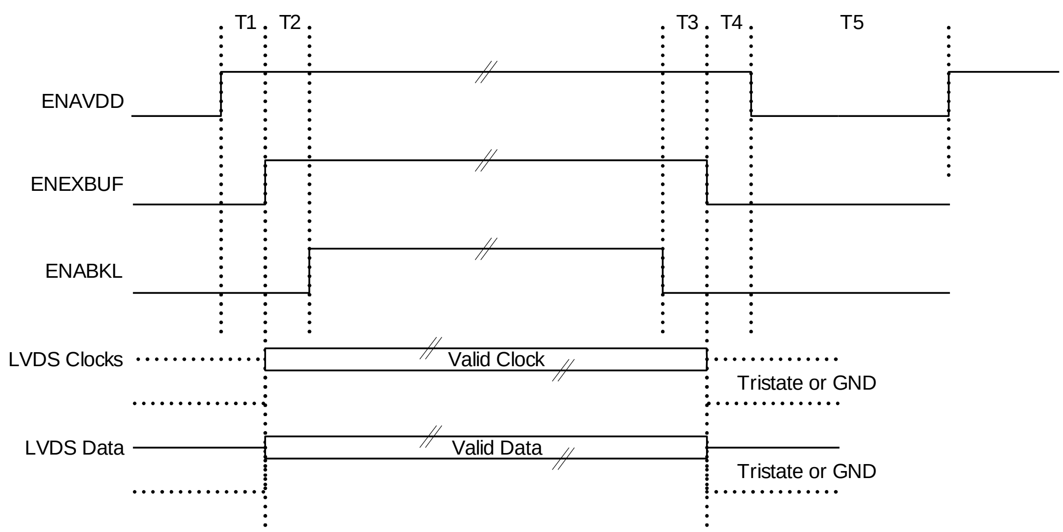

Figure 3: Power Sequencing

Table 6: Power Sequencing

	Range	Increment
T1	1-1023 ms	1 ms
T2	1-1023 ms	1ms
T3	1-1023 ms	1ms
T4	1-1023 ms	1 ms
T5	1-1023 ms	1ms

The power-on sequence begins when the LVDS software registers are set properly via opcode commands and the internal PLL lock detection circuit, the internal Sync detection circuit, and the XCLK detection circuit (see section 2.6) indicate that HSYNC, VSYNC and XCLK are stable. The power-off sequence begins when any of the detection circuits indicates instability in the timing signals (see section 2.6), or through opcode programming. Once the power-off sequence starts, the internal state machine will complete the power-off sequence and power-on sequence is allowed only after T5 is passed.

To verify the T1 – T5 LVDS Panel Power Sequencing, please see TB49 for more details.

2.6 Panel Protection

Damage to the LCD panel may occur if either HSYNC or VSYNC signals are absent from the LVDS link. This situation can happen when there is a catastrophic failure in the PC or the graphics system. The CH7308B is designed to prevent damage to the panel under such a failure. If the system fails, the CH7308B does not expect any software instruction from the graphics controller to power down the panel. Detection circuits are used to monitor the three timing signals – HSYNC, VSYNC and XCLK. If any one, combination of, or all of these signals becomes unstable or missing, the CH7308B will commence Power Down Sequencing.

The power up sequence can occur only if there are no missing HSYNC and VSYNC, the input clock is available, the PLL clock is stable and the SetActiveOutput opcode is called. The power down sequence is initiated if one of those conditions fails. The panel protection circuitry is comprised of the PLL Lock Detection block, which detects an unstable clock from the LVDS PLL, the SYNC Detection block, which detects missing inputs HSYNC and VSYNC, and the Clock Detection block, which detects missing input CLOCK.

The SYNC Detection block consists of counters to count HSYNC and VSYNC pulses. One counter is used to count the number of HSYNC pulses per frame over 3 frames. The end counts for all 3 frames must be equal to enable the power up sequence. In addition, the SYNC Detection block checks for the presence of VSYNC and HSYNC. If VSYNC is missing for 2 frames or if HSYNC is missing for 32us, the power up sequence is disabled. Conversely, if the panel has been enabled and the number of HSYNC pulses per frame is different over 3 frames, VSYNC is missing for 2 frames, or HSYNC is missing for 32us, the CH7308B will go into a power down sequence.

The PLL Lock Detection, SYNC Detection and Clock Detection blocks can be defeated independently. Opcode commands are supported for these features. The power up sequence can also occur if the panel protection circuitry is defeated.

2.7 Command Interface

Communication is through a two-wire path, control clock (SPC) and data (SPD). The CH7308B accepts incoming control clock and data from a graphics controller, and is capable of redirecting that data stream to the ADD2 card PROM, DDC, or CH7308B internal registers. The control bus is able to run up to 1MHz.

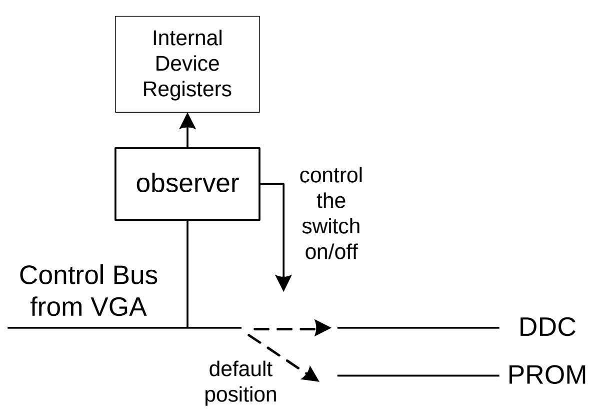

Figure 4: Control Bus Switch

Upon reset, the default state of the control bus direction switch is to redirect the control bus interface to the ADD2 PROM. At this stage, the CH7308B observes the Control bus traffic. If the observing logic sees a control bus transaction destined for the internal registers (device address 70h or 72h), it disables the PROM output pairs, and switches to internal registers. In the condition that traffic is to the internal registers, an opcode command is used to set the redirection circuitry to the appropriate destination (ADD2 PROM or DDC). Redirecting the traffic to internal registers while at the stage of traffic to DDC occurs on observing a STOP after a START on the control bus.

2.7.1 NAND Tree Test

CH7308B provides "NAND TREE Testing" to verify IO cell functions at the PC board level. This test will check the interconnect between the chip's I/O and the printed circuit board for faults (soldering, bent leads, open printed circuit board traces, etc.). The NAND tree test is a simple serial logic which turns all IO cell signals to input mode, connects all inputs with NAND gates as shown in Figure 6 and switches each signal to high or low according to the sequence in **Table 7**. The test results are then passed out of pin 48 (SDVO_STALL-). This test is enabled when the BSCAN pin (pin 63) is set to "1".

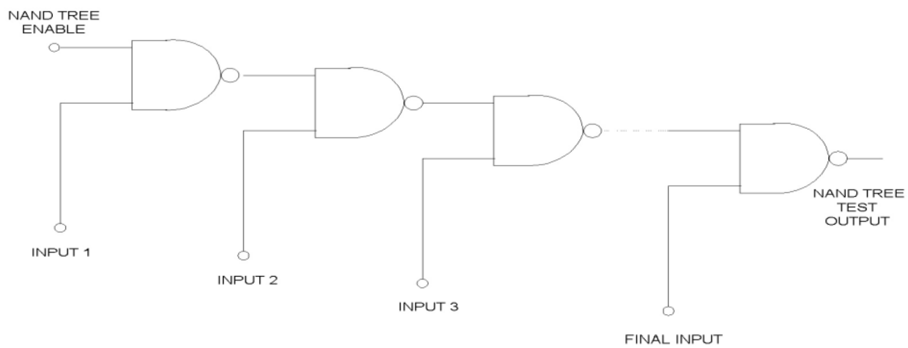

Figure 5: NAND Tree Connection

Testing Sequence
Set BSCAN = 1; (internal weak pull low)
Set all signals listed in **Table 7** to 1.
Set all signals listed in **Table 7** to 0, toggle one by one with a suggested time period of 200 ns.
Pin 48 will change its value each time an input value changed.

Table 7: Signal Order in the NAND Tree Testing

Order	Pin Name	LQFP Pin
1	ENABKL	1
2	ENAVDD	2
3	RESET*	4
4	AS	5
5	SPC	6
6	SPD	7
7	SD_PROM	9
8	SC_PROM	10
9	SD_DDC	11
10	SC_DDC	12
11	XI	14
12	XO	15
13	LL2C	17
14	LL2C*	18
15	LDC7	20
16	LDC7*	21
17	LDC6	23
18	LDC6*	24
19	LDC5	26
20	LDC5*	27
21	LDC4	29
22	LDC4*	30
23	LDC3	33
24	LDC3*	34
25	LL1C	36
26	LL1C*	37
27	LDC2	39
28	LDC2*	40
29	LDC1	42
30	LDC1*	43
31	LDC0	45
32	LDC0*	46
33	SDVOB_STALL+	47
34	SDVOB_STALL-	48

3.0 Register Control

The CH7308B is controlled by using Intel opcodes through the serial port. The serial bus uses only the SPC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device will retain all register values during power down modes.

For details regarding Intel® SDVO opcodes, please contact Intel®.

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All 2.5V power supplies relative to GND All 3.3V power supplies relative to GND	-0.5 -0.5		3.0 5.0	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	-40		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS1}	Vapor phase soldering (5 seconds)			260	°C
T_{VPS2}	Vapor phase soldering (11 seconds)			245	°C
T_{VPS3}	Vapor phase soldering (60 seconds)			225	°C

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The temperature requirements of vapor phase soldering apply to all standard and lead free parts.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce a destructive latchup.

4.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Analog Power Supply Voltage	2.375	2.5	2.625	V
AVDD_PLL	Analog PLL Power Supply Voltage	3.100	3.3	3.500	V
DVDD	Digital Power Supply Voltage	2.375	2.5	2.625	V
LVDD	LVDS Power Supply	3.100	3.3	3.500	V
VDD33	Generic for all 3.3V supplies	3.100	3.3	3.500	V
VDD25	Generic for all 2.5V supplies	2.375	2.5	2.625	V
	Ambient operating temperature	-40		85	°C

4.3 Electrical Characteristics

(Operating Conditions: T_A = -40°C – +85°C, VDD25 =2.5V ± 5%, VDD33=3.3V± 5%)

Symbol	Description	Min	Typ	Max	Units
I_{VDD25}	Total VDD25 supply current (2.5V supplies) (no upscaler)		170	200	mA
I_{VDD33}	Total VDD33 supply current (3.3V supply) (no upscaler)		70	85	mA
$I_{VDD25UP}$	Total VDD25 supply current (2.5V supplies) (with upscaler enabled)		270	340	mA
$I_{VDD33UP}$	Total VDD33 supply current (3.3V supply) (with upscaler enabled)		70	85	mA
I_{PD}	Total Power Down Current (all supplies)		30		uA

4.4 DC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$V_{RX\text{-}DIFFp\text{-}p}$	SDVO Receiver Differential Input Peak to Peak Voltage	$V_{RX\text{-}DIFFp\text{-}p} = 2 * \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-} \rvert$	0.175		1.200	V
$Z_{RX\text{-}DIFF\text{-}DC}$	SDVO Receiver DC Differential Input Impedance		80	100	120	Ω
$Z_{RX\text{-}COM\text{-}DC}$	SDVO Receiver DC Common Mode Input Impedance		40	50	60	Ω
$Z_{RX\text{-}COM\text{-}INITIAL\text{-}DC}$	SDVO Receiver Initial DC Common Mode Input Impedance	Impedance allowed when receiver terminations are first turned on	5	50	60	Ω
$V_{STALL\text{-}DIFFp\text{-}p}$	SDVO Stall Differential Output Peak to Peak Voltage	$V_{STALL\text{-}DIFFp\text{-}p} = 2 * \lvert V_{STALL\text{-}D+} - V_{STALL\text{-}D-} \rvert$	0.8		1.200	V
V_{SDOL} [1]	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH} [2]	Serial Port (SPC, SPD) Input High Voltage		2.0		VDD25+ 0.5	V
V_{SPIL} [2]	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Serial Port Inputs		0.25			V
V_{DDCIH}	DDC Serial Port Input High Voltage		4.0		VDD5 + 0.5	V
V_{DDCIL}	DDC Serial Port Input Low Voltage		GND-0.5		0.4	V
V_{PROMIH}	PROM Serial Port Input High Voltage		4.0		VDD5 + 0.5	V
V_{PROMIL}	PROM Serial Port Input Low Voltage		GND-0.5		0.4	V
V_{SD_DDCOL} [3]	SPD (serial port data) Output Low Voltage from SD_DDC (or SD_EPROM)	Input is V_{INL} at SD_DDC or SD_EPROM. 4.0KΩ pullup to 2.5V.			$0.9*V_{INL}$ + 0.25	V

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{DDCOL} [4]	SC_DDC and SD_DDC Output Low Voltage	Input is V_{INL} at SPC and SPD. 5.6KΩ pullup to 5.0V.			0.933*V_{INL} + 0.35	V
$V_{EPROMOL}$ [5]	SC_EPROM and SD_EPROM Output Low Voltage	Input is V_{INL} at SPC and SPD. 5.6KΩ pullup to 5.0V.			0.933*V_{INL} + 0.35	V
V_{ASIH}	AS Input High Voltage		2.0		VDD25 + 0.5	V
V_{ASIL}	AS Input Low Voltage		GND-0.5		0.5	V
I_{ASPU}	AS Pull Up Current	V_{IN} = 0V	10		40	uA
$V_{RESETIH}$	RESET* Input High Voltage		2.7		VDD33 + 0.5	V
$V_{RESETIL}$	RESET* Input Low Voltage		GND-0.5		0.5	V
$I_{RESETPU}$	RESET* Pull Up Current	V_{IN} = 0V	10		40	uA
V_{TESTIH}	BSCAN Input High Voltage		2.0		VDD25 + 0.5	V
V_{TESTIL}	BSCAN Input Low Voltage		GND-0.5		0.5	V
I_{TESTPD}	BSCAN Pull Down Current	V_{IN} = 2.5V	10		40	uA
V_{XIIH}	XI (for clock input) Input High Voltage		2.6		VDD33 + 0.5	V
V_{XIIL}	XI (for clock input) Input Low Voltage		GND-0.5		0.6	V
$V_{MISCAOH}$	ENAVDD, ENABKL Output High Voltage	I_{OH} = -6.5mA	VDD-0.2			V
$V_{MISCAOL}$	ENAVDD, ENABKL Output Low Voltage	I_{OL} = 9.0mA			0.2	V

Notes:
1. V_{SDOL} is the SPD output low voltage when transmitting from internal registers, not from DDC or EEPROM.
2. V_{SPIH} and V_{SPIL} are the serial port (SPC and SPD) input low voltage when transmitting to internal registers. Separate requirements may exist for transmission to the DDC and EEPROM.
3. V_{SD_DDCOL} is the output low voltage at the SPD pin when the voltage at SD_DDC or SD_EPROM is V_{INL}. Maximum output voltage has been calculated with a worst case pullup of 4.0kΩ to 2.5V on SPD.
4. V_{DDCOL} is the output low voltage at the SC_DDC and SD_DDC pins when the voltage at SPC and SPD is V_{INL}. Maximum output voltage has been calculated with 5.6k pullup to 3.3V on SC_DDC and SD_DDC.
5. $V_{EPROMOL}$ is the output low voltage at the SC_EPROM and SD_EPROM pins when the voltage at SPC and SPD is V_{INL}. Maximum output voltage has been calculated with 5.6kΩ pullup to 5V on SC_EPROM and SD_EPROM.

4.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
UI_{DATA}	SDVO Receiver Unit Interval for Data Channels		Typ. – 300ppm	1/[Data Transfer Rate]	Typ. + 300ppm	ps
f_{SDVOB_CLK}	SDVO CLK Input Frequency		100		200	MHz
f_{PIXEL}	SDVO Receiver Pixel frequency		25		200	MHz
f_{SYMBOL}	SDVO Receiver Symbol frequency		1		2	GHz
t_{RX-EYE}	SDVO Receiver Minimum Eye Width		0.4			UI
$t_{RX-EYE-JITTER}$	SDVO Receiver Max. time between jitter median and max. deviation from median				0.3	UI
$V_{RX-CM-ACp}$	SDVO Receiver AC Peak Common Mode Input Voltage				150	mV
$RL_{RX-DIFF}$	Differential Return Loss	50MHz – 1.25GHz	10			dB
RL_{RX-CM}	Common Mode Return Loss	50MHz – 1.25GHz	6			dB
t_{SKEW}	SDVO Receiver Total Lane to Lane Skew of Inputs	Across all lanes			2	ns
C_{XI}	XI Input Capacitance				15	pF
$f_{TOL\ XI}$	XI Input Clock Frequency Tolerance (when crystal not used)		-1000		+1000	ppm
DC_{XI}	XI Input Clock Duty Cycle (when crystal not used)		45		55	%
T_{SPR}	SPC, SPD Rise Time (20% - 80%)	Standard mode 100k Fast mode 400k 1M running speed			1000 300 150	ns ns ns
T_{SPF}	SPC, SPD Fall Time (20% - 80%)	Standard mode 100k Fast mode 400k 1M running speed			300 300 150	ns ns ns
T_{PROMR}	SC_PROM, SD_PROM Rise Time (20% - 80%)	Fast mode 400K			300	ns
T_{PROMF}	SC_PROM, SD_PROM Rise Time (20% - 80%)	Fast mode 400K			300	ns
T_{DDCR}	SC_DDC, SD_DDC Rise Time (20% - 80%)	Standard mode 100k			1000	ns
T_{DDCF}	SC_DDC, SD_DDC Fall Time (20% - 80%)	Standard mode 100k			300	ns

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$T_{DDCR\text{-}DELAY}$[1]	SC_DDC, SD_DDC Rise Time Delay (50%)	Standard mode 100k		0		ns
$T_{DDCF\text{-}DELAY}$[1]	SC_DDC, SD_DDC Fall Time Delay (50%)	Standard mode 100k		3		ns

Notes:
1. Refers to the figure below, the delay refers to the time pass through the internal switches.

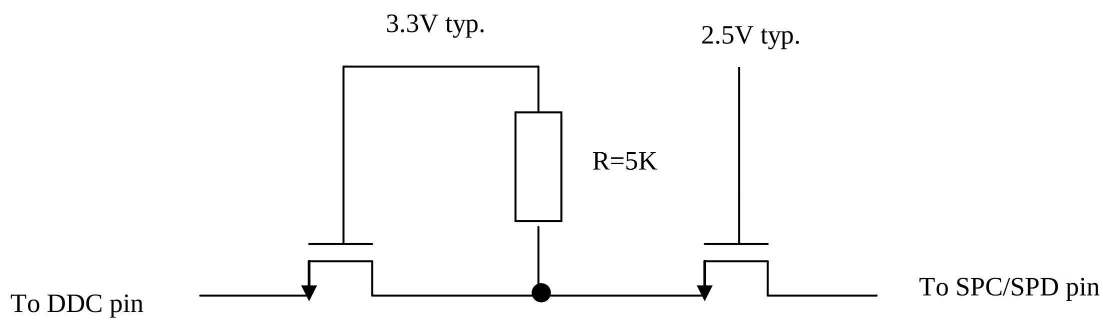

Figure 6: DDC – SPC/SPD Circuit

4.6 LVDS Output Specifications

The LVDS specifications meet the requirements of ANSI/EIA/TIA-644. Refer to **Figure 7** for definitions of parameters.

Symbol	Description	Test Condition	Min	Typ	Max	Unit
$\|V_t\|$	Steady State Differential Output Magnitude for logic 1	100Ω differential load	247		453	mV
$\| V_t *\|$	Steady State Differential Output Magnitude for logic 0	100Ω differential load	247		453	mV
$\| V_t \| - \| V_t *\|$	Steady State Magnitude of Differential between Logic 1 and 0 Outputs	100Ω differential load			50	mV
$\|V_{OS}\|$	Steady State Magnitude of Offset Voltage for Logic 1	Measured at centertap of two 50Ω resistors connected between outputs	1.125		1.375	V
$\|V_{OS}*\|$	Steady State Magnitude of Offset Voltage for Logic 0	Measured at centertap of two 50Ω resistors connected between outputs	1.125		1.375	V
|Vos|-|Vos*|	Steady State Magnitude of Offset Difference between Logic States	Measured at centertap of two 50Ω resistors connected between outputs			50	mV
f_{LLC} [1]	LVDS Output Clock Frequency		25	108		MHz
t_{UI} [1]	LVDS data unit time interval	25MHz < f_{LLC}<108MHz	1.3		5.7	ns
t_r	LVDS data rise time t_{UI} > 5ns 1.3ns<t_{UI}<5ns	100Ω and 5pF differential load 20%->80% Vswing			0.3*t_{UI} 1.5	ns ns
t_f	LVDS data fall time T_{UI} > 5ns 1.3ns<t_{UI}<5ns	100Ω and 5pF differential load 80%->20% Vswing			0.3*t_{UI} 1.5	ns ns
Vring	Voltage ringing after transition	100Ω and 5pF differential load			20% Vswing	

Note 1: Corresponds to maximum pixel rate f_{XCLK} for single channel operation. Dual channel operation is required for pixel rates greater than 108MHz.

4.7 LVDS Output Timing

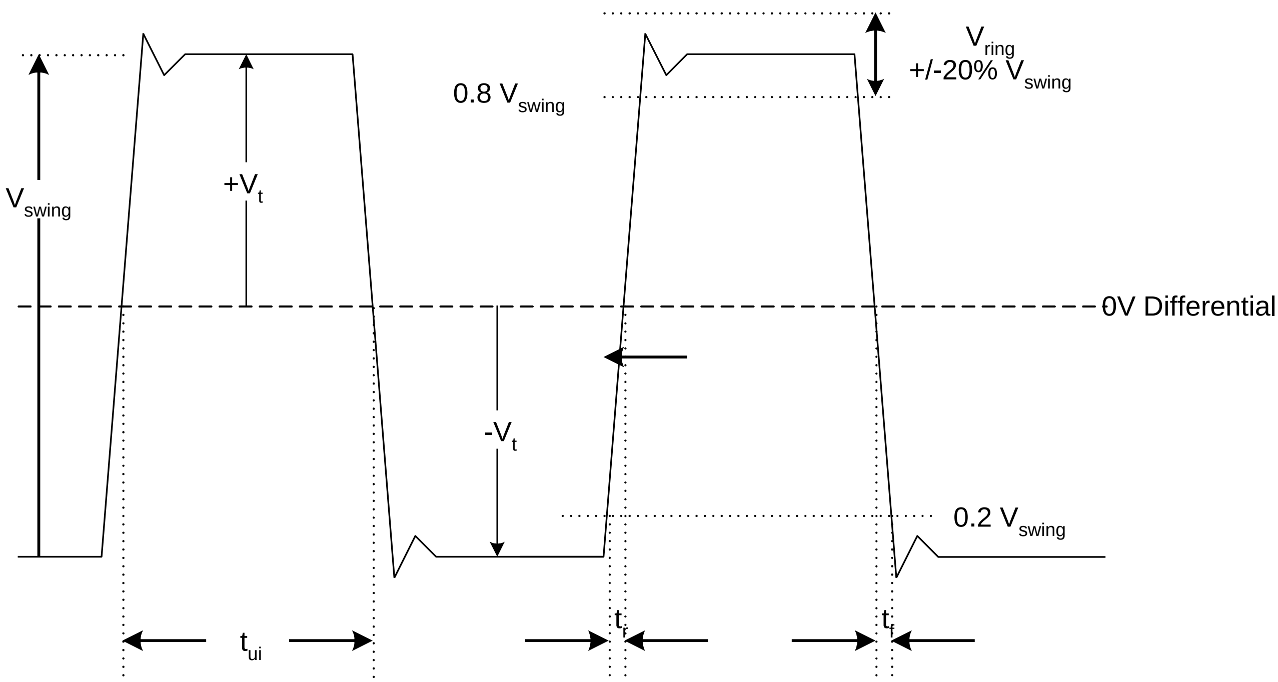

Figure 7: AC Timing for LVDS Outputs

Table 8: AC Timing for LVDS Outputs

Symbol	Parameter	Min	Typ	Max
$\lvert V_t \rvert$	Steady State Differential Output Magnitude	see section 4.6		
V_{SWING}	Voltage Difference between the two Steady State Values of Output	$\lvert V_t \rvert + \lvert V_t{}^* \rvert$		
t_{Ui}	Unit time interval	see section 4.6		
t_r	Rise time	see section 4.6		
t_f	Fall time	see section 4.6		

5.0 Package Dimensions

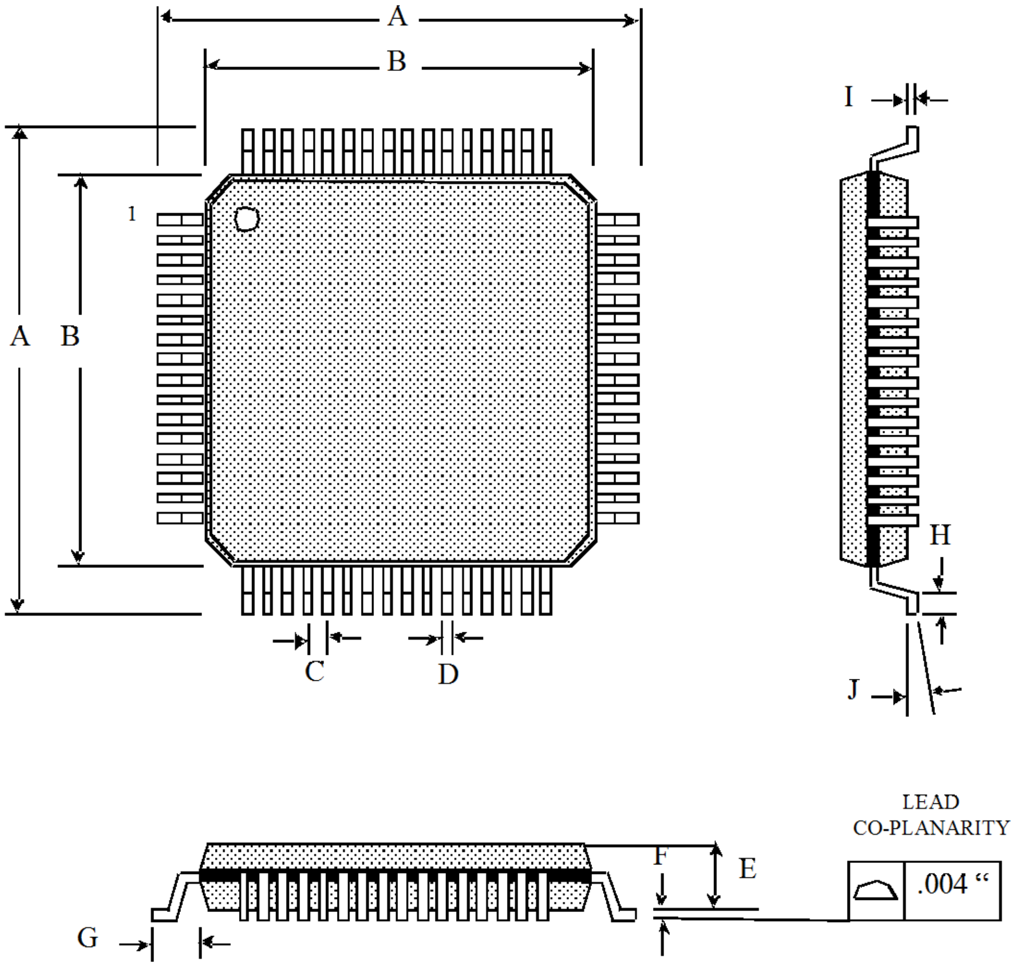

Table of Dimensions

No. of Leads		SYMBOL									
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

Figure 8: 64 Pin LQFP Package

6.0 Revision History

Table 9: Revisions

Rev. #	Date	Section	Description
1.0	11/23/04	All	Version 1.0
1.1	12/20/04	2.2	Updated panel-fitting scaler information.
		4.1	Updated T_{VPS} – Vapor phase soldering information.
1.2	1/05/05	Ordering Information	Lead Free tape and reel part number added.
		4.1	Note 1 updated.
1.3	1/27/05	4.4	Added $V_{MISCAOH}$ and $V_{MISCAOL}$ DC Specification data.
1.4	2/2/05	1.1, 1.2	Added TEST pin (pin50) and description.
		2.5	Updated Figure 4 and added reference to TB49.
		Table 8	Corrected note to which section to refer to
		2.2	Added Wide SXGA+, 1680 x 1050, to Table 5
1.5	2/7/05	1.2	Change descriptions for pin 11, 12, 14, 15, 60, 61
		2.6	Replace "PANEN set to 1" with "SetActiveOutput is called".
		4.4, 4.5, 4.6, 4.7	Change spec. values.
		4.4	Changed conditions and value for V_{DDCOL}
		4.5	Changed definition of f_{PIXEL} and value for $RL_{RX-DIFF}$
		4.6	Changed parameters f_{LLC}, t_{UI} , t_R, t_F.
1.61	8/8/05	All	Changed the maximum pixel rate to 140MP/s
		Features, 2.2	Changed the maximum upscale resolution to 1600x900
		Table 2	Updated the table to reflect the new maximum pixel rate of 140MP/s
		2.2	Removed panel sizes no longer supported.
		Ordering Information	Added a footnote stating the current revision of the CH7308A is revision D and marked as XUD
		General Description	The last sentence of the 2nd paragraph was edited to avoid confusion in what is the maximum pixel rate per channel.
1.7	10/12/05	Ordering information	Added Green parts into the ordering information.
		4.4, 4.5	Added serial interface AC and DC Electrical Specification information.
1.8	12/20/05	General Description	Sentence mentioning supported pixel rates for dual panel LVDS panels (100MP/s to 140MP/s).
		3.0 Register Control	Changed the first sentence to clarify that the CH7308A is controlled by use of Intel Opcodes instead of register reads/writes.
2.0	1/11/2006	All text and figures	Modified the datasheet to include the CH7308B.
		Features and General Description	Added CH7308B related information in the features section and the second paragraph of the General Description section.
		Ordering Information	Added CH7308B ordering information.
2.1	3/13/2008	Features	Added 1600x1200 and 1920x1200 reduced blanking resolution support.
		Pin Description	Pin 63 and Pin 64 are changed to "open"
		Table 5	Added 1920x1200 resolution reduced blanking to Table 5.
2.2	8/5/2008	Figure 3	Added LVDS Clock and LVDS Data to Figure 3.
2.3	9/22/2008	4.4	Updated DC Specifications.
2.4	12/2/2008	4.2, 4.3.	Updated operating temperature.
2.41	3/30/2008	1.2 Table 1	Updated description for Pin 63.
3.0	05/10/2011	4.1, 4.2 All	Update Ambient operating temperature to -40°C to +85°C. Remove CH7308A

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ORDERING INFORMATION			
Part Number	Package Type	Number of Pins	Voltage Supply
CH7308B-TF	Lead Free - LQFP	64	2.5V, 3.3V
CH7308B-TF-TR	Lead Free - Tape and Reel LQFP	64	2.5V, 3.3V

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