CH7510 DisplayPort Receiver with Integrated mini-LVDS Timing Controller (TCON)

FEATURES

- Fully compliant with DisplayPort Specification version 1.1a and Embedded DisplayPort (eDP) Specification version 1.2.
- Support 2 Main Link Lanes at 1.62Gb/s or 2.7Gb/s link rate
- Support LCD panel with resolution up to 1920x1200 @60Hz or 1366x768@120Hz.
- Support 6 pairs and 8 pairs mini-LVDS output for both 6-bit and 8-bit LCD panel interface, with the maximum clock up to 300MHz
- Flexible TCON output control, and flexible mini-LVDS output mapping
- Support single clock mode: R/L mini-LVDS data output with one common mini-LVDS clock.
- Support HDCP Amendment for Displayport Rev.1.1
- Support Gamma correction control
- Support dithering and 6-bit + FRC
- Support Enhanced Framing Mode
- Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- 2 external clock configuration: 27MHz crystal, 27MHz reference clock
- Support 2-level and 3-level Gate Drivers (output STV1 and STV2 at the same time), 8 programmable GPOs for driving Source or Gate drivers in TFT LCD panel
- Programmable LCD panel power sequence
- Support internal test pattern
- Blank panel during invalid input
- Support OSD display when GPIO pins control Back-light Luminance
- Supports PWM. Backlight luminance level control through AUX channel, and GPIO pin Support Dynamic Backlight Control (OSD display)
- Support analog current interface for light sensor
- Support loading of CH9904 BOOT ROM when power up
- Support updating BOOT ROM through I2C Slave or AUX CH
- Programmable power management. Support Hardware fully power down control
- Spread spectrum control is available for transmitting mini-LVDS signal
- Hot Plug Detection
- Achieve bit error rate $<10^{-9}$ for raw transport data per lane and symbol error rate $<10^{-12}$ for control data
- Offered in a 68-pin QFN package

GENERAL DESCRIPTION

Chrontel's CH7510 is a low-cost, low-power semi-conductor device that integrates a mini-LVDS timing controller (TCON). This device receives high-speed serialized video data and uses the Block Diagram, fully programmable TCON to drive the LCD panel modules through integrated mini-LVDS interface, which is operating in low-voltage and low EMI emission.

The CH7510 is designed to comply with DisplayPort Specification 1.1a and Embedded DisplayPort Specification version 1.2. It supports two Main Link lanes that are capable of receiving data rate running at 1.62Gb/s or 2.7Gb/s. The device can accept input data in 18-bit 6:6:6 or 24-bit 8:8:8 RGB digital formats.

The high performance CH7510's TCON consists of programmable logic blocks for processing input video data, configurable timing control signals and video data to interface LCD Gate Drivers and Source Drivers. During system power up, setting the power on/off sequence for a particular LCD panel can be achieved through CH7510's TCON configuration registers. This timing control information is stored in the BOOT ROM along with the EDID information that will be used during the Link Training through AUX Channel.

The CH7510 has a luminance control function to adjust LCD backlight. The brightness control command sent through AUX Channel can be dynamically translated by CH7510 and converted into LCD backlight control signal. The CH7510 will save the last setting of brightness level value in the BOOT ROMand use it upon power up.

Advanced Power Management Unit (PMU) is designed to reduce power consumption in normal operation.

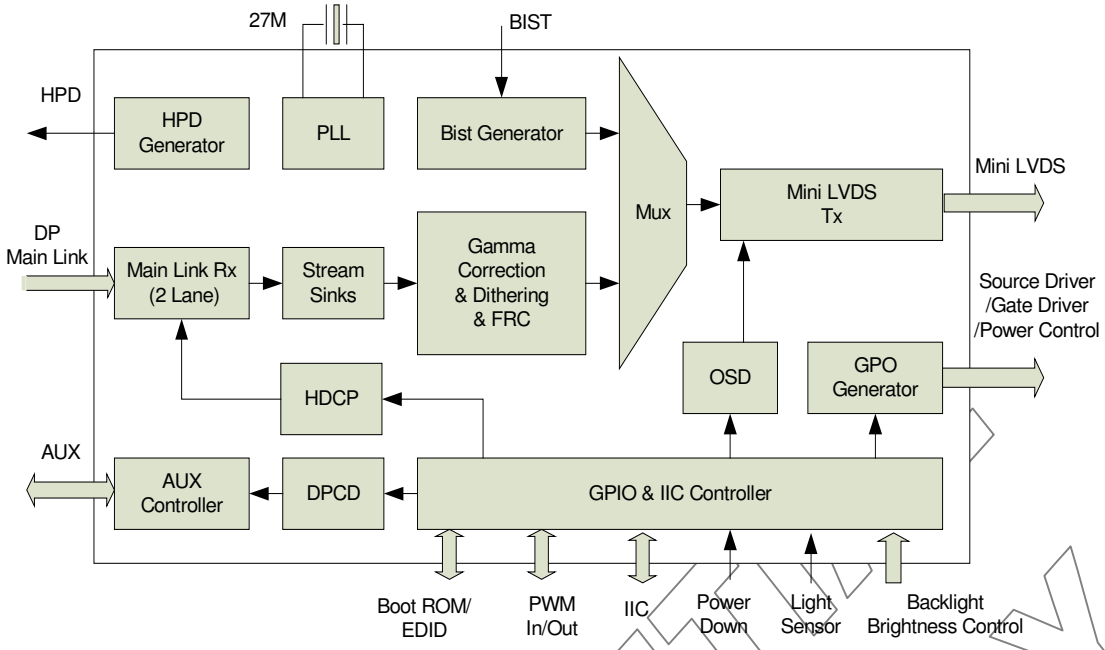

Figure 1: Functional Block Diagram

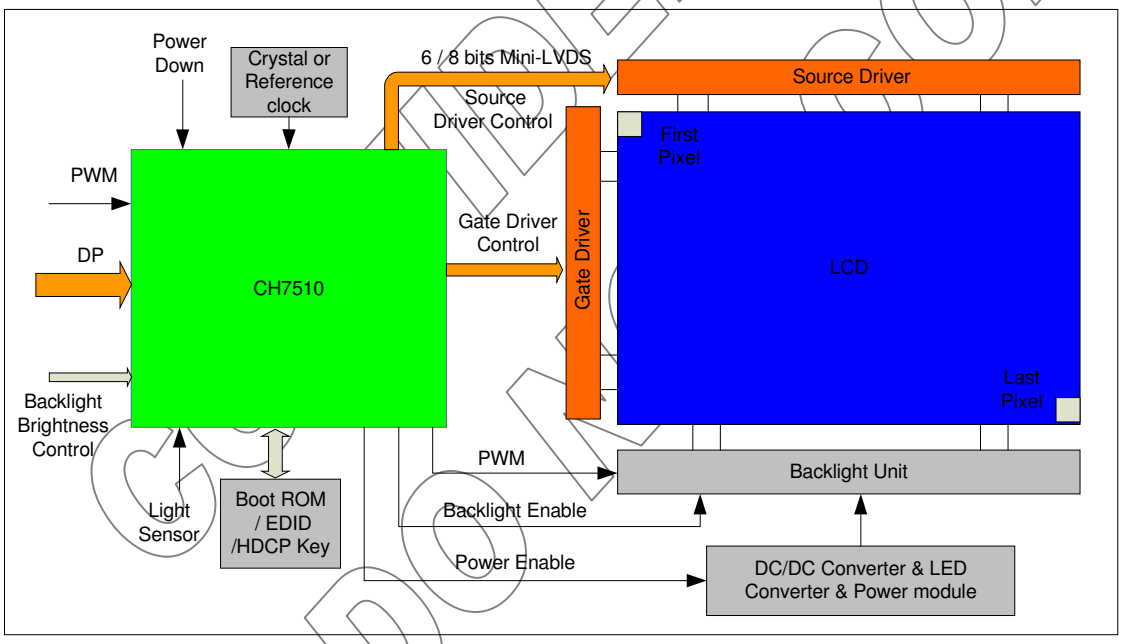

Figure 2: System Application Diagram

1.0 PIN ASSIGNMENT

1.1 Package Diagram

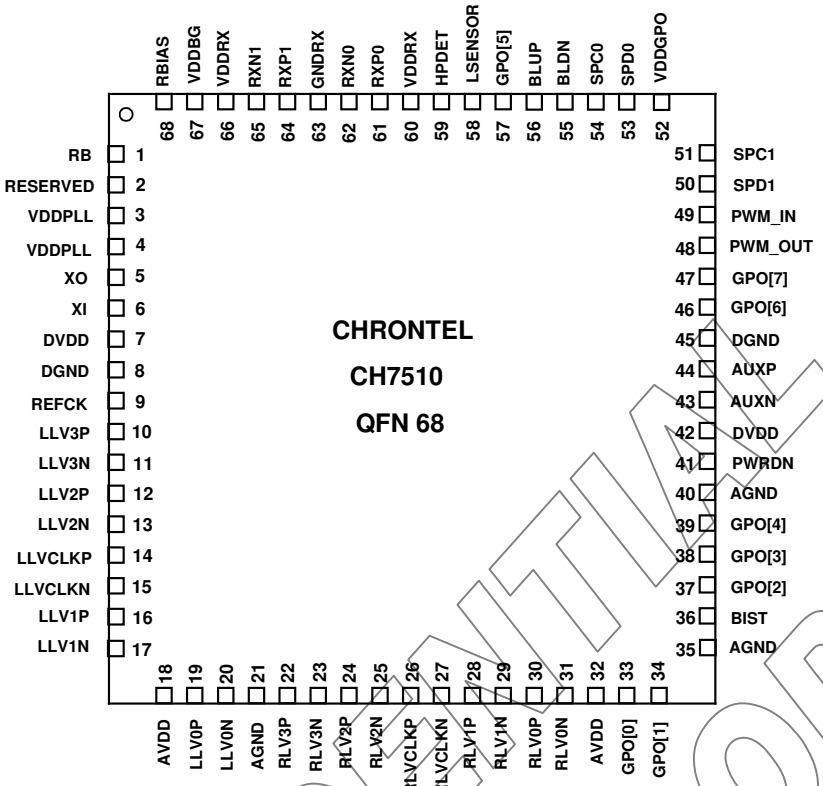

Figure 2: CH7510 68-pin QFN pin out

1.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1	In	RB	**Reset Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
2		RESERVED	**Reserved Pin**
5,6	In	XO, XI	**27MHz Crystal Input**
9	In	REFCK	**Reference Clock Input** This pin is used as clock input pin when injecting 27/14.318MHz clock to CH7510
10~17, 19,20, 22~31	Out	LLV[3:0]P/N, LLVCLKP/N, RLV[3:0]P/N, RLVCLKP/N,	**mini-LVDS Output** LLV0P/N ~ LLV3P/N: Left channel data LLVCLKP/N: Left channel clock RLV0P/N ~ RLV3P/N: Right channel data RLVCLKP/N: Right channel clock Refer to register description part for detailed mini-LVDS pin mapping
33,34,36 39,57	Out	GPO[5: 0]	**LCD Source/Gate Driver Control**

~39,57			Refer to register description for detailed GPO mapping
36	In	BIST	**BIST Enable for TCON application**
41	In	PWRDN	**Power Down Control** CH7510 enters/exit power down state when receiving active low pulse from this pin
43	In/Out	AUXN	**Aux channel differential negative input/output**
44	In/Out	AUXP	**Aux channel differential positive input/output**
46	Out	GPO[6]	**General Purpose Output Pin** LCD panel VCC enable output by default
47	Out	GPO[7]	**General Purpose Output Pin** LCD panel backlight enable output by default
48	Out	PWM_OUT	**PWM output for backlight brightness dimming** PWM Duty Cycle Range: 0~100%(16 steps) The output Frequency from PWM_OUT0 can be up to 400KHz. Voltage level is 3.3V. Bypass PWM input, and while in bypass mode, frequency of PWM_OUT0 can be up to 1MHz.
49	In	PWM_IN	**Backlight brightness PWM input** PWM_IN has two work modes: Bypass mode and Duty Cycle Multiplication with AUX CH mode. In bypass mode, the input frequency to PWM_IN can be up to 1MHz. In Duty Cycle Multiplication with AUX CH mode, the input frequency to PWM_IN can be up to 50KHz. Voltage level is 3.3V.
50	In/Out	SPD1	**Serial Port Data Input/Output for Chip BOOT ROM/EDID/HDCP ROM** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4kΩ - 9 kΩ pull up resistor to 3.3V.
51	Out	SPC1	**Serial Port Clock Output for Chip BOOT ROM/EDID/HDCP ROM** This pin functions as the clock output of the serial port and operates with output from 0 to 3.3V. This pin requires an external 4kΩ - 9kΩ pull up resistor to 3.3V.
53	In/Out	SPD0	**Serial Port Data Input / Output for CH7510 I2C Slave** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4kΩ - 9 kΩ pull up resistor to 3.3V. CH7510 serial port device address is 0x21 and transmitted in SPD as following(MSB transmitted first) B7 B6 B5 B4 B3 B2 B1 B0 0 1 0 0 0 0 1 R/W
54	In	SPC0	**Serial Port Clock Input for CH7510 I2C Slave** This pin functions as the clock input of the serial port and operates with inputs from 0 to 3.3V. This pin requires an external 4kΩ - 9kΩ pull up resistor to 3.3V.
55	In	BLDN	**Decrement Backlight Brightness Input**
56	In	BLUP	**Increment Backlight Brightness Input**
58	In	LSENSOR	**Light Sensor Input**
59	Out	HPDET	**Hot Plug Detect** This output pin indicates whether this device is active or not. It also generates interrupt pulse as defined by DP standard. Output voltage is 3.3v.
61,62	In	RXP0, RXN0	**Main link Lane 0 input** One pair of differential data input. It handles clock-embedded high speed differential data input as DP standard

63,64	In	RXP1, RXN1	**Main link Lane 1 input** One pair of differential data input. It handles clock-embedded high speed differential data input as DP standard
68	In	RBIAS	**Band-gap bias** This pin should be left open or pulled low with a 10k resistor in the application.
3,4	Power	VDDPLL	**Stream PLL Power Supply (1.8V)**
7,42	Power	DVDD	**Digital Power Supply (1.8V)**
8,45	Power	DGND	**Digital Power Ground**
18,32	Power	AVDD	**LVDS Power Supply (3.3V)**
21,35,40	Power	AGND	**LVDS Power Ground**
52	Power	VDDGPO	**GPO Power Supply (3.3V)**
60,66	Power	VDDRX	**Main link Power Supply (1.8V)**
63	Power	GNDRX	**Main link Power Ground**
67	Power	VDDBG	**Band-gap Power Supply (1.8V)**

Note:

1. **The Voltage of LVDD (3.3V) should be given earlier than the DVDD and AVDD. And after the Powers are stable, please give a Resetb signal (low to high signal).**
2. **The rise slope time of DVDD(T4) should not be larger than 2ms.**

2.0 PACKAGE DIMENSIONS

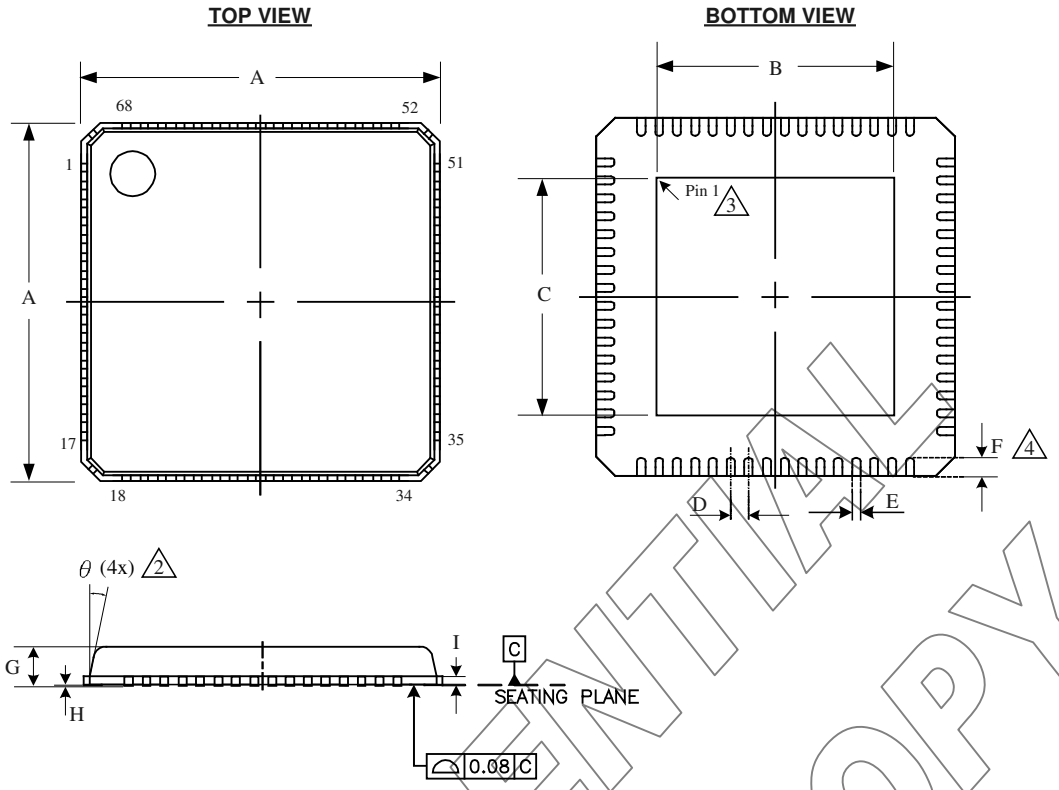

Figure 3: 68 Pin QFN Package (8 X 8 mm)

Table of Dimensions

No. of Leads		SYMBOL								
68 (8 X 8 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	7.90	5.45	5.45	0.40 BSC	0.15	0.30	0.80	0.00	0.20
	MAX	8.10	5.75	5.75		0.25	0.50	1.00	0.05	

Notes:

1. Conforms to JEDEC standard JESD-30 MO-220.

2 Side of body may be square or curved.

3 Exposed pad may have chamfer in area of Pin 1.

4 Pins may protrude from edge of body by 0.05 mm.

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ORDERING INFORMATION			
Part Number	**Package Type**	**Operating Temperature Range**	**Minimum Order Quantity**
CH7510A-BF	68QFN, Lead-free	Commercial : -20 to 70°C	260/TRAY

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