CH7515 4 Lane eDP to 4 Channel LVDS Monitor Controller

FEATURES

- Supports Embedded DisplayPort (eDP) Specification version 1.2.
- Support 4 Main Link Lanes at either 1.62Gb/s or 2.7Gb/s link rate
- Supports input color depth 6/8/10-bit per pixel in RGB format
- Support VESA and CEA timing standards up to QSXGA 2560x2048 @ 60Hz or 4Kx2K@24/30Hz for 2D, and Full HD 1920x1080 @120Hz for 3D(L/R eye frame at 60Hz each), with 10 bit graphic color depth
- Support eDP Authentication: Alternative Scramble Seed Reset (ASSR) and Alternative Framing
- Support Single Port, Dual Port and Quad port LVDS output interface with 6/8/10-bit color depth up to 400MHz pixel rate
- Support both OpenLDI (or JEIDA), SPWG (or VESA) and non-JEITA (10-bit only) bit mapping for LVDS application
- Flexible LVDS output pins swapping
- 2 channel IIS/ S/PDIF audio output
- Support Dynamic Backlight luminance Control by the command through AUX channel, or through the interface of PWM in/out and Backlight Brightness Control (OSD display)
- Support PWM bypass through and on-chip PWM generation
- Black panel during invalid input
- Support Panel selection function with external hardware configuration
- Initiated and controlled by firmware which is loaded from External BOOT ROM automatically upon power up.
- BOOT ROM data updated through I2C bus or AUX Channel
- Support dynamic refresh rate (DDR) switching
- Supports Enhanced Framing Mode
- 3 work modes: connect 27MHz crystal, inject 27MHz or 14.318MHz clock
- Programmable LCD panel power sequence
- Hot Plug Detection
- Support chip power down by GPIO pin
- Support power management mechanism through AUX Channel
- EMI reduction capability for DP input and LVDS output. Spread spectrum control is available for transmitting LVDS signal
- Achieve bit error rate $<10^{-9}$ for raw transport data per lane and symbol error rate $<10^{-12}$ for control data
- Low power consumption
- Offered in a 128-pin TQFP package (14 x 14mm)

GENERAL DESCRIPTION

Chrontel's CH7515 is a low-cost, low-power semiconductor device that translates the Embedded DisplayPort signal to the LVDS. This innovative eDP receiver with integrated 4 channel LVDS transmitters is specially designed to target the All-In-One PC and the terminal display devices with large size panel market segments. Leveraging the DisplayPort's unique source/sink "Link Training" routine, the CH7515 is capable of instantly bring up the video display to the LCD when the initialization process is completed between CH7515 and the graphic chip.

The CH7515 is designed to meet the Embedded DisplayPort Specification version 1.2. The 4 eDP Main Link Lanes receiver supports input with data rate running at either 1.62Gb/s or 2.7Gb/s, and can accept digital RGB signal for LVDS output up to QSXGA 2560x2048@60Hz or 4Kx2K@24/30Hz. With advanced 3D processing module integrated, The CH7515 can support up to 1920x1080@120Hz 3D display mode, with programmable emitter control signal and 3D LCD panel's backlight control signal output.

The Backlight Enable control and the PWM are the two kinds of backlight control functions designed in the CH7515 Panel power control module. The brightness control commands sent through AUX Channel can be dynamically translated by CH7515 and converted into LCD backlight control signal. Alternatively, the brightness control commands can be input from the PWM in and GOIO pin of Backlight Brightness Control. The CH7515 will save the last setting of brightness level into the external BOOT ROM and restore it upon power up. The CH7515 can dynamically adjust backlight brightness according to video stream to save power consumption and it supports OSD display in this way.

The CH7515 will immediately convert the Embedded DisplayPort signal to LVDS output after DisplayPort Link Training is completed. This feature can be achieved by loading the panel's EDID and the CH7515's configuration settings in the serial external BOOT ROM connected to the CH7515. During system power-up and upon completion of the DisplayPort Link Training through AUX Channel, CH7515 will generate LVDS signal according to the panel power-up timing sequencing stored in the external BOOT ROM.

An advanced Power Management Unit (PMU) is incorporated in CH7515, which is specially designed to reduce power consumption in normal operation.

APPLICATION

- All-In-One PC
- Terminal Display Devices

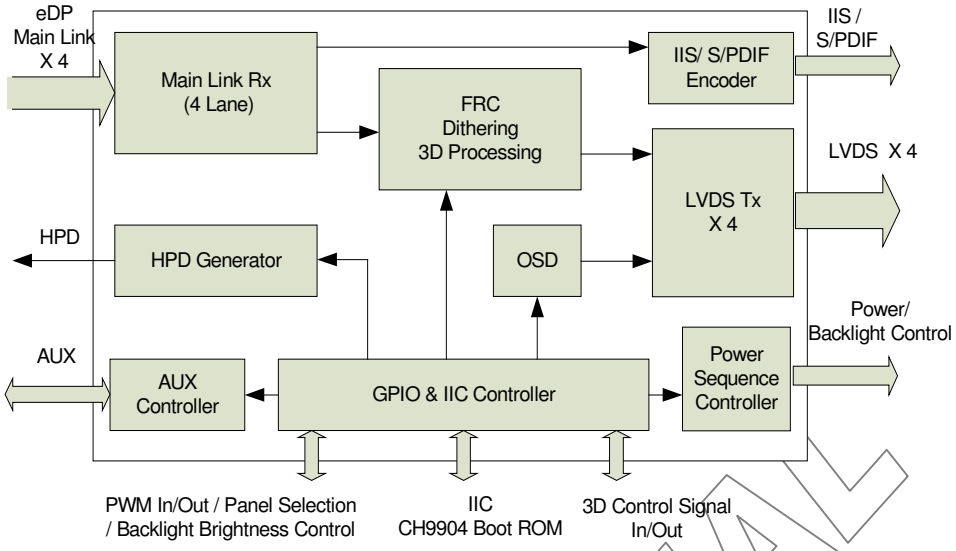

Figure 1: CH7515 Functional Block Diagram

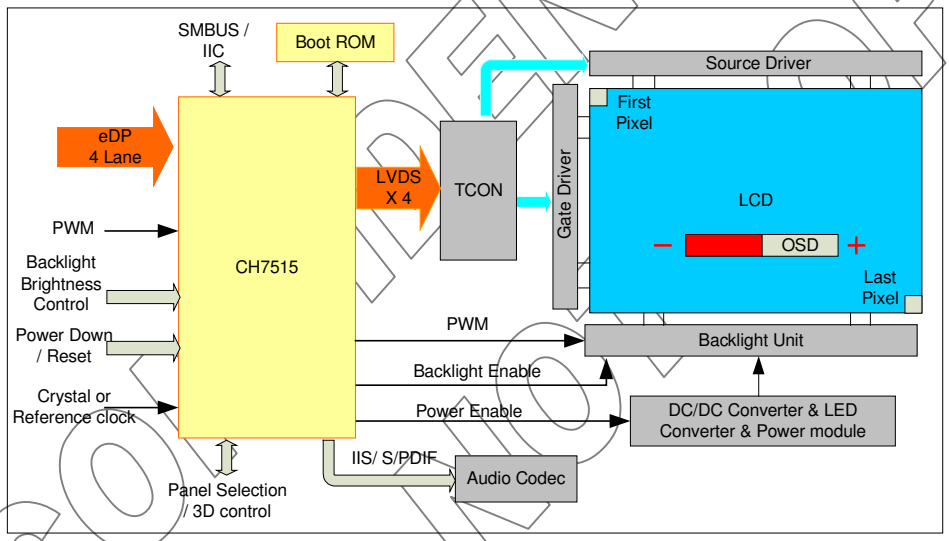

Figure 2: CH7515 Application Diagram

1.0 PIN-OUT

1.1 Package Diagram

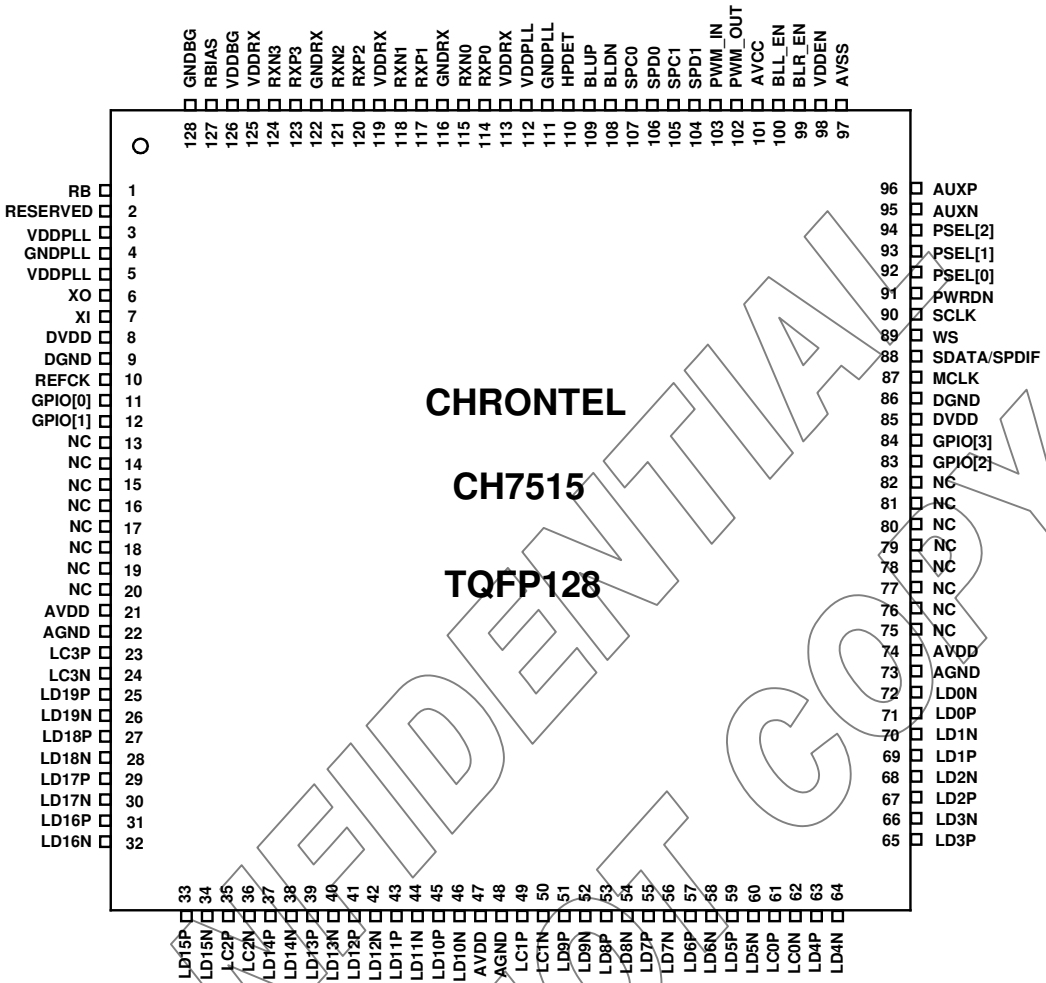

Figure 3: CH7515 128-Pin TQFP Pin Out

1.2 Pin Description

Table 1: CH7515 Pin Description

Pin #	Type	Symbol	Description
1	In	RB	**Reset* Input (Internal pull-up)** When this pin is pull low, the device is held in the power-on reset condition. When this pin is pull high, reset is controlled through the serial port register.
2		RESERVED	**Reserved Pin**
6,7	In	XO, XI	**27MHz Crystal Input**
10	In	REFCK	**Clock Input** This pin is used as clock input pin when injecting 27MHz/14.318MHz clock to CH7515
11,12,83,84	In/Out	GPIO[3:0]	**General Purpose Input/Output**
13~20,75~82		NC	**Not Connected**
23~34	Out	LC3P/N, LD19P/N~LD15P/N	**The Fourth Channel LVDS Output**
35~46	Out	LC2P/N, LD14P/N~LD10P/N	**The Third Channel LVDS Output**
49~60	Out	LC1P/N, LD9P/N~LD5P/N	**The Second Channel LVDS Output**
61~72	Out	LC0P/N, LD4P/N~LD0P/N	**The First Channel LVDS Output**
87	Out	MCLK	**I2S Master Clock Output**
88	Out	SDATA	**I2S Data Output**
	Out	SPDIF	**S/PDIF Output**
89	Out	WS	**I2S Word Select**
90	Out	SCLK	**I2S Clock Output**
91	In	PWRDN	**Power Down Control** CH7515 enters/exit power down state when receiving active low pulse from this pin
92~94	In	PSEL[2:0]	**LVDS Panel Selection** These pins should be pull-up or pull-down in the application, instead of floating.
95~96	In/Out	AUXN/P	**Aux channel differential input/output** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal**.**
98	Out	VDDEN	**LCD Panel VCC Enable**
99	Out	BKLR_EN	**LCD Panel Right Eye Backlight Enable in 3D Mode** **LCD Panel Backlight Enable in 2D Mode**
100	Out	BKLL_EN	**LCD Panel Left Eye Backlight Enable**
102	Out	PWM_OUT	**PWM output for backlight brightness dimming**
103	In	PWM_IN	**Backlight brightness PWM input**
104	In/Out	SPD1	**Serial Port Data Input/Output for Chip BOOT ROM/EDID/HDCP ROM** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4kΩ - 9 kΩ pull up resistor to 3.3V.
105	Out	SPC1	**Serial Port Clock Output for Chip BOOT ROM/EDID/HDCP ROM**

			This pin functions as the clock output of the serial port and operates with output from 0 to 3.3V. This pin requires an external 4kΩ - 9kΩ pull up resistor to 3.3V.
106	In/Out	SPD0	**Serial Port Data Input / Output for CH7515 I2C Slave** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to 3.3V. Outputs are driven from 0 to 3.3V. This pin requires an external 4kΩ - 9 kΩ pull up resistor to 3.3V. CH7515 serial port device address is 0x21 and transmitted in SPD as following(MSB transmitted first) B7 B6 B5 B4 B3 B2 B1 B0 0 1 0 0 0 0 1 R/W
107	In	SPC0	**Serial Port Clock Input for CH7515 I2C Slave** This pin functions as the clock input of the serial port and operates with inputs from 0 to 3.3V. This pin requires an external 4kΩ - 9kΩ pull up resistor to 3.3V.
108	In	BLDN	**Decrement Backlight Brightness Input**
109	In	BLUP	**Increment Backlight Brightness Input**
110	Out	HPDET	**Hot Plug Detect** This output pin indicates whether this device is active or not. It also generates interrupt pulse as defined by eDP standard. Output voltage is 3.3v.
114,115	In	RXP0, RXN0	**Embedded DisplayPort Lane 0 input** One pair of differential data input. It handles clock-embedded high speed differential data input as eDP standard
117,118	In	RXP1, RXN1	**Embedded DisplayPort Lane 1 input** One pair of differential data input. It handles clock-embedded high speed differential data input as eDP standard
120,121	In	RXP2, RXN2	**Embedded DisplayPort Lane 2 input** One pair of differential data input. It handles clock-embedded high speed differential data input as eDP standard
123,124	In	RXP3, RXN3	**Embedded DisplayPort Lane 3 input** One pair of differential data input. It handles clock-embedded high speed differential data input as eDP standard
127	In	RBIAS	**Band-gap Bias**
3,5,112	Power	VDDPLL	**PLL Power Supply (1.8V)**
4,111	Power	GNDPLL	**PLL Ground**
8,85	Power	DVDD	**Digital Power Supply (1.8V)**
9,86,88	Power	DGND	**Digital Power Ground**
21,47,74	Power	AVDD	**LVDS Power Supply (3.3V)**
22,48,73	Power	AGND	**LVDS Power Ground**
97	Power	AVSS	**Analog Ground**
101	Power	AVCC	**Analog Power Supply (3.3V)**
113,119,125	Power	VDDRX	**eDP Rx Power Supply (1.8V)**
116,122	Power	GNDRX	**eDP Rx Power Ground**
126	Power	VDDBG	**Band-gap Power Supply (1.8V)**
128	Power	GNDBG	**Band-gap Ground**

2.0 PACKAGE DIMENSIONS

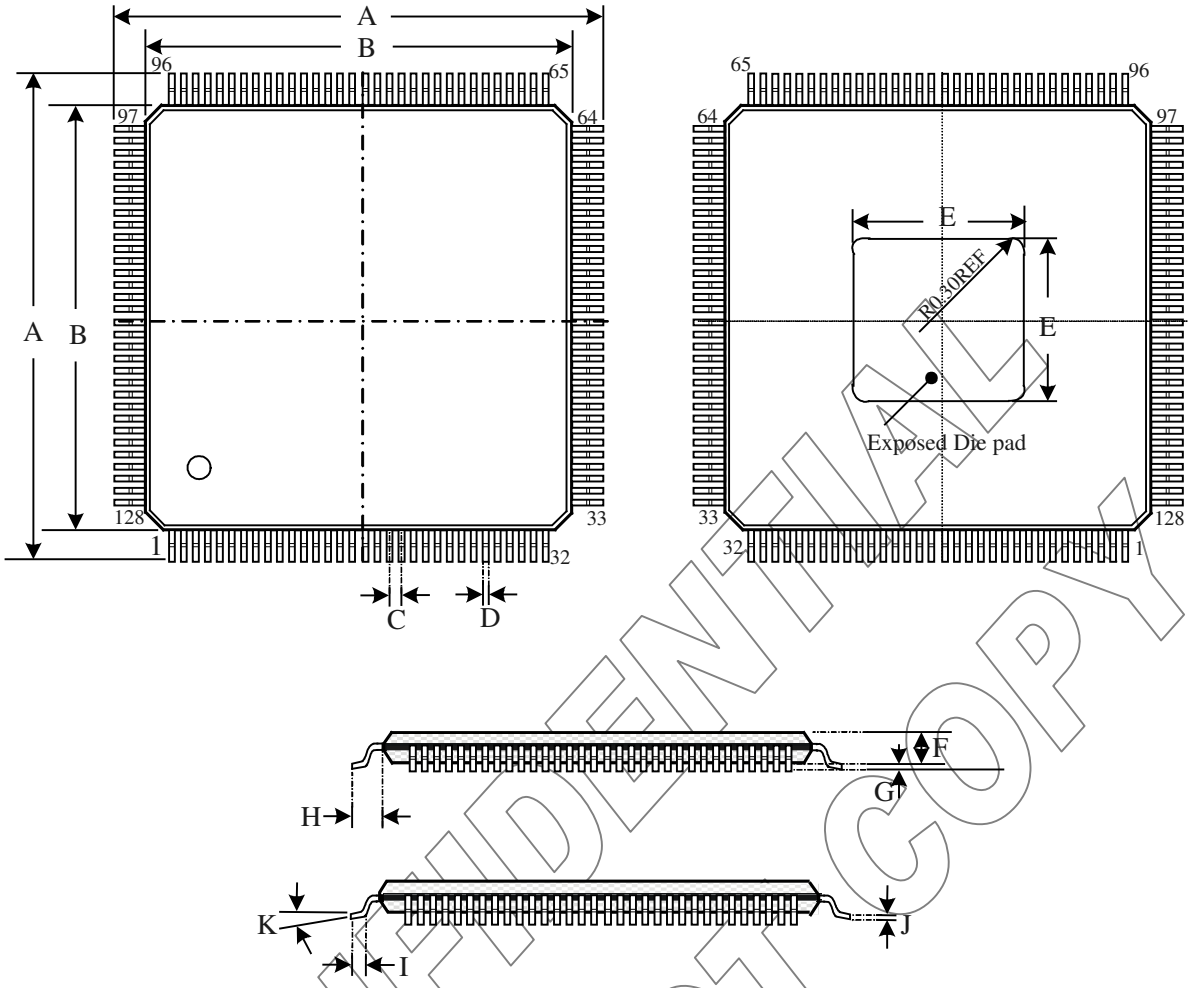

Figure 4: 128 pin TQFP package (14 X 14 mm)

Table of Dimensions

No. of Leads		SYMBOL										
128 (14 X 14 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli-meters	MIN	15.85	13.90	0.35	0.13	5.30	0.95	0.05	0.85	0.45	0.09	0°
	MAX	16.15	14.10	0.45	0.23	6.35	1.05	0.15	1.15	0.75	0.20	7°

Notes:
Conforms to JEDEC standard JESD-30 MO-220.

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ORDERING INFORMATION			
Part Number	**Package Type**	**Operating Temperature Range**	**Minimum Order Quantity**
CH7515A-TF	128 TQFP, Lead-free	Commercial: 0 to 70°C	90/Tray

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