Video Multiplexer with Source Control

Features

- Triple 8-bit DAC and buffers support 1280 x 1024 display resolution
- High-speed multiplexing between digital and analog RGB signals
- 24-bit digital RGB interface supports up to 16.7 million colors
- Supports CCIR601 4:2:2 YCrCb input formats
- Built in YUV-to-RGB color space conversion
- Analog auxiliary inputs with programmable input attenuation
- 2's complement input capability on Red and Blue channels, supporting 4:4:4 YUV format with analog YUV outputs
- Programmable brightness, contrast, and hue attributes for the digital input signals
- Programmable switching delay
- Two-wire serial programming
- Enhanced replacement of STV8438
- CMOS technology in 44-pin PQFP
- 5V supply

Description

Chrontel's CH8438 combines a 24-bit digital video interface, YUV to RGB converter, three 8-bit DACs, a high-speed analog multiplexer, an analog input attenuator, and three video buffers in one integrated circuit.

The CH8438's high-speed analog multiplexer allows simultaneous display of video (digital RGB) with graphics (analog RGB), making CH8438 ideal for video games, editing, PC video, and for applications requiring picture-in-picture capability.

CH8438 provides a 24-bit digital pixel bus interface, which supports RGB, 4:4:4 YUV and 4:2:2 YCrCb input formats. With the 4:2:2 YCrCb input format, a built-in color space converter translates YUV video information to RGB before muxing with the analog graphics input, while the 4:4:4 YUV format accepts 2's complement Red and Blue data, and provides analog YUV outputs.

CH8438 has seven 4-bit control registers which are programmable with the serial interface pins. The programmable functions include digital input formats; video attributes of contrast, hue, and brightness; analog input attenuation; and switching delay.

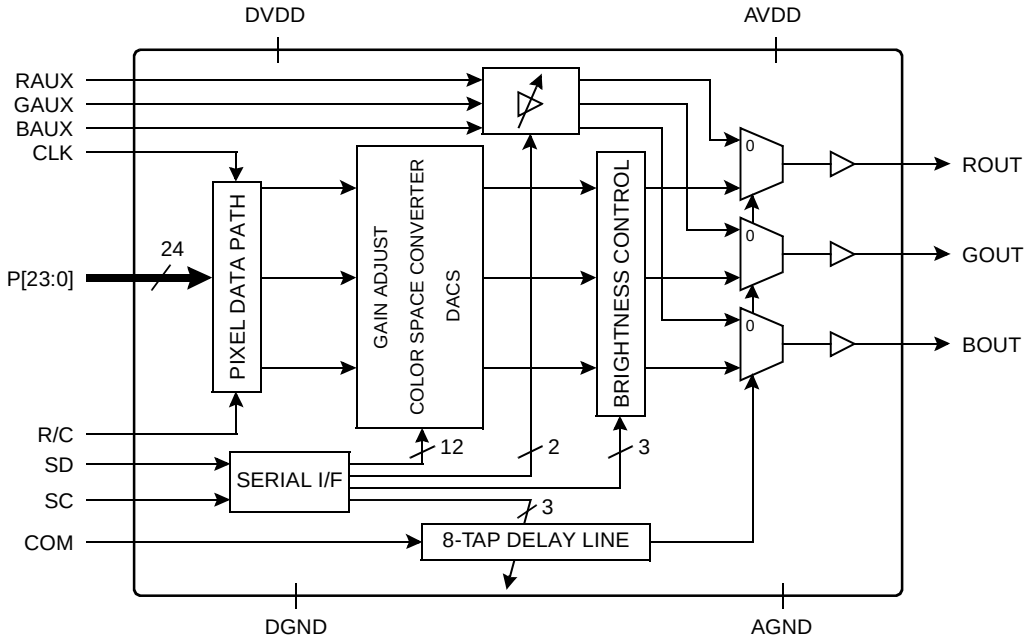


Figure 1: CH8438 Block Diagram

Table 1 • Pin Description

Pin	Type	Symbol	Description
1 – 12, 29 – 36, 41 – 44	In	P11 - P0, P23 – P16, P15 – P12	**Pixel Data Input.** Digital video interface supports the following input formats: RGB, 4:4:4 YCrCb, and four 4:2:2 YCrCb modes.
13, 15, 26	Power	AVDD	**Analog 5V Supply**
14, 16, 20, 23	Power	AGND	**Analog Ground**
17	In	SC	**Serial Clock.** This input clocks Serial Data for loading the control registers. Serial input has an internal pull-up.
18	Out	ROUT	**Analog Output**, channel R
19	In	RAUX	**Auxiliary Analog Input**, channel R
21	Out	GOUT	**Analog Output**, channel G
22	In	GAUX	**Auxiliary Analog Input**, channel G
24	Out	BOUT	**Analog Output**, channel B
25	In	BAUX	**Auxiliary Analog Input**, channel B
27	Power	DGND	**Digital Ground**
28	Power	DVDD	**Digital 5V Supply**
37	In	R/C (HREF)	Refer to **"Digital Input Format"** on page 9 and **"Display Modes"** on page 10 for more information. R/C input has an internal pull-up.
38	In	CLK	**Clock Input.** The digital inputs are sampled on the rising edge of this input.
39	In	SD	**Serial Data.** Refer to **"Serial Port Programming"** on page 11 for more information. Serial Data input has an internal pull-up.
40	In	COM	**Multiplexer Control Input.** This input controls the multiplexer to pass the auxiliary analog inputs or the internal digital channel to the output buffers. COM = 0 connects auxiliary analog input to output buffer COM = 1 connects internal digital channel to output buffer

General Description (continued)

Analog Outputs

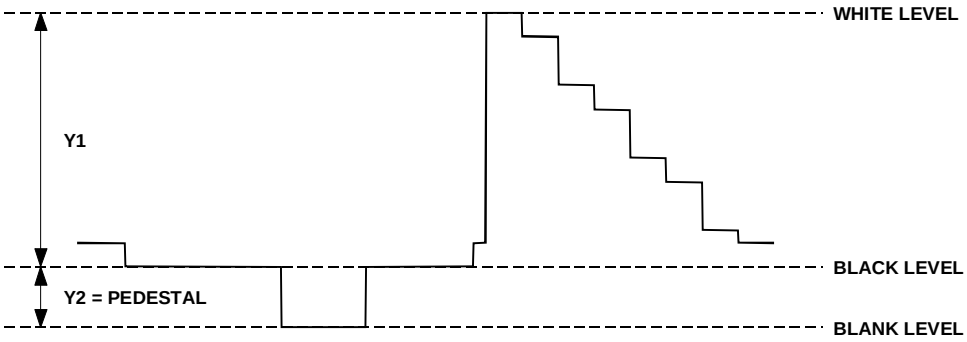
The analog RGB or YUV outputs consist of low impedance, wide-band output buffers designed to drive 75 Ω transmission lines and 75 Ω-terminated color monitors, as shown in **Figure 11** on page 20. The default and maximum voltage levels at these outputs are shown in **Table 2** below.

Table 2 • Analog Output of Digital RGB Signal

Color/Level	Default Value (V)	Max Setting (V)†
White	0.66	0.970
Blank/Black	0.00	0.164

Note: † Digital input gain and brightness control registers are set at maximum settings

4(a) Auxiliary Analog Input with blank pedestal



4(b) Analog Output

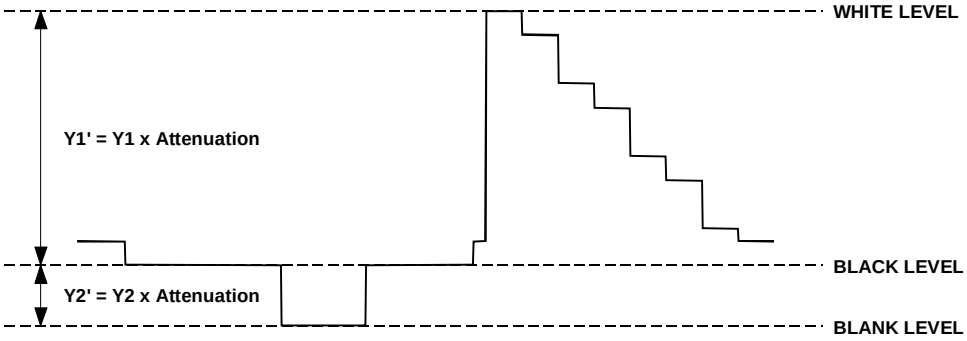


Figure 4: Analog Input and Output Waveforms (with blank pedestal)

Digital Input Format

CH8438 supports six different digital input formats (modes) summarized in **Table 3** below. The six modes include 24-bit True-Color RGB format (RGB output), 4:4:4 YCrCb format (YUV output) and four 4:2:2 YCrCb formats (with color space conversion to provide RGB output).

Table 3 • Mode Table

MODE	FORMAT	Register R6 (DIF[3:0])	R/C	Number of Pipeline Clock Cycles†
0	RGB	0000	1	0
1	4:4:4	0000 0001	0 X	0
2	4:2:2	0010	HREF	5
3	4:2:2	0011	HREF	5
4	4:2:2	0100	HREF	5
5	4:2:2	0101	HREF	5

Note: † See **Figure 7** on page 18 for an example of the on-chip DAC inputs transition after five pipeline clock cycles

The function of pin R/C changes in modes 2 – 5, becoming the input pin for the signal HREF. In modes 2 – 5, HREF and P[23:0] are clocked by the rising edge of CLK. When HREF (pin R/C) is set high, the rising edge of CLK clocks in the first 16 bits [Y0 and U0(Cb)] of the YUV 4:2:2 data. The output is blanked when HREF = 0 is clocked in. For more detailed information, please refer to **Figure 9** on page 19.

In mode 1, the U-data path is identical to the V-data path, therefore, P[23:16] can be used as the "V" inputs and P[7:0] can be used as the "U" inputs, as shown in **Table 4** below.

Table 4 • Pixel Data Organization

MODE	P[23:16]								P[15:8]								P[7:0]							
	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
0	B7	B6	B5	B4	B3	B2	B1	B0	G7	G6	G5	G4	G3	G2	G1	G0	R7	R6	R5	R4	R3	R2	R1	R0
1	U7	U6	U5	U4	U3	U2	U1	U0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	V7	V6	V5	V4	V3	V2	V1	V0
2	Y7	Y6	Y5	Y4	Y3				Y2	Y1	Y0	C7	C6	C5			C4	C3	C2	C1	C0			
3	C7	C6	C5	C4	C3				C2	C1	C0	Y7	Y6	Y5			Y4	Y3	Y2	Y1	Y0			
4	C4	C3	C2	C1	C0			Y7	Y1	Y0	C7	C6	C5				Y6	Y5	Y4	Y3	Y2			
5									Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	C7	C6	C5	C4	C3	C2	C1	C0

Serial Port Programming

The CH8438 control registers can be downloaded through the two-wire serial port. This is a write only port with the transfer protocol shown in **Figure 10** on page 19. Each data packet consists of a start, a 3-bit address followed by a "0," 4 bits of data, and a stop.

The transfer sequence is initiated when a high-to-low transition of serial data ("SD") occurs while serial clock ("SC") is high. Similarly, the transfer sequence is terminated when a low-to-high transition of SD occurs while SC is high. The transitions of the address and data bits can only occur when SC is in a low state.

SC and SD can be connected to a microcontroller or a video controller's programmable I/O pins. For more information, refer to Application Note 18 (AN-18) "Programming the CH8438".

Control Registers

CH8438 contains seven 4-bit control registers which provide access to basic video attribute control functions. These registers are accessible via the address bits, A[2:0]. The following sections describe the functions and the controls available through these registers.

Table 7 • Register Map

Register	Default Value	Address			Description
R0	0H	0	0	0	Multiplexer Delay control register
R1	0H	0	0	1	Digital Video Brightness control register
R2	8H	0	1	0	Red or V Digital Input Gain control register
R3	8H	0	1	1	Green or Y Digital Input Gain control register
R4	8H	1	0	0	Blue or U Digital Input Gain control register
R5	0H	1	0	1	Analog Input Attenuation control register
R6	0H	1	1	0	Digital Input Format control register
RTEST	0H	1	1	1	Reserved

Table 8 • Control Register Summary

Register	Address			Register Data			
	A2	A1	A0	D3	D2	D1	D0
R0	0	0	0	0	MDS2	MDS1	MDS0
R1	0	0	1	PS	DVB2	DVB1	DVB0
R2	0	1	0	RV_G3	RV_G2	RV_G1	RV_G0
R3	0	1	1	GY_G3	GY_G2	GY_G1	GY_G0
R4	1	0	0	BU_G3	BU_G2	BU_G1	BU_G0
R5	1	0	1	0	0	AA1	AA0
R6	1	1	0	COM_INV	DIF2	DIF1	DIF0
RTEST	1	1	1	0	0	0	0

Note: All "0" values of register data D[3:0] shown in table above must be programmed to "0" for proper operation of the device.

Register Descriptions (continued)

R2: Red or V Digital Input Gain Control Register

D3	D2	D1	D0
RV_G3	RV_G2	RV_G1	RV_G0

The initial value of this register upon power-up is 1000

RV_G[3:0] = Digital Input Gain

Mode 0: These bits select the gain applied to the digital red input

Modes 1, 2, 3, 4, 5: These bits select the gain applied to the digital V inputs

For detailed information, please refer to **Table 9** on page 15.

R3: Green or Y Digital Input Gain Control Register

D3	D2	D1	D0
GY_G3	GY_G2	GY_G1	GY_G0

The initial value of this register upon power-up is 1000

GY_G[3:0] = Digital Input Gain

Mode 0: These bits select the gain applied to the digital green input

Modes 1, 2, 3, 4, 5: These bits select the gain applied to the digital Y inputs

For detailed information, please refer to **Table 9** on page 15.

R4: Blue or U Digital Input Gain Control Register

D3	D2	D1	D0
BU_G3	BU_G2	BU_G1	BU_G0

The initial value of this register upon power-up is 1000

BU_G[3:0] = Digital Input Gain

Mode 0: These bits select the gain applied to the digital blue input

Modes 1, 2, 3, 4, 5: These bits select the gain applied to the digital U inputs

For detailed information, please refer to **Table 9** on page 15.

Table 9 • Digital Input Gain Control

G3	G2	G1	G0	Full-Scale Output Voltage (Volts) †
0	0	0	0	0.66 – 25%
0	0	0	1	. . .
0	0	1	0	. . .
0	0	1	1	. . .
0	1	0	0	. . .
0	1	0	1	. . .
0	1	1	0	. . .
0	1	1	1	. . .
1	0	0	0	0.66
1	0	0	1	. . .
1	0	1	0	. . .
1	0	1	1	. . .
1	1	0	0	. . .
1	1	0	1	. . .
1	1	1	0	. . .
1	1	1	1	0.66 + 22%

Note: † Assumes 75Ω-terminated color monitor

Electrical Specifications (continued)

Table 14 • Analog Outputs (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ± 5%)

Symbol	Description	Test Condition @ T_A = 25°C	Min	Typ	Max	Units
PSRR	Power supply rejection ratio				0.5	% / % V_{DD}

Table 15 • AC Characteristics

Symbol	Description	Min	Typ	Max	Units
t_1	CLK to COM relative timing			5	ns
t_2	CLK to DAC output delay	6.5		17	ns
t_3	CLK to Analog Mux Switch Control delay[1]	5.5		18.5	ns
t_4	CLK to pixel data setup requirement	3			ns
t_5	CLK to pixel data hold requirement	2.5			ns
t_6	SD transition to SC falling edge	5			ns
t_7	SD data setup time	5			ns
t_8	SD hold time from SC falling edge	5			ns
t_9	SD transition from SC rising edge	5			ns
T_{sc}	SC serial clock period	50			ns
I_{DD}	V_{DD} supply current		135	180	mA
I_{DD_PS}	Power Saver V_{DD} supply current		2[2]		mA

Note: 1 These limits are for multiplexer delay control register R0[2:0] = 000. For other R0 settings, the limits are obtained by adding the difference in nominal multiplexer delay to the limits for R0[2:0] = 000.

Note: 2 This value is untested

Test Conditions: Unless otherwise specified, the testing conditions are the same as in **Table 11, "Recommended Operating Conditions,"** on page 16. TTL input values are 0 – 3V, with input rise / fall times < 3 ns, measured between the V_{IL} and V_{IH}. Timing reference points at 50% for non-TTL inputs and outputs. TTL reference points at 1.5V for inputs and outputs. Analog output load < 10 pF.

Timing Diagrams (continued)

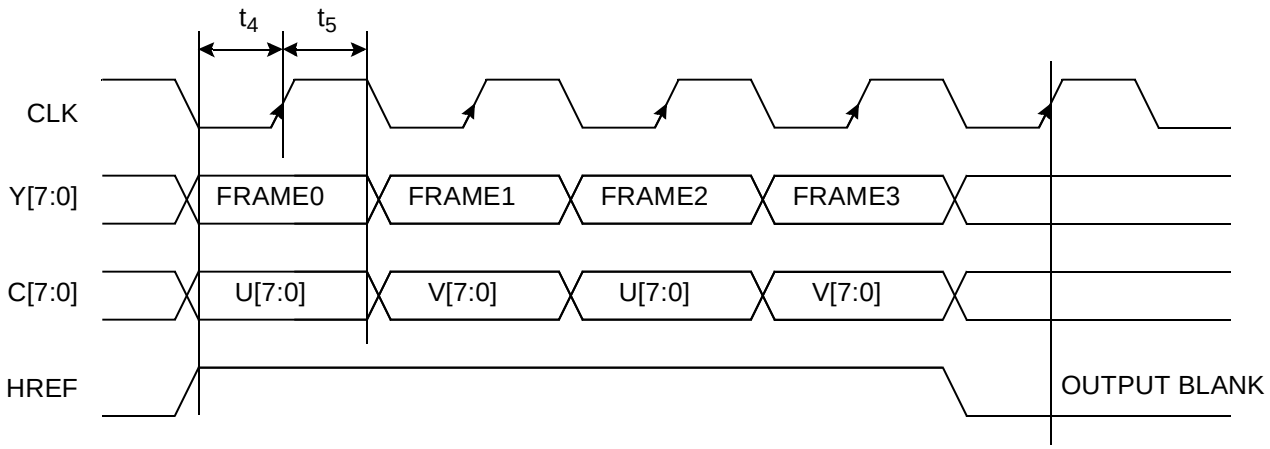


Figure 9: 4:2:2 YCrCb Input Data Timing

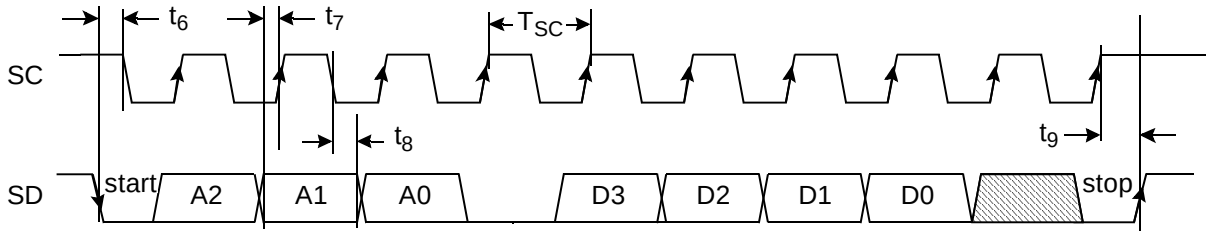


Figure 10: Serial Port Transfer Protocol

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH8438-QA	PQFP 10 x 10 mm	44	5V
CH8438-QB	PQFP 14 x 14 mm	44	5V

Note: For new designs, use the 10 x 10 mm package part. The 14 x 14 mm package will be phased out.

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