



## Dual Graphics Clock Generator

### Features

- Generates 16 preset video clocks, 8 preset memory clocks, and buffers the reference frequency output
- Built-in power supply conditioning circuitry provides excellent jitter performance and eliminates the need for an external VDD dropping resistor
- Requires only two external components: one 14.318 MHz crystal and one 0.1  $\mu\text{F}$  decoupling capacitor
- Supports VGA, Super-VGA, XGA™, and 8514 graphic standards
- Supports output frequencies up to 135 MHz
- Drop-in replacement for ICS2494 and AV9194
- CMOS technology in 20-pin PDIP and SOIC
- 5V or 3.3V supply. For specific details on the 3.3V version, please consult Chrontel.

### Description

CH9294 is a dual PLL clock generator designed for high frequency graphics applications. It can also be used in applications requiring multiple clocks, such as PC motherboards, disk drives, CD-ROM systems, and modems.

The CH9294 provides separate memory clock (MCLK) and video clock (VCLK) outputs, and a 14.318 MHz reference clock output. Other input frequencies can be used to obtain different output frequencies. Internal loop filter elements minimize external part count.

The STROBE pin should be tied high or left open if not used. FSx pins are latched on the falling edge of STROBE.

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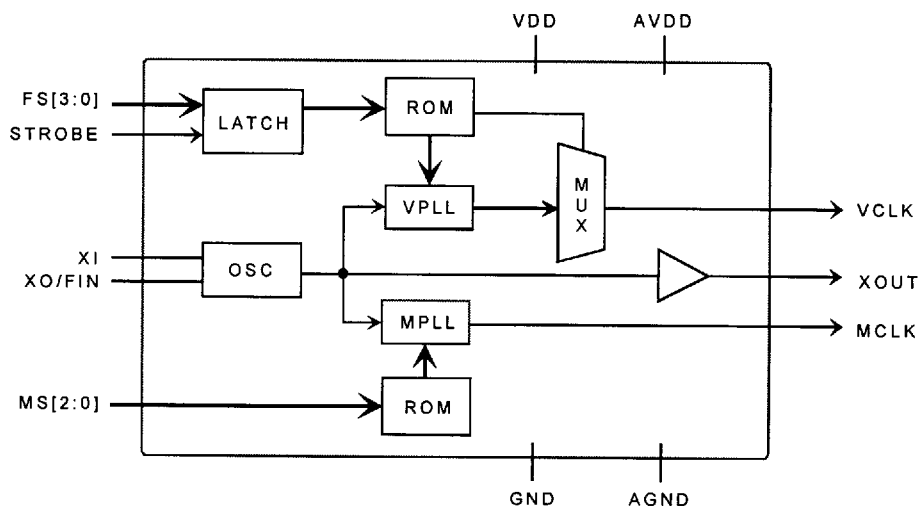


Figure 1: Block Diagram

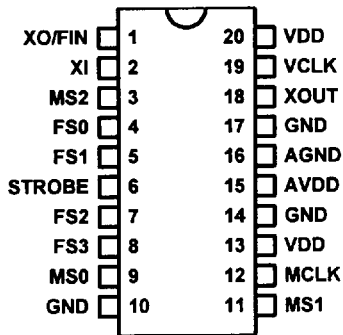


Figure 2: CH9294E and G

Table 1 • Pin Description CH9294E and G

Pin	Type	Symbol	Description
1	Out / In	XO / FIN	Crystal output or external FREF input
2	In	XI	Crystal input
3	In	MS2	Memory clock select 2 (MS2 is internal pull-down for Version E and internal pull-up for Version G)
4, 5, 7, 8	In	FS0, FS1, FS2, FS3	Video frequency clock select (internal pull-up)
6	In	STROBE	FS0 through FS3 strobe input (internal pull-up)
9, 11	In	MS0, MS1	Memory clock select (internal pull-up)
10, 14, 17	Power	GND	Ground
12	Out	MCLK	Memory clock output
13, 20	Power	VDD	5V supply
15	Power	AVDD	Analog 5V supply
16	Power	AGND	Analog ground
18	Out	XOUT	Buffered reference (14.318 MHz) frequency output
19	Out	VCLK	Video clock output

Table 2 • Frequencies for CH9294E and G (in MHz)

## Video Clock

Frequency Select (FS)				VCLK	
FS3	FS2	FS1	FS0	Version E	Version G
0	0	0	0	50.35	25.18
0	0	0	1	56.65	28.32
0	0	1	0	65.0	40.0
0	0	1	1	72.0	72.0
0	1	0	0	80.0	50.0
0	1	0	1	89.8	77.0
0	1	1	0	63.0	36.0
0	1	1	1	75.0	44.9
1	0	0	0	25.18	130.0
1	0	0	1	28.32	120.0
1	0	1	0	31.5	80.0
1	0	1	1	36.0	31.5
1	1	0	0	40.0	110.0
1	1	0	1	44.9	65.0
1	1	1	0	50.0	75.0
1	1	1	1	65.0 (default)	94.5 (default)

Note: Consult Chronitel for other standard frequency table versions, exact output frequencies, and details about available custom patterns

## Memory Clock

Memory Select (MS)			MCLK	
MS2	MS1	MS0	Version E	Version G
0	0	0	40.0	55.0
0	0	1	41.61	65.0
0	1	0	44.74	70.0
0	1	1	50.0 (default)	80.0
1	0	0	52.5	45.0
1	0	1	55.0	40.0
1	1	0	57.5	60.0
1	1	1	60.0	50.0 (default)

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**Table 3 • Absolute Maximum Ratings**

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	-0.5 to +7.0	V
VIN	Input voltage on any pins with respect to GND	-0.5 to VDD +0.5	V
TSTOR	Storage temperature	-55 to +150	°C

**Note:** Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 4 • DC Specifications (Operating Conditions: TA = 0°C - 70°C, VDD = 5V ±5%)**

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 4.75V, IOH = 4mA	2.4			V
VOL	Output low voltage	VDD = 4.75V, IOL = 8mA			0.4	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			5	20	µA
ILK	Input leakage current		-10		10	µA
IDD	Operating current	VDD = 5V VCLK = 50MHz, No load MCLK = 55MHz, No load		45		mA

**Table 5 • AC Specifications (Operating Conditions: TA = 0°C - 70°C, VDD = 5V ±5%)**

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FIN	Crystal / FREF input			14.318		MHz
TSU	Setup time, data to strobe		25			ns
THOLD	Hold time, strobe to data		25			ns
TSTROBE	Strobe pulse width		50			ns
VCLK	Video clock frequency		8		135	MHz *
MCLK	Memory clock frequency		8		135	MHz *
TR	Output clock rise time	CL = 25pF, VOL - VOH		2		ns
TF	Output clock fall time	CL = 25pF, VOL - VOH		2		ns
TDC	Output clock duty cycle	VDD = 5V @VDD / 2	40	50	60	%

**Note:** \* Output levels are guaranteed up to 90 MHz. Please consult ChronTEL for suggested circuit implementations for frequencies higher than 90 MHz

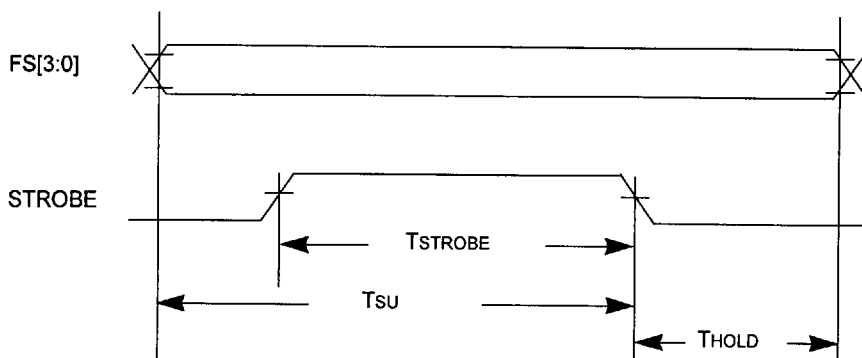


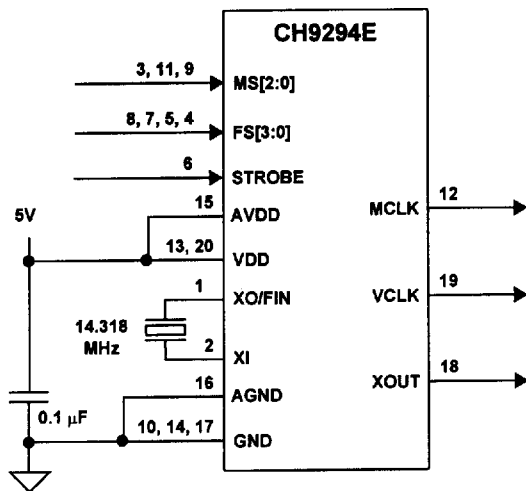
Figure 3: Strobe Timing Diagram

### Layout Considerations

To minimize phase noise and maximize performance, the following layout guidelines are recommended:

- Place all power supply bypass capacitors in close proximity to their respective power pins
- Use a ground plane to connect GND, AGND, and all external component grounds
- Avoid running any signal lines through the synthesizer section of the board

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**Figure 4: Application Schematic**

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ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9294x-N	300 mil PDIP	20	5V
CH9294x-S	300 mil SOIC	20	5V
<b>Note:</b> x = frequency table version			