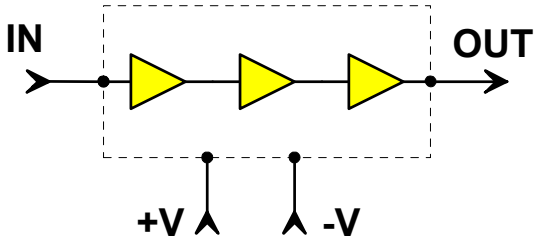
W-band Low Noise Amplifier

Preliminary

GaAs Monolithic Microwave IC

Description

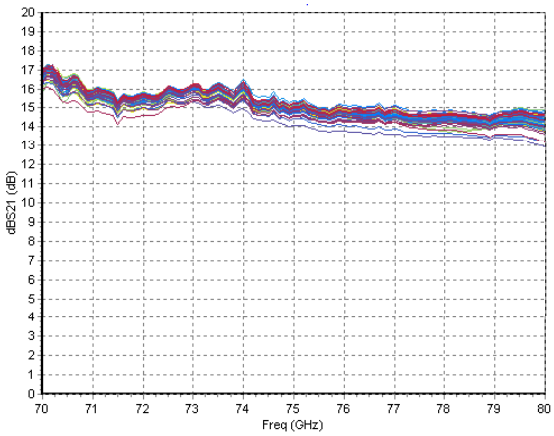
The CHA1077a is a W-band monolithic 3-stages low noise amplifier. All the active devices are internally self-biased. This chip is compatible with automatic equipment for assembly.
The circuit is manufactured on P-HEMT process: 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



W-band amplifier block-diagram

Main Features

- W-band low noise amplifier
- High gain
- Wide operating frequency range
- High temperature range
- On-chip self biasing
- Additional external resistor allows to choose getting more gain instead of a minimum noise factor
- Automatic assembly oriented
- Low DC power consumption
- BCB layer protection
- Chip size: 2.6 x 1.32 x 0.1mm



Small signal gain

Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating frequency	76		77	GHz
G_lin	Small signal gain		15		dB
NF	Noise figure		4.5		dB
P_1dB	Output power at 1dB gain compression		9		dBm

ESD Protections : Electrostatic discharge sensitive device observe handling precautions !

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Electrical Characteristics

Full operating temperature range, used according to section "Typical assembly and bias configuration".

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating frequency	76		77	GHz
G_lin	Small signal gain	11	15	19	dB
G_fl	Small signal gain flatness		0.5	1	dB
NF	Noise figure		4.5	6.5	dB
P_out_1dB	Output power at 1dB gain compression	6	9		dBm
Is	Reverse isolation	20	30		dB
VSWR_in	VSWR at input port (50Ω)		2:1	2.5:1	
VSWR_out	VSWR at output port (50Ω)		2:1	2.5:1	
+V	Positive supply voltage (1)	4.4	4.5	4.6	V
+I	Positive supply current		40	70	mA
-V	Negative supply voltage (1)	-4.6	-4.5	-4.4	V
-I	Negative supply current	-10	-6	0	mA
Top	Operating temperature range	-40		100	°C

(1) Negative supply voltage must be applied at least 1us before positive supply voltage.

Absolute Maximum Ratings (1)

Symbol	Parameter	Values	Unit
P_in	Maximum input power (2)	3	dBm
+V	Positive supply voltage	5	V
-V	Negative supply voltage	-5	V
+I	Positive supply current	80	mA
-I	Negative supply current	-13	mA
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) CW mode

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Chip Mechanical Data and Pin References

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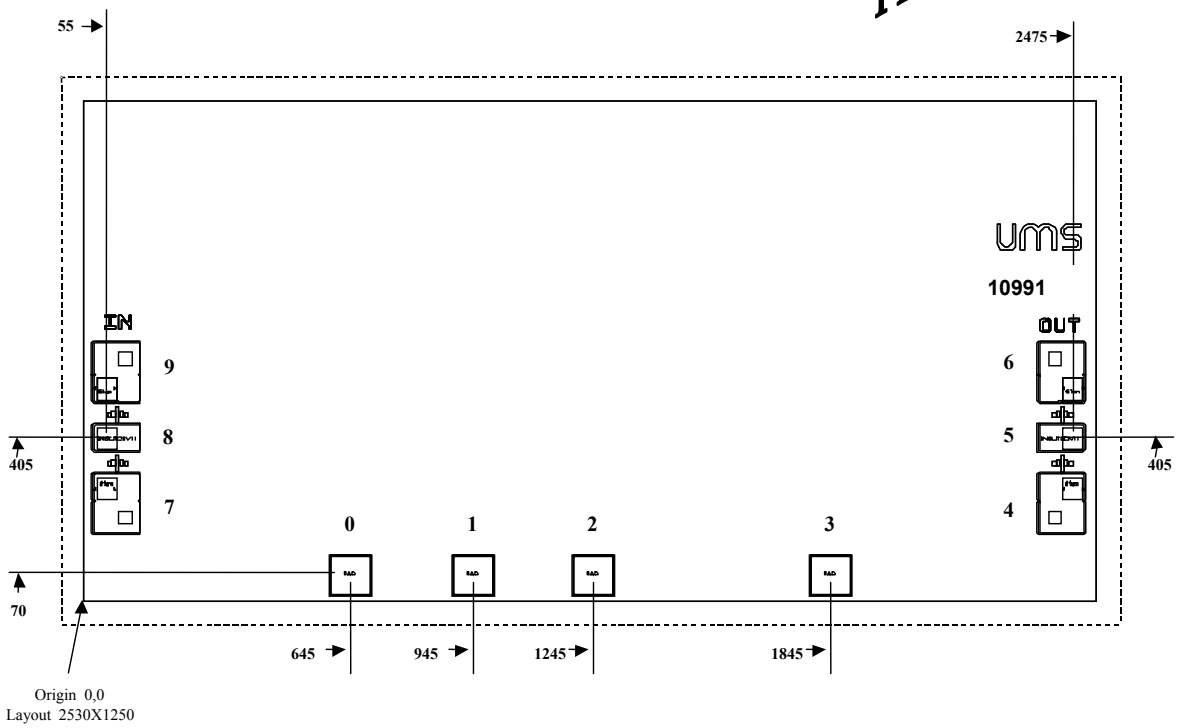

Unit = µm
External chip size (layout size + dicing streets) = 2600X1320 +/-35
Chip thickness = 100 +/- 10
HF Pads (5,8) = 105 X 86 (BCB opening)
DC/IF Pads = 86 x 83 (BCB opening)

Pin number	Pin name	Description
4, 6, 7, 9		Ground: should not be bonded. If required, please ask for more information.
3		Ground (optional)
5	**OUT**	RF output port
8	**IN**	RF input port
0	**+V**	Positive supply voltage
1	**-V1**	Negative supply voltage for the first stage
2	**-V23**	Negative supply voltage for the second and third stage

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Typical Assembly and Bias Configuration to get minimum noise figure :

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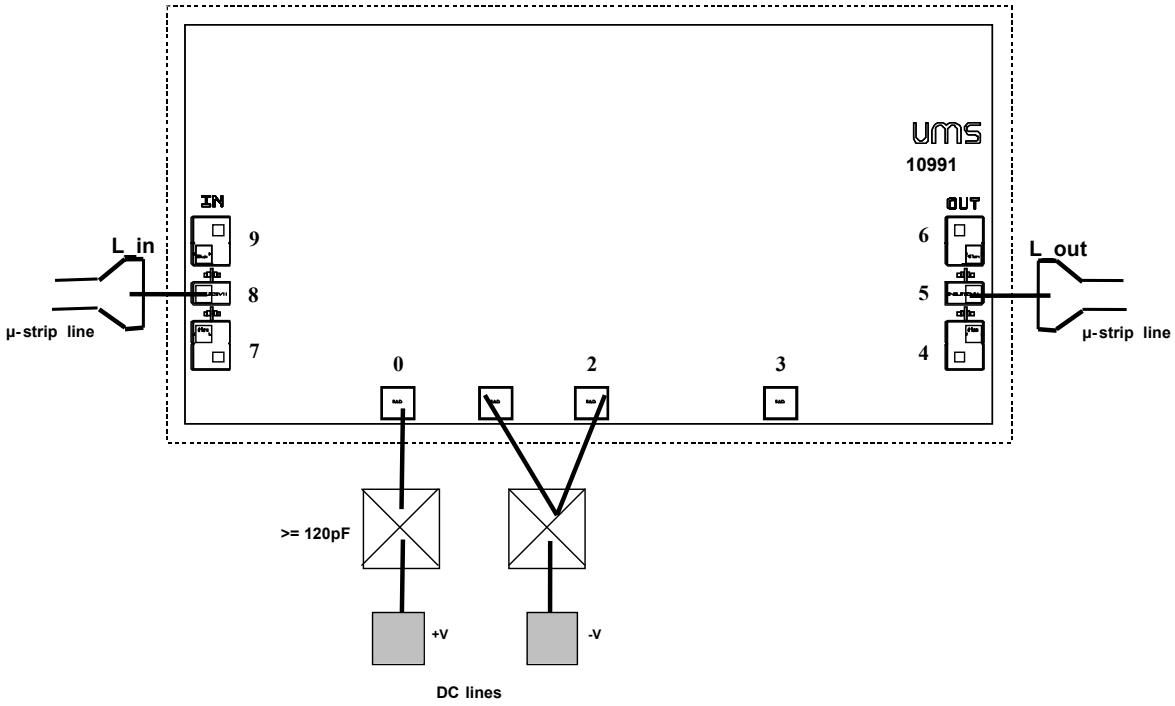

This drawing shows an example of assembly and bias configuration. All the transistors are internally self-biased. An external capacitor is recommended for the positive and negative supply voltages.
For the RF pads the equivalent wire bonding inductance (diameter=25µm) have to be according to the following recommendation.

Port	Equivalent inductance (nH)	Wire length (mm) (1)
IN	L_in = 0.25	0.34
OUT	L_out = 0.25	0.34

(1) This value is the total length including the necessary loop from pad to pad.

For a micro-strip configuration a hole in the substrate is necessary for chip assembly.

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Typical Assembly and Bias Configuration to increase the gain :

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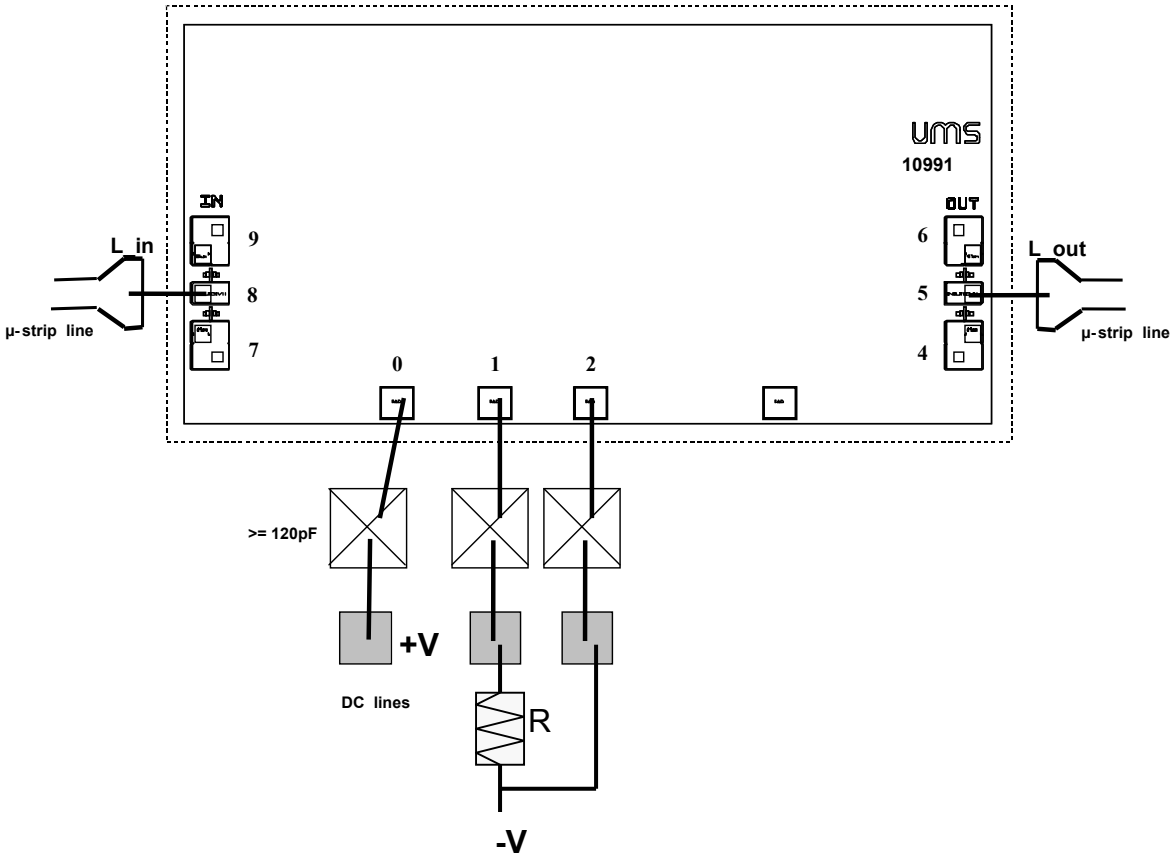

Let's tune the value of the external resistor R to control the biasing point of the first stage and then getting a higher gain for the LNA (trade-off ability between the gain and the noise factor).

Typical value of the external resistor R :

R (kΩ)	Description
0	Low-noise configuration
2	Maximum gain configuration

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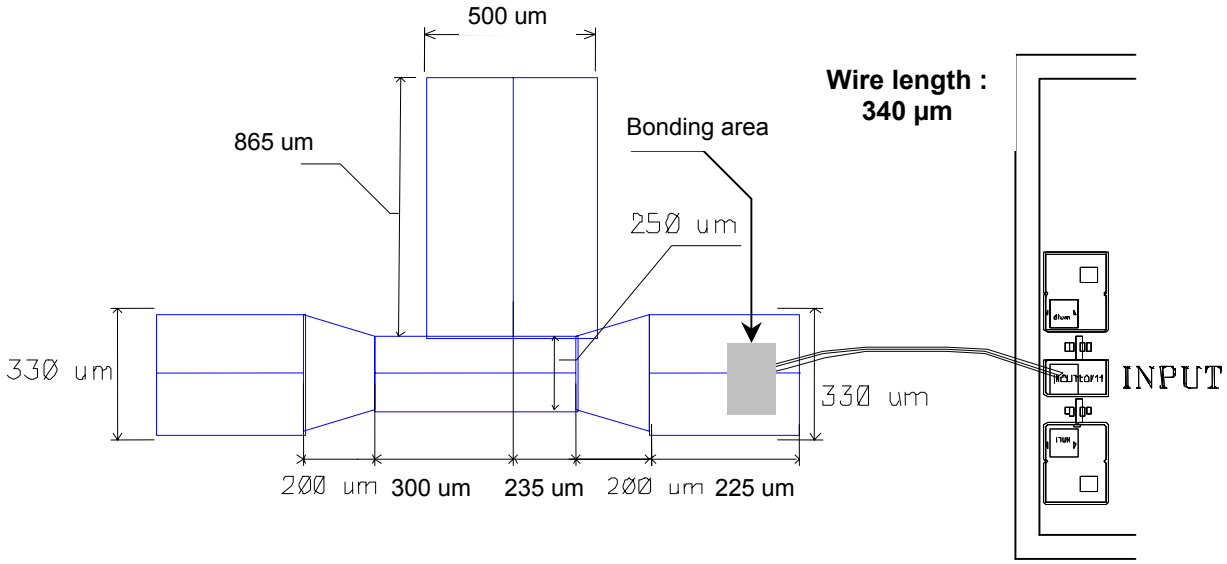
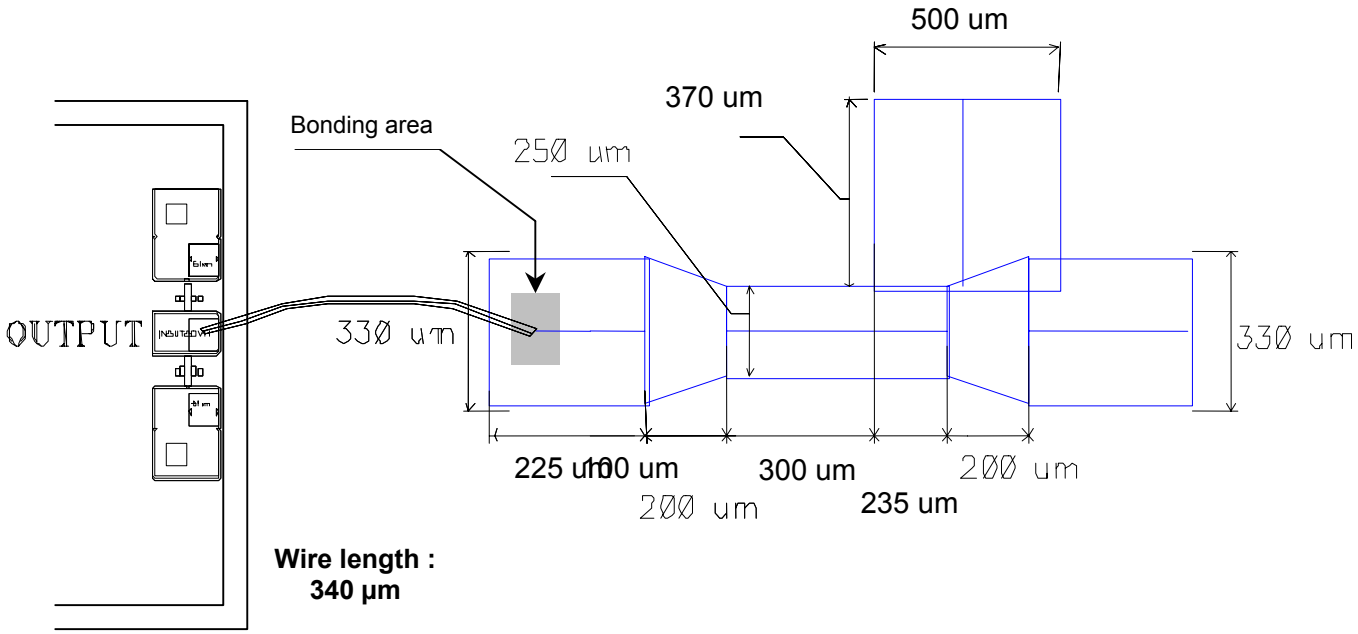
As the connections at 77GHz (between MMIC and MMIC or between MMIC and external substrate) are critical, the transition matching network is split into two parts: one on MMIC and one on the external substrate. This choice allows doing also a direct connection between MMICs. For a connection to an external substrate a network is proposed on soft substrate for IN and OUT ports. The following drawings give the dimensions for a RO3003 substrate (thickness=0.127mm, εr=3).



Proposed matching network for a 50Ω transition between IN port and a µ-strip line on RO3003 substrate



Proposed matching network for a 50Ω transition between OUT port and a µ-strip line on RO3003 substrate

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Ordering Information

Chip form : CHA1077a98F/00

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