# 16-24GHz Low Noise, Variable Gain Amplifier

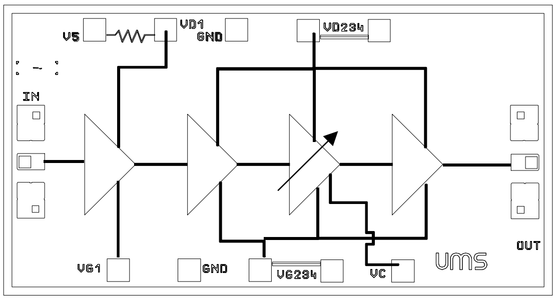
## GaAs Monolithic Microwave IC

## Description

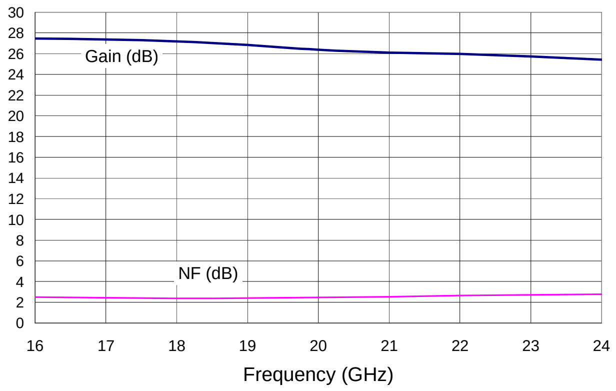
The CHA2292 is a high gain four-stage monolithic low noise amplifier with variable gain. It is designed for a wide range of applications, from military to commercial communication systems.The backside of the chip is both RF and DC grounded. This helps simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Typical on wafer measurements: Gain & NF



## Main Features

- Frequency range: 16-24GHz
- 2.8dB Noise Figure.
- 25dB Gain
- 15dB Gain control range
- DC power consumption: 160mA @ 5V
- Chip size: 2.32 X 1.23 X 0.10mm

## Main Characteristics

Tamb. = 25°

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fop | Operating frequency range | 16 | | 24 | GHz |
| G | Small signal gain | 24 | 26 | | dB |
| NF | Noise figure | | 2.8 | 3.5 | dB |
| Gctrl | Gain control range with Vc variation | 15 | 20 | | dB |
| Id | Bias current | | 160 | | mA |

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

## Electrical Characteristics for Broadband Operation

Tamb = +25℃, V5=Vd2, 3, 4=5V

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fop | Operating frequency range | 16 | | 24 | GHz |
| G | Small signal gain (1) | 24 | 26 | | dB |
| ΔG | Small signal gain flatness (1) | | ±1 | | dB |
| Is | Reverse isolation (1) | | 50 | | dB |
| NF | Noise figure with Vc=1.2V | | 2.8 | 3.5 | dB |
| Gctrl | Gain control range versus Vc | 15 | 20 | | dB |
| P1dB | Output power at 1dB compression with Vc=1.2V | | 11 | | dBm |
| VSWRin | Input VSWR (1) | | 2.5:1 | 3.5:1 | |
| VSWRout | Output VSWR (1) | | 2.0:1 | 3:1 | |
| Vd | DC voltage V5= Vd2,3,4<br>Vc | <br>-1.5 | 5<br>[-0.7, +1.2] | <br>+1.3 | V<br>V |
| Id1 | Bias current (2) with Vc=1.2V | | 35 | | mA |
| Id | Bias current total (3) with Vc=1.2V | | 160 | | mA |

(1) These values are representative of on-wafer measurements that are made without bonding wires at RF ports.
(2) For optimum noise figure, the bias current Id1 should be adjusted to 35mA with Vg1 voltage.
(3) With Id1=35mA, adjust Vg2, 3, 4 voltage for a total drain current around 160mA.

## Absolute Maximum Ratings

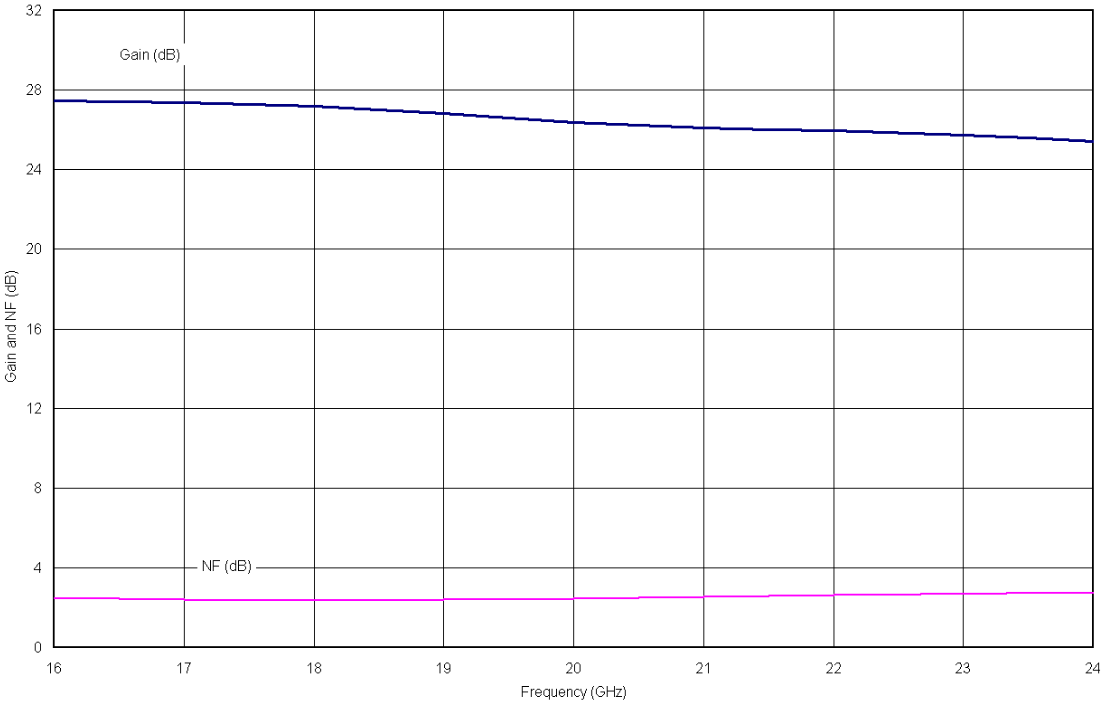
Tamb. = 25℃ (1)

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| Vd | Drain bias voltage | 5.5 | V |
| Vc | Control bias voltage | 1.5 | V |
| Id | Drain bias current | 250 | mA |
| Vg | Gate bias voltage | -2.0 to +0.4 | V |
| Pin | Maximum peak input power overdrive (2) | +15 | dBm |
| Ta | Operating temperature range | -40 to +85 | ℃ |
| Tstg | Storage temperature range | -55 to +155 | ℃ |

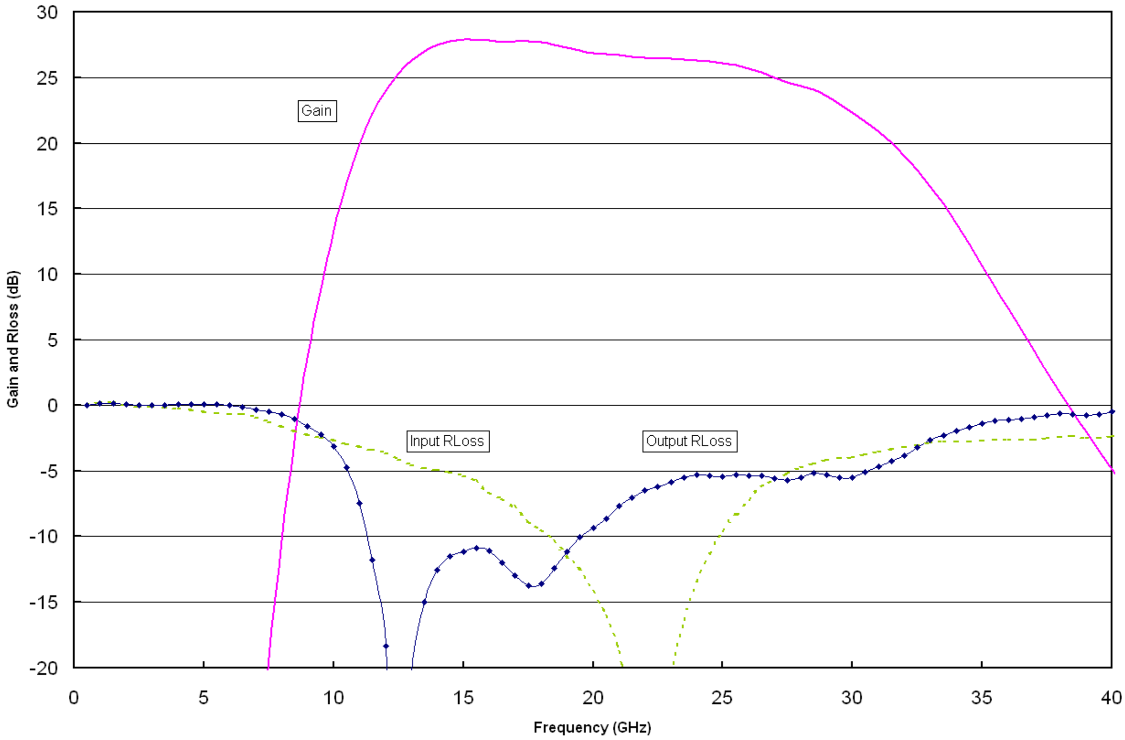
(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

## Typical on wafer Measurements

Bias Conditions: V5=Vd2, 3, 4=5V, Vg1 for Id1=35mA, Vg=-0.3V, Vc=+1.2V



Gain & Noise Figure versus frequency

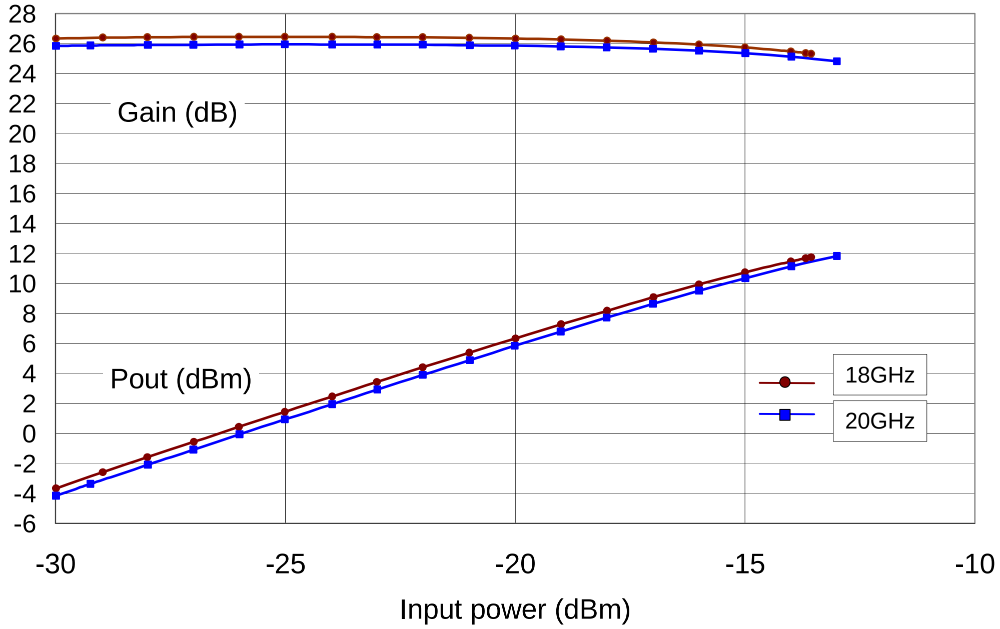


Typical on-wafer Gain & Return Loss

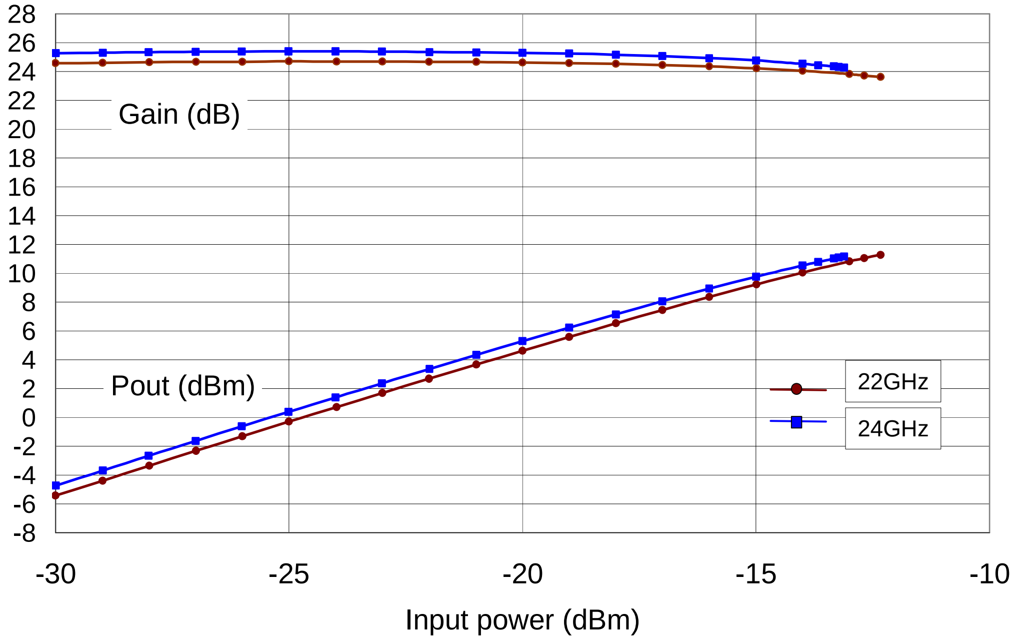
## In jig Measurements

Bias Conditions: V5=Vd2, 3, 4=5V, Vg1=Vg=-0.3V, Vc=+1.2V

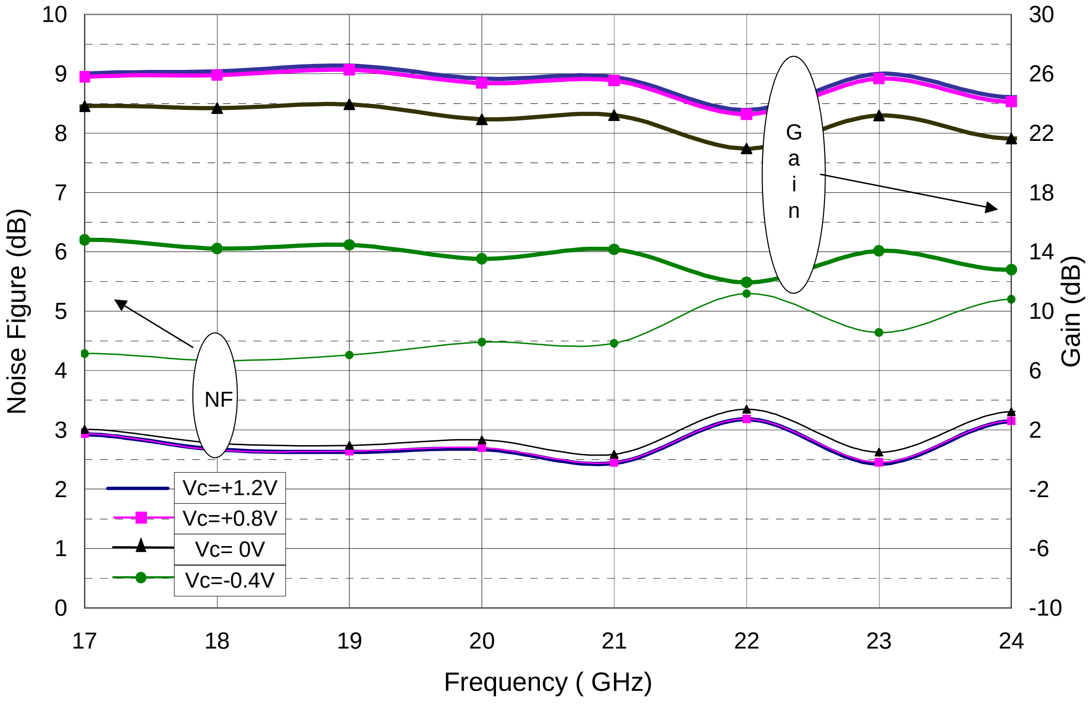
All these measurements include the jig losses (about 0.5dB on gain, 0.2dB on noise figure and 0.3dB on output power).



Gain & Output power @ 18-20 GHz



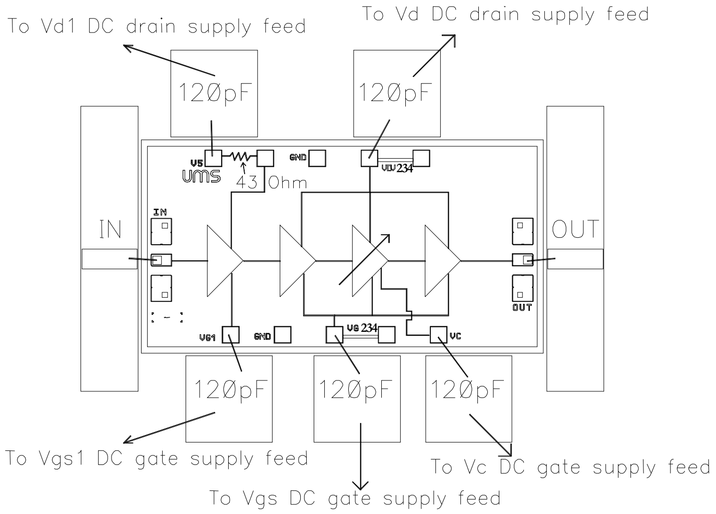
Gain & Output power @ 22–24 GHz

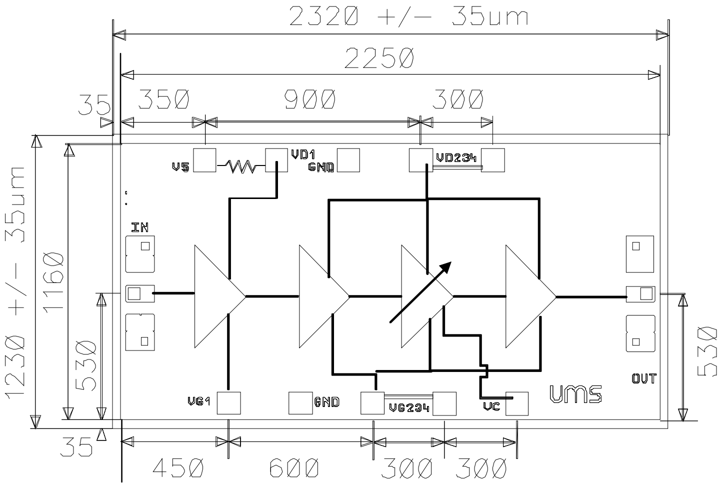


Gain & Noise Figure versus Vc

## Chip Assembly and Mechanical Data

Note: Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended
Bond Pad: 100 x 100µm





**Bonding pad positions**
(Chip thickness: 100µm. All dimensions are in micrometers)

## Ordering Information

Chip form : CHA2292-99F/00