24-30GHz Low Noise, Variable Gain Amplifier

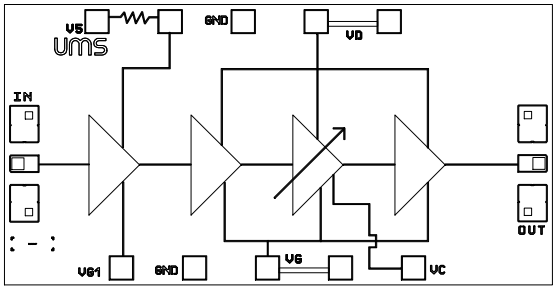
GaAs Monolithic Microwave IC

Description

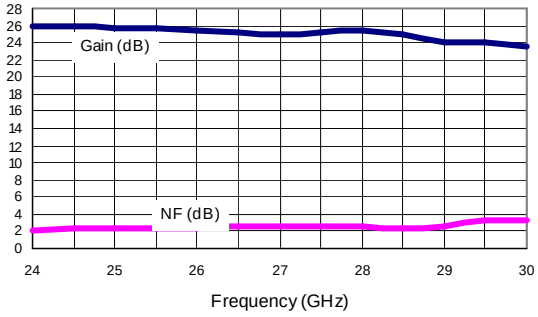
The CHA2293 is a high gain four-stage monolithic low noise amplifier with variable gain. It is designed for a wide range of applications, from military to commercial communication systems.The backside of the chip is both RF and DC grounded. This helps simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Typical on wafer measurements :Gain & NF



Main Features

- Frequency range : 24-30GHz
- 3dB Noise Figure.
- 24dB gain
- Gain control range: 15dB
- Low DC power consumption, 160mA @ 5V
- Chip size : 2.32 X 1.23 X 0.10 mm

Main Characteristics

Tamb. = 25℃

	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	24		30	GHz
G	Small signal gain		24		dB
NF	Noise figure		3	3.5	dB
Gctrl	Gain control range with Vc variation		15		dB
Id	Bias current		160		mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics for Broadband Operation

Tamb = +25℃, V5=Vd= 5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	24		30	GHz
G	Small signal gain (1)	22	24		dB
∆G	Small signal gain flatness (1)		±1.5		dB
Is	Reverse isolation (1)		50		dB
NF	Noise figure with Vc=1.2V		3	3.5	dB
Gctrl	Gain control range versus Vc	12	15		dB
P1dB	Output power at 1dB compression with Vc=1.2V		12		dBm
VSWRin	Input VSWR (1)			4.0:1	
VSWRout	Output VSWR (1)			2.0:1	
Vd	DC voltage V5= Vd Vc	 -1.5	5 [-0.7,+1.2]	 +1.3	V V
Id1	Bias current (2) with Vc=1.2V		35		mA
Id	Bias current total (3) with Vc=1.2V		160		mA

(1) These values are representative of on-wafer measurements that are made without bonding wires at RF ports.
(2) For optimum noise figure, the bias current Id1 should be adjust to 35mA with Vg1.
(3) With Id1=35mA, adjust Vg voltage for a total drain current around 160mA.

Absolute Maximum Ratings

Tamb. = 25℃ (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5.5	V
Vc	Control bias voltage	1.5	V
Id	Drain bias current	250	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Ta	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +155	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

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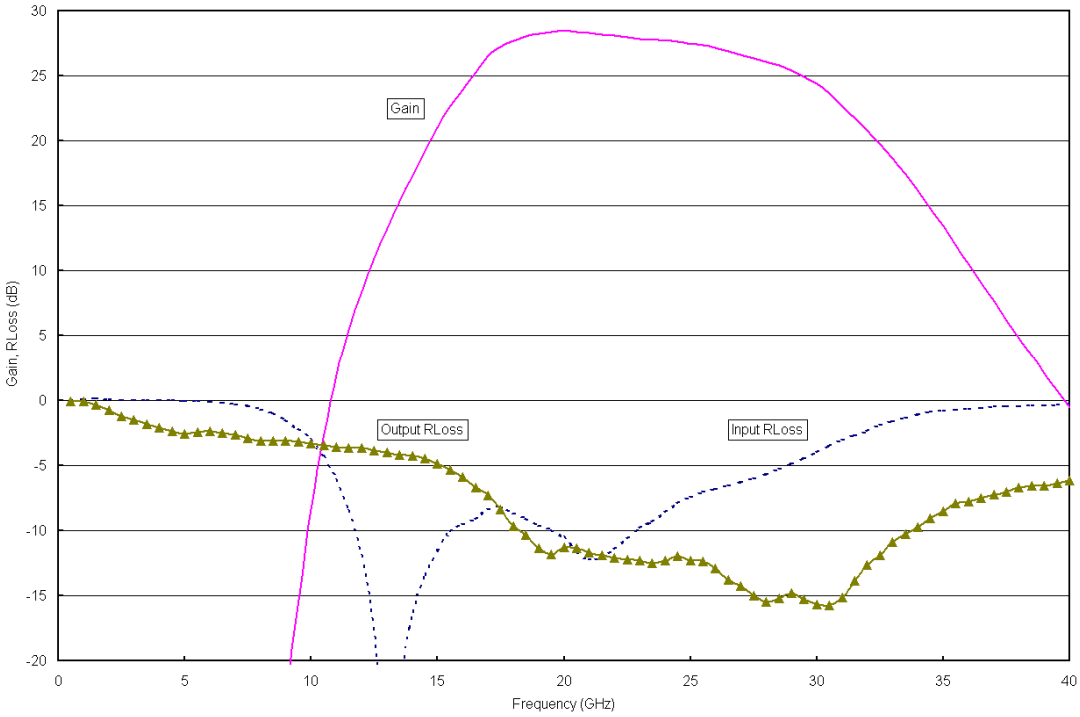
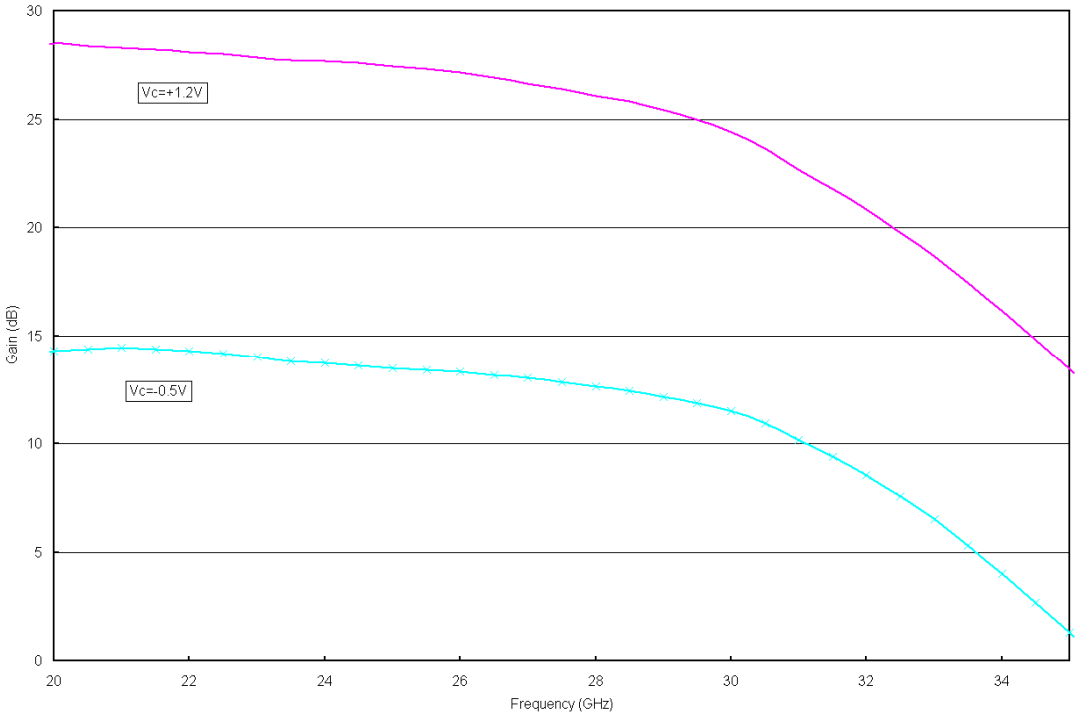
Typical on wafer Measurements

Bias Conditions : V5=Vd=5V, Vg1 pour Id1=35mA, Vg=-0.3V, Vc=+1.2V



Typical on-wafer Gain and Return Loss

Bias Conditions : V5=Vd=5V, Vg1 pour Id1=35mA, Vg=-0.3V



Control gain range versus Frequency

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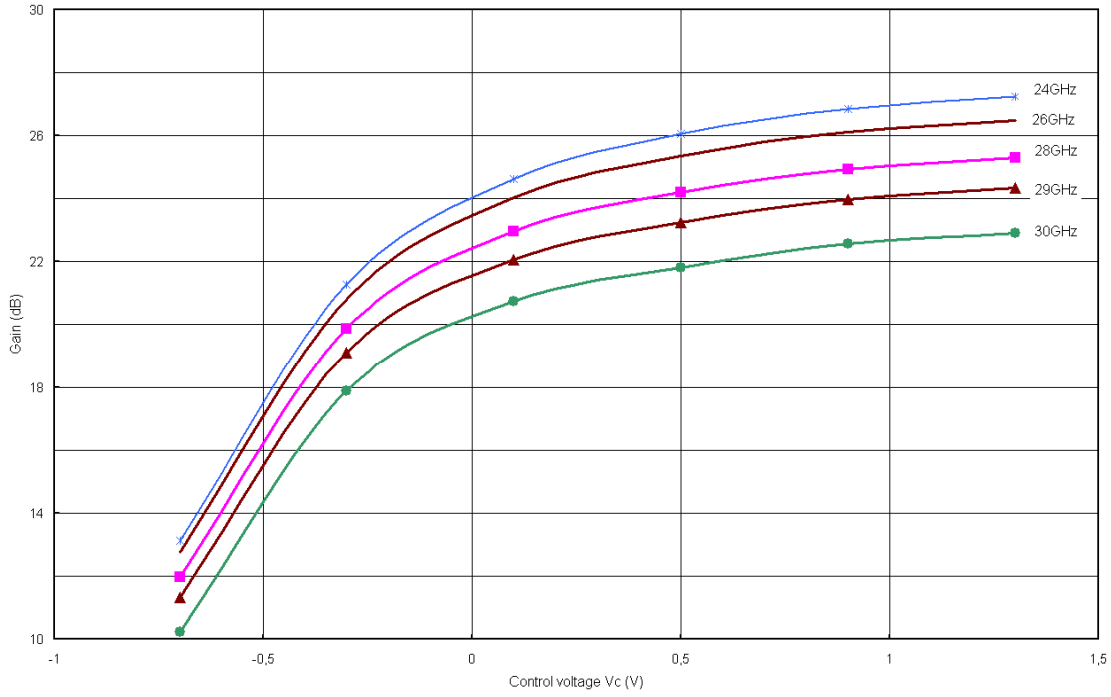
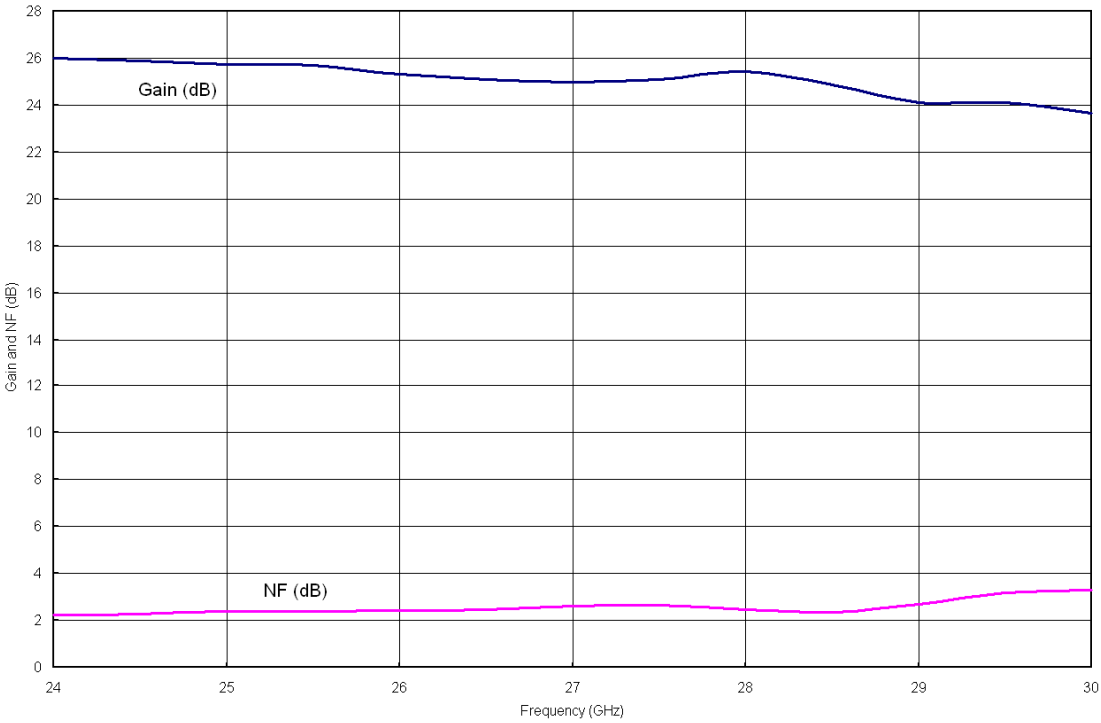
Bias Conditions : V5=Vd=5V, Vg1=Vg=-0.3V



Gain versus control voltage



Gain and Noise Figure versus Frequency (Vc=+1.2V)

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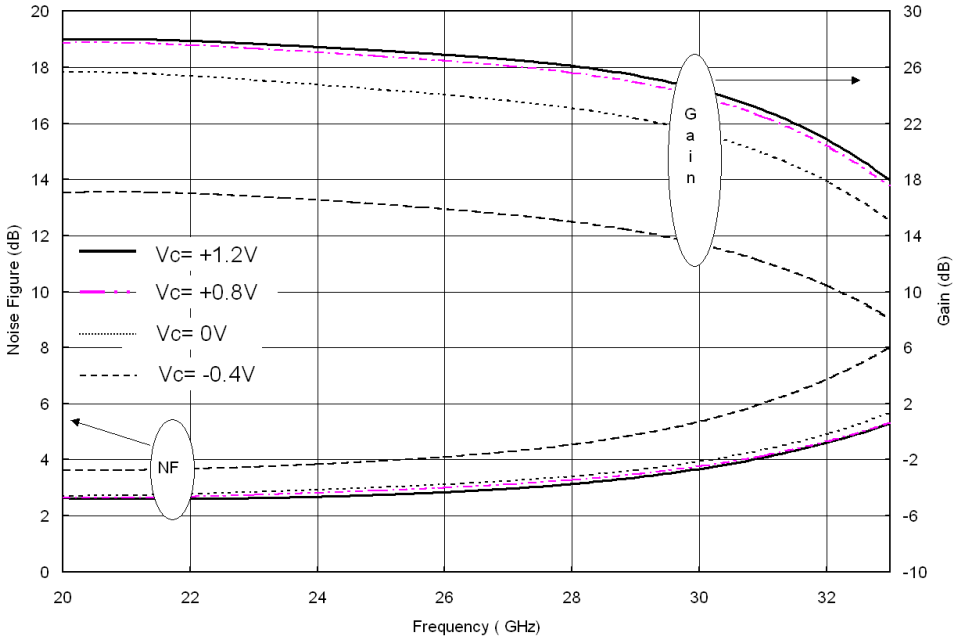
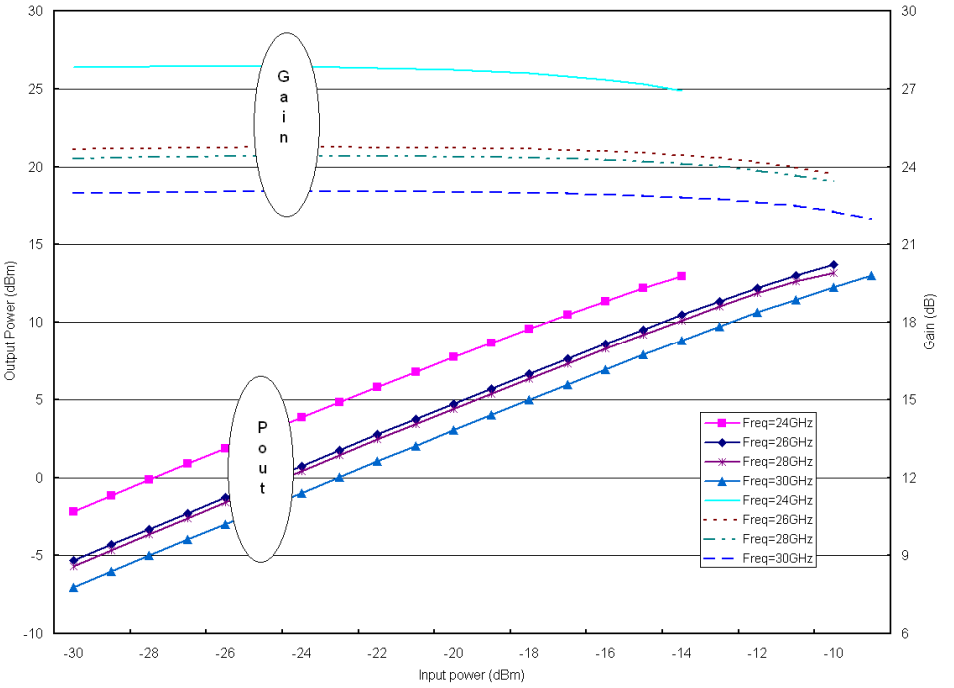
In jig Measurements

Bias Conditions : V5=Vd=5V, Vg1=Vg=-0.3V, Vc=+1.2V
All these measurements include the losses from the jig (about 0.5dB on gain, 0.2dB on noise figure and 0.3dB on output power)

Gain & Output power @ 24-30GHz

Gain & Noise figure versus Vc





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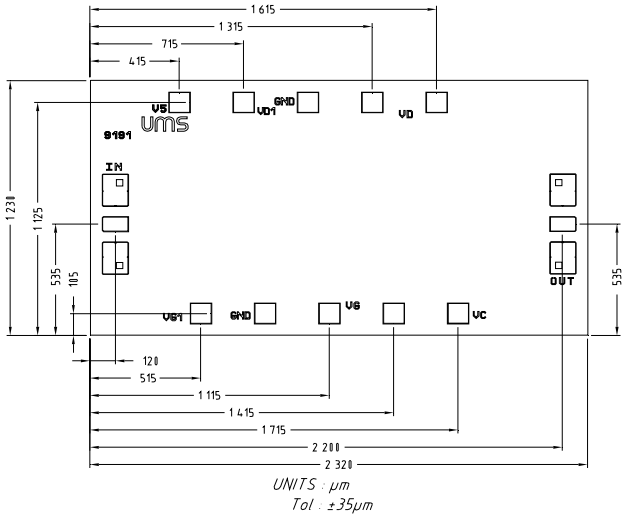
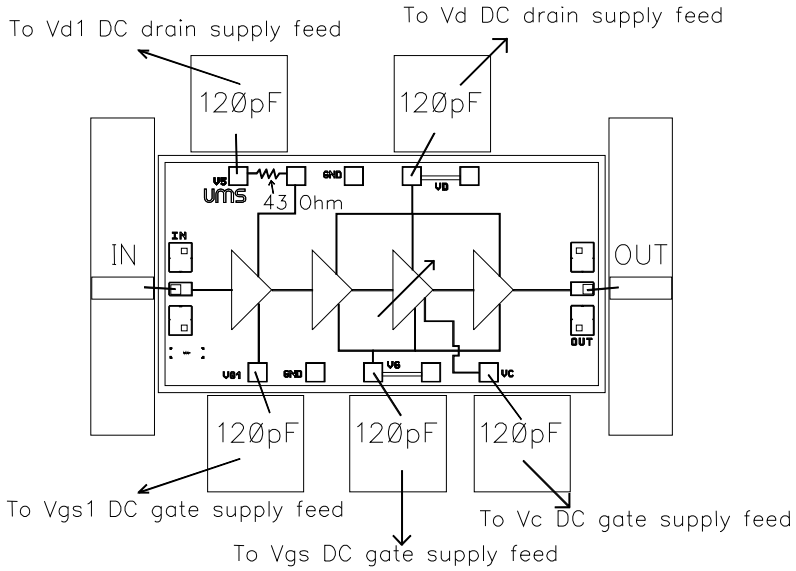
Mechanical Data and Chip Assembly





Note: Supply feeds should be capacitively bypassed. 25µm diameter gold wire is recommended
Bond Pad: 100 x 100 µm

Ordering Information

Chip form : CHA2293-99F/00

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