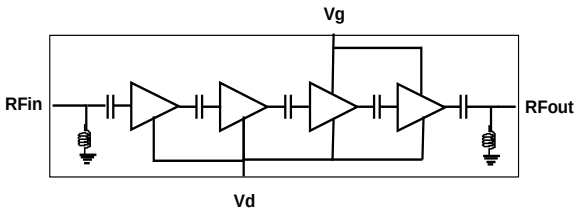
34-44GHz Low Noise Amplifier

GaAs Monolithic Microwave IC

Description

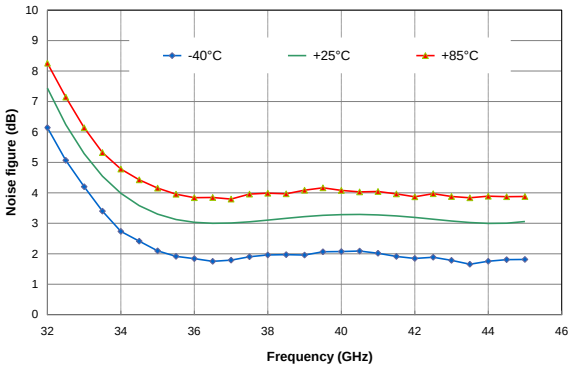
The CHA2494-98F is a wide band monolithic low noise amplifier.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Main Features

- Broadband performances: 34-44GHz
- 3dB noise figure
- 20dB gain
- 20dBm Output IP3
- DC bias: Vd=4V @ Id=80mA
- Chip size 2.59x1.16x0.1mm

Noise figure versus temperature



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	34		44	GHz
Gain	Linear Gain		20		dB
NF	Noise Figure		3.0		dB
OIP3	3rd order intercept point		20		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +4V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	34		44	GHz
Gain	Linear Gain		20		dB
NF	Noise Figure		3.0		dB
RLin	Input Return Loss		-8		dB
RLout	Output Return Loss		-8		dB
OIP3	Output 3rd order intercept point		20		dBm
OP1dB	Output Power @1dB comp.		12		dBm
Vg	Gate voltage		-0.45		V
Id	Drain current		80		mA

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.
A bonding wire of typically 0.3 to 0.4nH will improve the matching at the accesses.

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5V	V
Id	Drain bias current	160	mA
Vg	Gate bias voltage	-2 to +0.4	V
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	DC drain voltage	4	V
Id	DC drain current controlled with Vg	80	mA
Vg	DC gate voltage	-0.45	V

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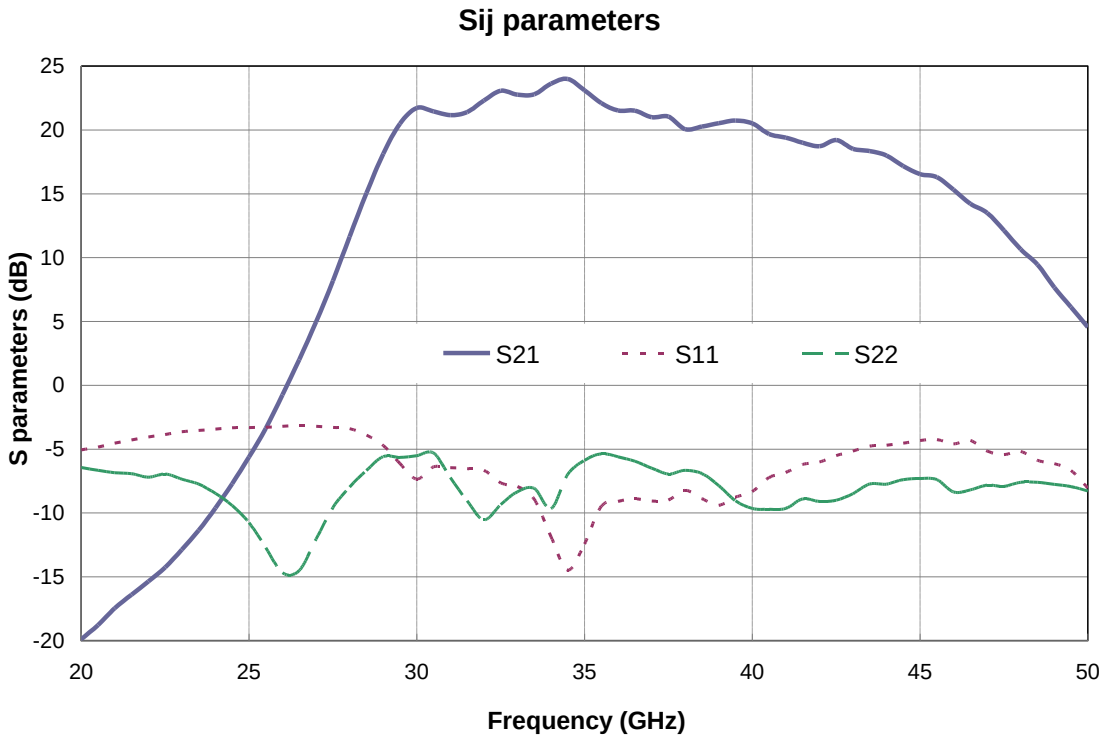
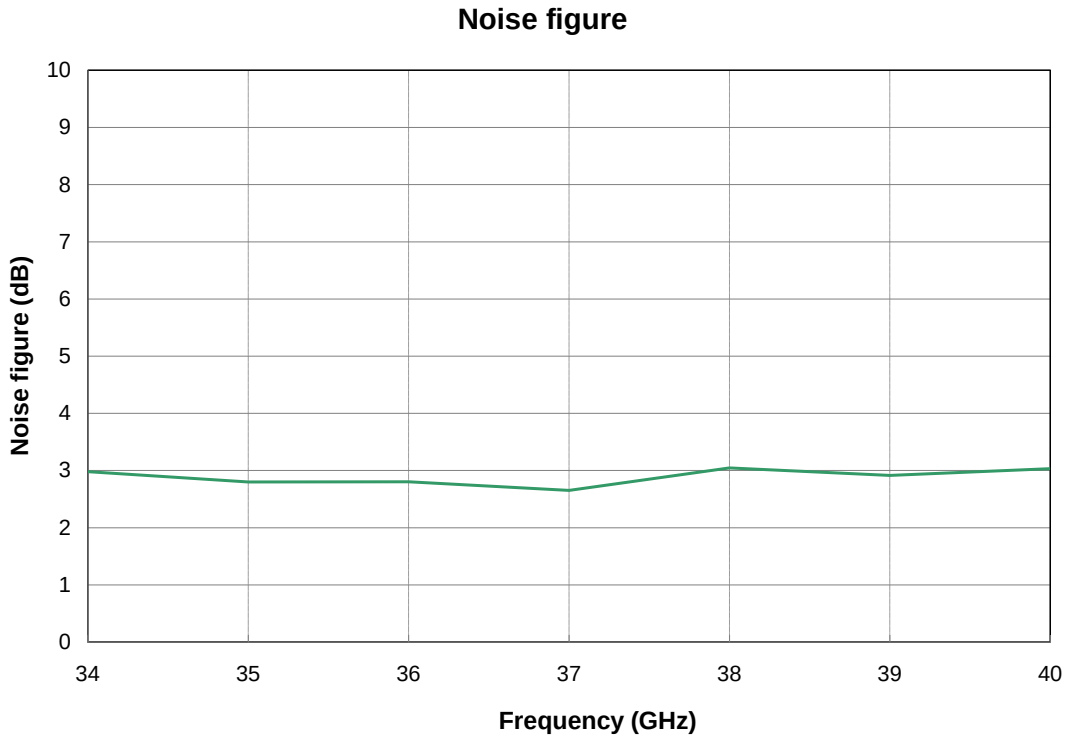
Typical on wafer Measurements

Tamb = +25°C, Vd = +4V, Id = 80mA





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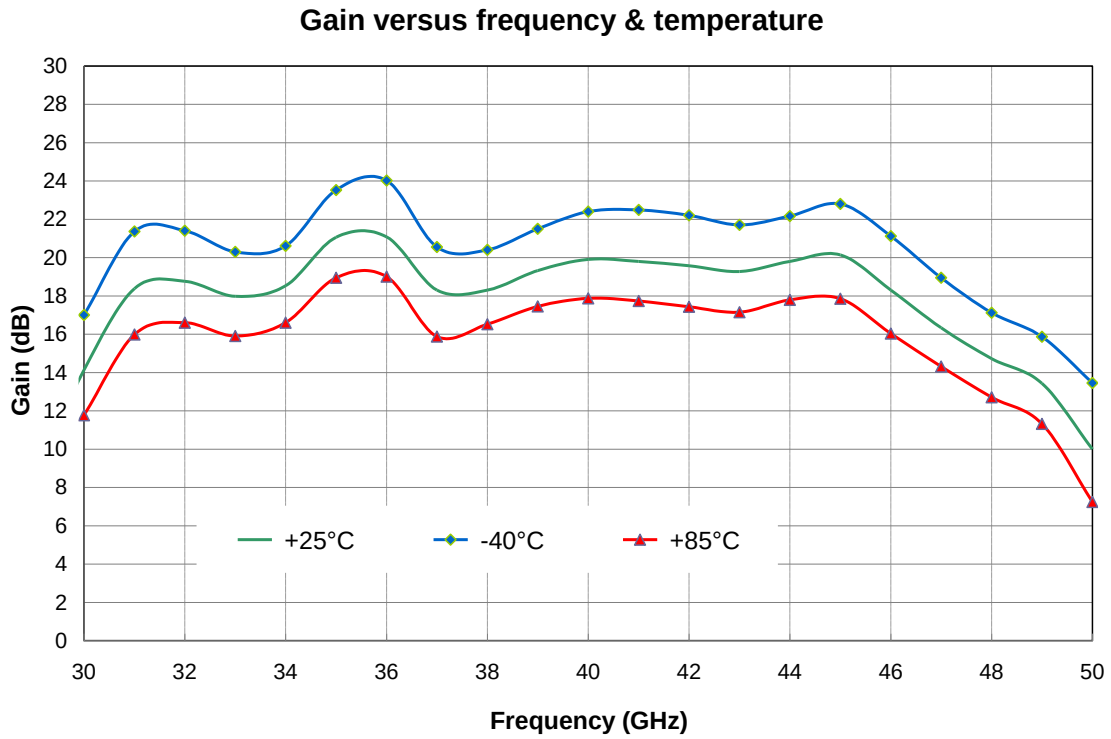
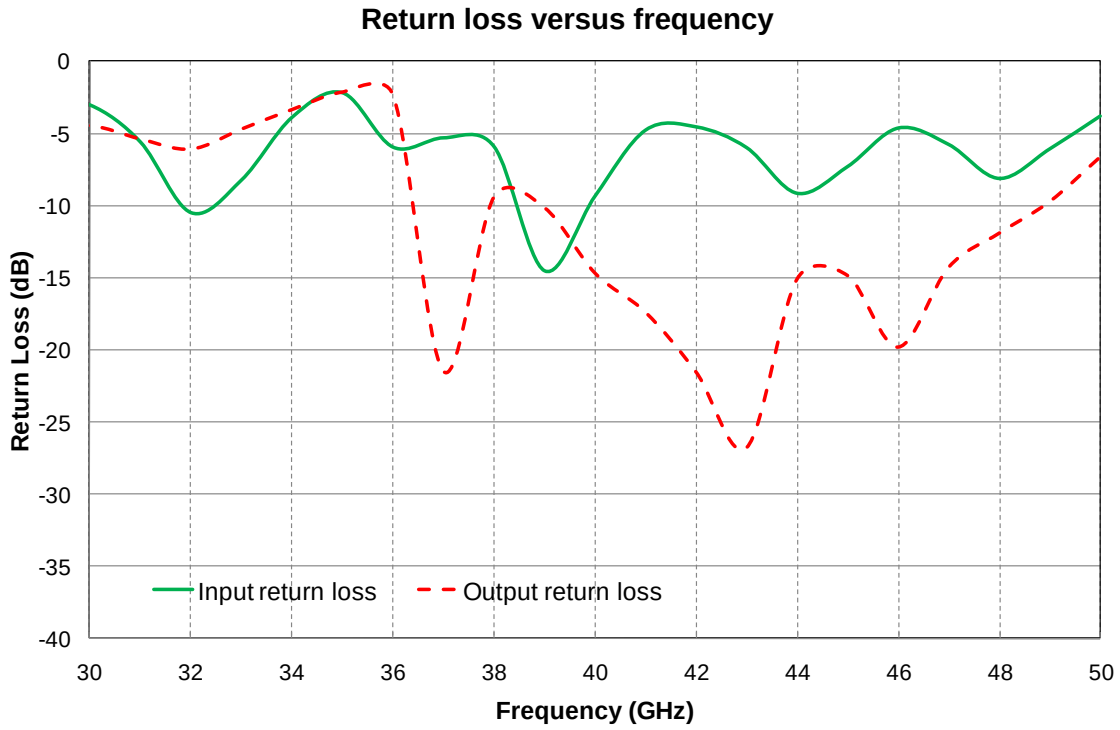
Typical Test Fixture Measurements

Tamb = +25°C, Vd = +4V, Id = 80mA





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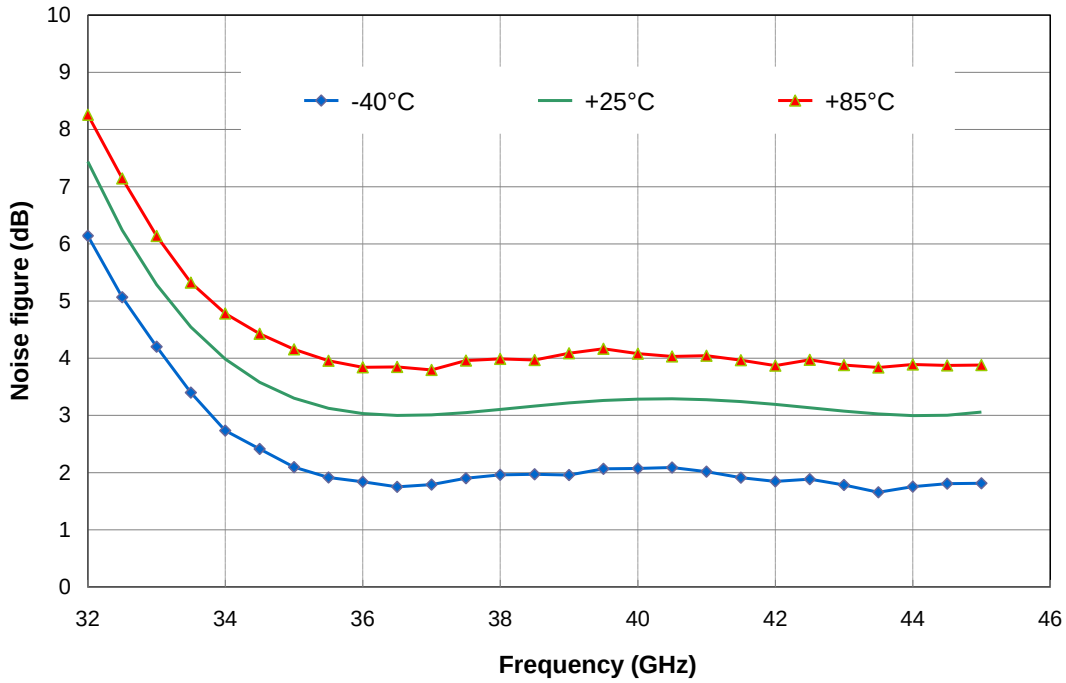
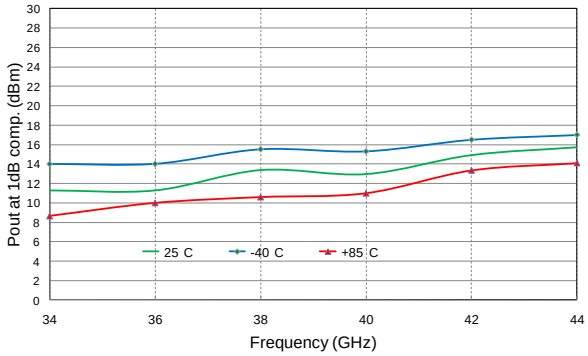
Typical Test Fixture Measurements

Tamb = +25°C, Vd = +4V, Id = 80mA

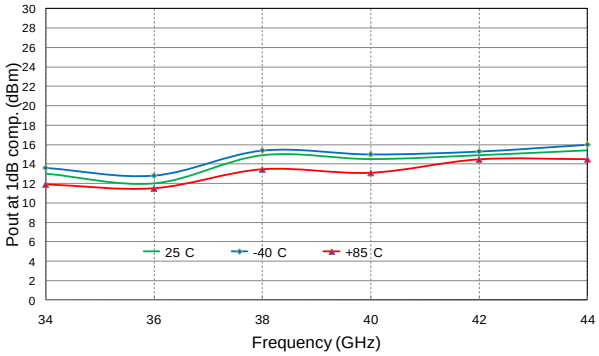
Noise figure versus frequency & temperature



Output Power @ 1dB comp. versus temperature at 80mA



Output Power @ 1dB comp. versus temperature at 120mA



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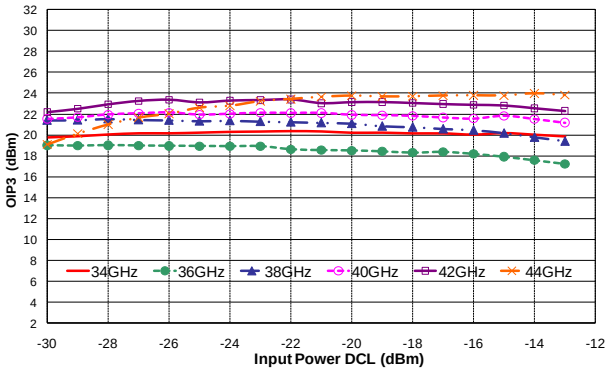
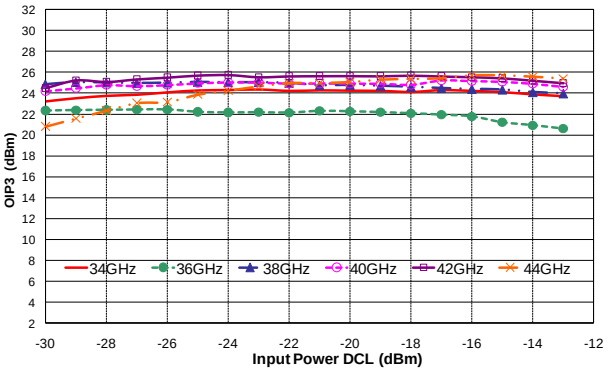
Typical Test Fixture Measurements

Tamb = +25°C, Vd = +4V, Id = 80mA

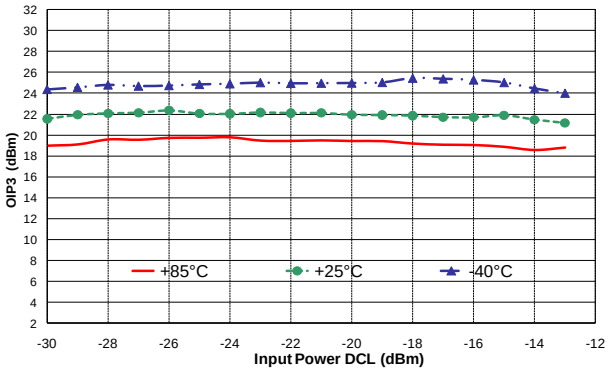
Output IP3 versus frequency at 80mA



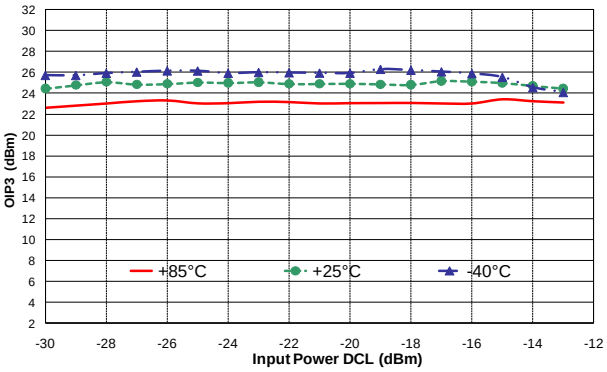
Output IP3 versus frequency at 120mA



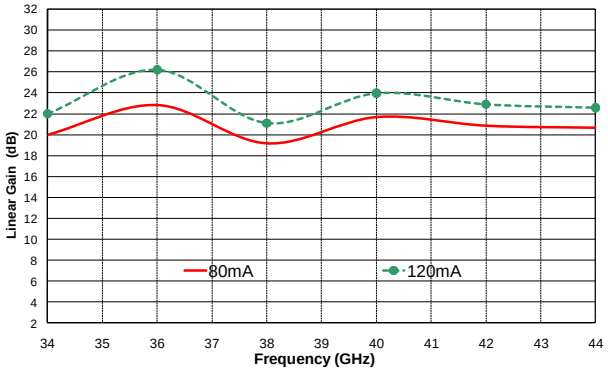
Output IP3 versus temperature at 80mA & 40GHz



Output IP3 versus temperature at 120mA & 40GHz



Linear gain versus current



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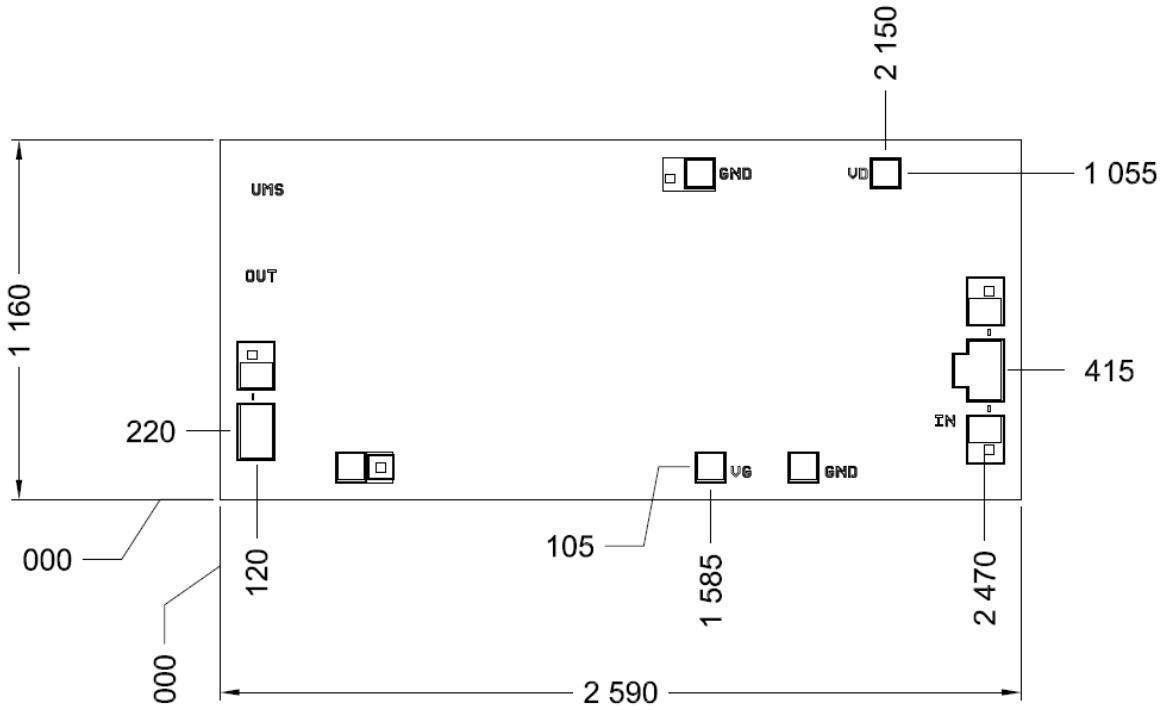
Mechanical data



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Chip thickness: 100µm
DC pad size: 86x83µm
RF pad size: 105x172µm

Chip size: 2590x1160 ±35µm
All dimensions are in micrometers

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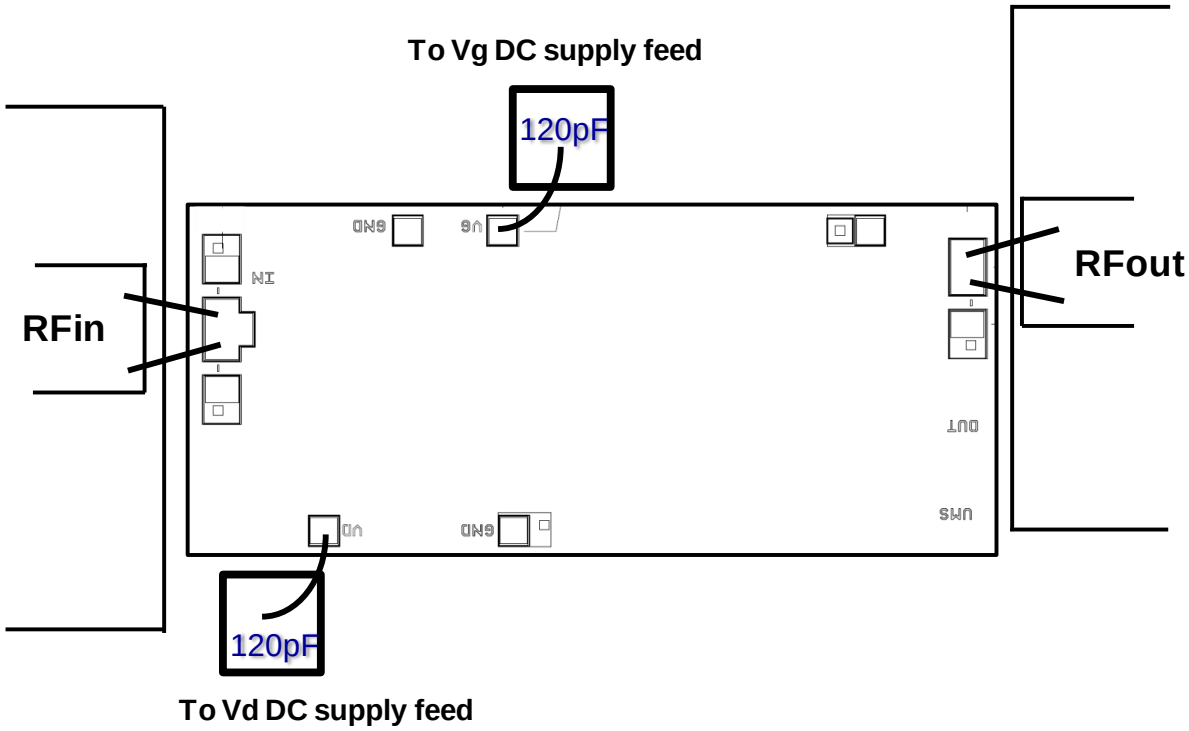
Recommended assembly plan



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
VD	Vd	120pF	Drain Supply
VG	Vg	120pF	Gate Supply

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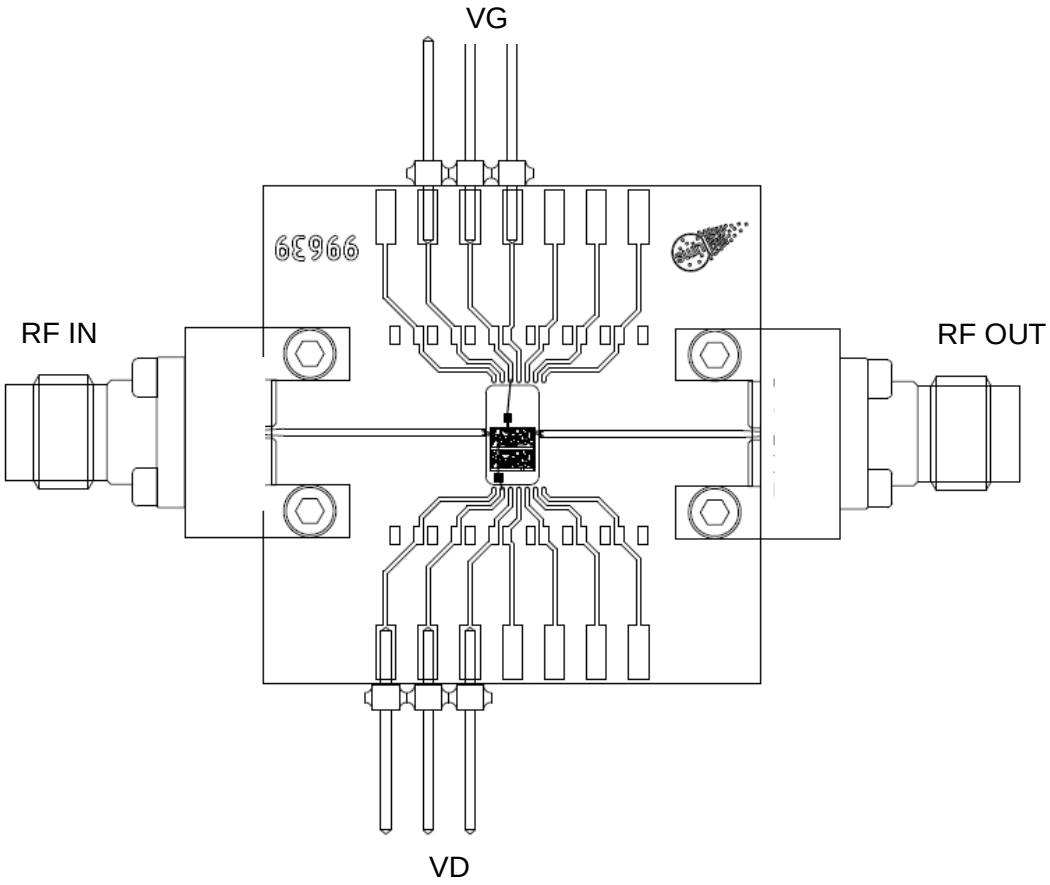
Evaluation mother board

- Based on typically Ro4003 / 8mils or equivalent.
- Decoupling capacitors of 120pF are recommended for all DC accesses.
- The board losses are estimated from 2 to 3dB in the frequency range.



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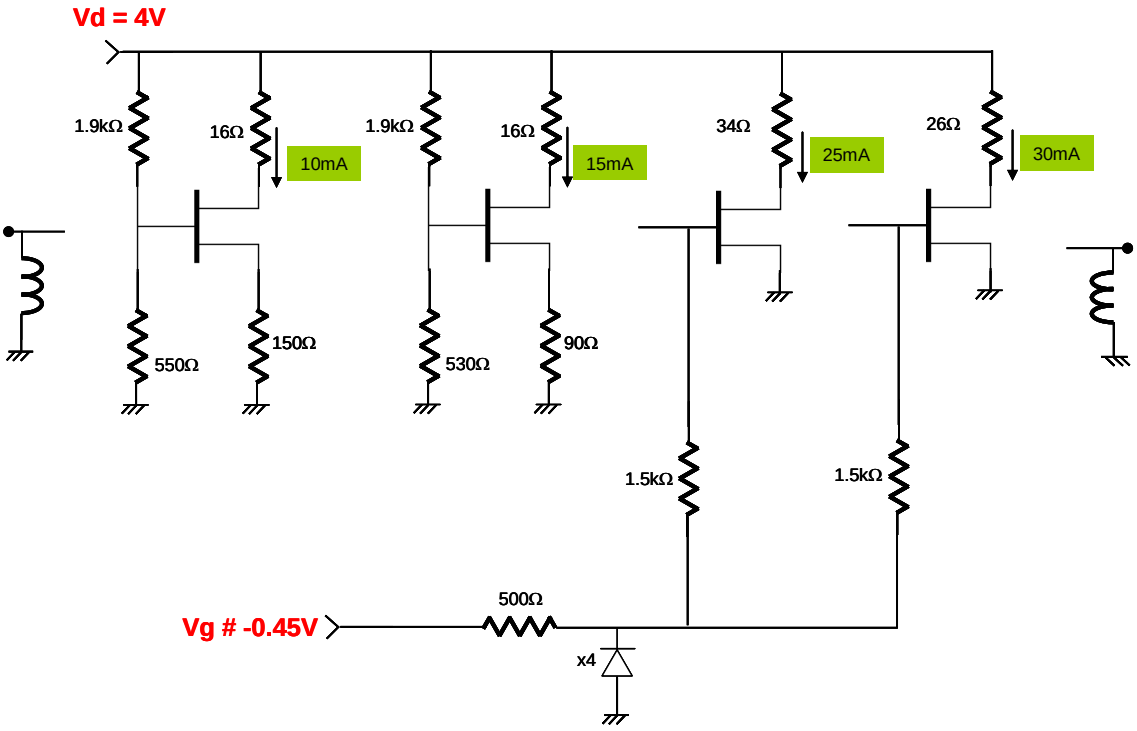
DC Schematic

LNA: 4V, 80mA



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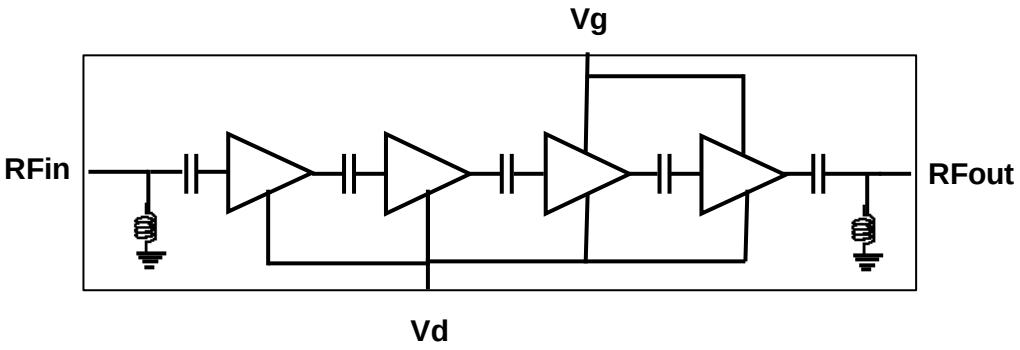
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



ESD protections is also implemented on gate access common to 3rd and 4th stage (1st and 2nd stage are self-biased).

Due to BCB coating on the chip, qualification domain implies the chip must be glued.

Biasing conditions:

Vg could be tuned to reach 120mA in order to increase the output power and the gain (see pages 5 & 6).
The current has no influence on Noise figure.

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Chip form:	CHA2494-98F/00

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