

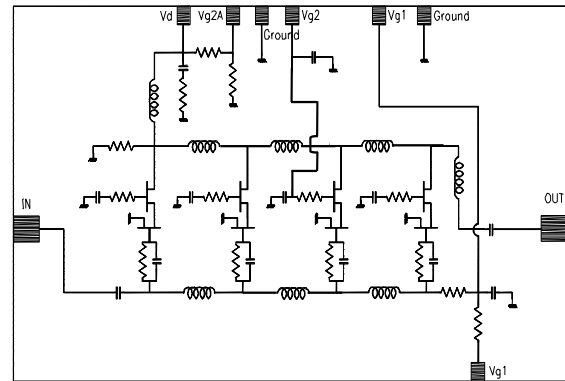
1-18GHz WIDE BAND AMPLIFIER

GaAs Monolithic Microwave IC

Description

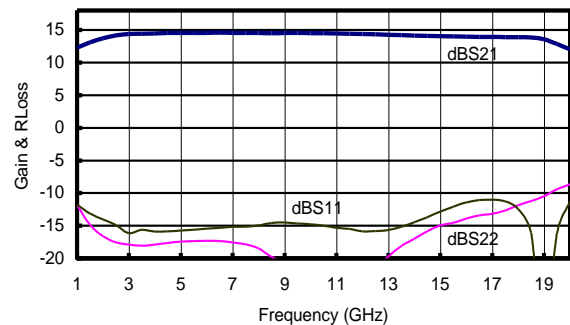
The CHA3023-99F is a travelling wave amplifier using cascode FET. It is designed for a wide range of applications.

The circuit is manufactured with a pHEMT process of 0.25 μ m gate length, via holes through the substrate and air bridges and it is available in die form.



Main Features

- Broadband performances: 1-18GHz
- 14dB gain
- 3dB typical Low Noise Figure
- ± 0.7 dB gain flatness
- Chip size: 2.15 X 1.42 X 0.10mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	1		18	GHz
G	Small signal Gain	12.5	14		
NF	Noise figure			4	dB
Id	Bias current		95		mA

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Specifications (for Broadband Operation)

Tamb. = +25°C

Vd = 5V, Vg1 = -0.3V tuned to have Id = 95mA, Vg2 = +2V

Symbol	Parameter	Min	Typ	Max	Unit	
Fop	Operating frequency range	1		18	GHz	
G	Small signal gain F= 1 to 3GHz	11.5	13		dB	
		12.5	14		dB	
ΔG	Small signal gain flatness		± 0.7		dB	
P1dB	Output power at 1dB gain compression	15	17		dBm	
VSWRin	Input VSWR		2.2:1			
VSWRout	Output VSWR		2.2:1			
NF	Noise Figure F= 1 to 4GHz		4	6	dB	
			2.5	4	dB	
Vdc	DC voltage	Vd	+5		V	
			Vg1	-0.3		V
				Vg2	+2	
Id	Bias current		95		mA	

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Min.	Max.	Unit
Vd	Drain to ground bias voltage	0	6.5	V
Id	Drain current		110	mA
Vg1	Gate to ground bias voltage	-1.5	0.3	V
Vg2	Gate to ground bias voltage	0	3	V
Pin	Maximum peak input power overdrive		+15	dBm
Pin	Maximum input CW power		+10	dBm
Top	Operating temperature	-40	85	°C
Tstg	Storage temperature range	-55	150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

Device thermal performances

All the figures given in this section are obtained assuming that the packaged device is only cooled down by conduction through the package thermal pad (no convection mode considered).

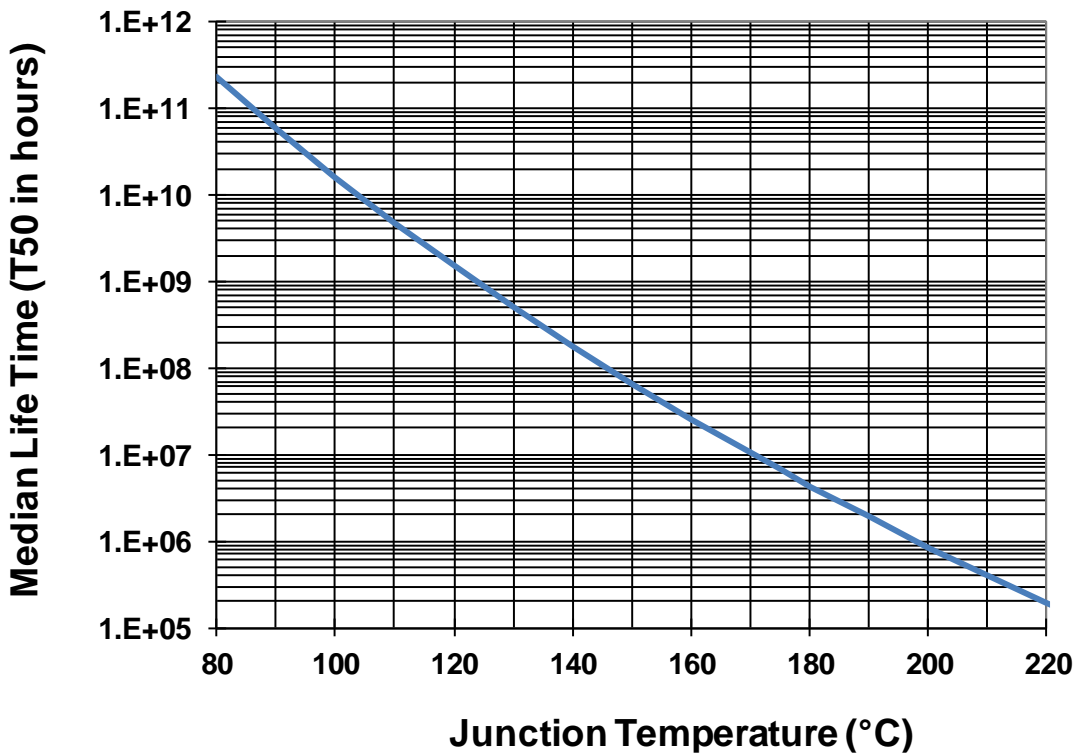
The temperature is monitored at the package back-side interface (T_{case}).

The system maximum temperature must be adjusted in order to guarantee that $T_{junction}$ remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with these requirements.

Parameter	Biassing conditions	$T_{junction}$ (°C)	R_{TH} (°C/W)	T50 (Hours)
$R_{TH}^{(1)}$ Thermal Resistance (Junction to Case)	Vd = 5V Idq = 95mA Pdis = 475mW	115	63	5E+09

⁽¹⁾ Assuming 85°C T_{case}



Typical on-wafer Sij parameters

Tamb.= +25°C

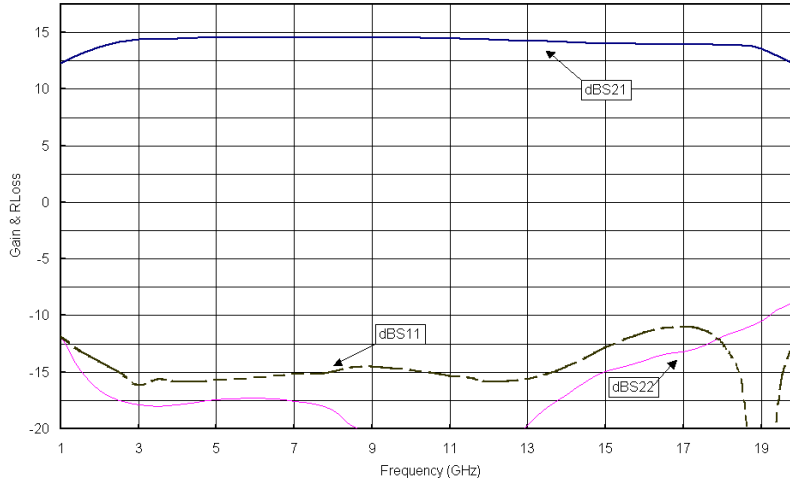
Vd = 5.0V ; Vg2 = 2V and Vg1 tuned to Id = 95mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1.00	-11.84	-86.69	-68.86	12.95	12.27	175.21	-11.75	175.50
1.50	-14.88	-96.63	-59.00	-65.50	13.11	164.60	-13.13	134.72
2.00	-16.59	-102.61	-57.76	-85.24	13.74	152.90	-14.05	103.57
2.50	-17.55	-106.89	-55.88	-101.83	14.21	140.45	-14.93	77.53
3.00	-17.90	-110.67	-56.09	-133.36	14.38	127.54	-16.15	60.98
3.50	-18.04	-114.80	-54.51	-146.60	14.42	116.64	-15.59	48.79
4.00	-17.90	-119.10	-53.45	-166.51	14.50	105.01	-15.88	36.69
4.50	-17.64	-124.04	-52.07	178.88	14.55	93.81	-15.86	24.61
5.00	-17.43	-129.21	-52.57	165.06	14.56	82.83	-15.73	15.78
5.50	-17.36	-134.92	-50.96	155.03	14.57	71.87	-15.62	6.63
6.00	-17.32	-140.65	-49.52	145.22	14.57	61.00	-15.45	-1.24
6.50	-17.35	-146.35	-48.93	131.37	14.59	50.26	-15.32	-9.98
7.00	-17.55	-152.20	-48.40	115.97	14.58	39.44	-15.18	-16.89
7.50	-17.83	-157.72	-47.52	106.26	14.57	28.65	-15.15	-23.44
8.00	-18.45	-162.53	-46.94	95.20	14.56	17.95	-14.94	-30.10
8.50	-19.80	-164.62	-46.12	84.24	14.54	7.35	-14.56	-35.12
9.00	-20.69	-168.37	-45.55	74.79	14.55	-3.41	-14.48	-41.40
9.50	-21.89	-169.76	-44.84	62.64	14.55	-14.27	-14.67	-46.03
10.00	-23.72	-166.34	-44.04	53.09	14.53	-25.14	-14.80	-51.30
10.50	-25.53	-158.58	-43.80	39.38	14.50	-36.02	-14.99	-53.99
11.00	-26.70	-141.85	-43.12	26.47	14.48	-46.99	-15.32	-57.64
11.50	-25.89	-122.93	-42.27	14.98	14.44	-57.87	-15.48	-58.42
12.00	-24.09	-110.31	-41.97	2.10	14.40	-68.96	-15.87	-59.30
12.50	-21.74	-106.76	-41.35	-12.13	14.35	-79.91	-15.80	-58.07
13.00	-19.70	-104.76	-41.15	-24.23	14.29	-90.92	-15.65	-56.60
13.50	-18.11	-106.18	-40.87	-38.14	14.23	-101.96	-15.16	-55.31
14.00	-17.00	-112.34	-40.38	-49.23	14.17	-112.98	-14.47	-55.03
14.50	-15.86	-116.67	-40.14	-64.35	14.11	-124.02	-13.71	-56.11
15.00	-14.97	-120.58	-39.83	-75.76	14.05	-135.10	-12.85	-58.60
15.50	-14.53	-124.94	-39.66	-88.72	14.01	-146.32	-12.09	-63.04
16.00	-13.93	-128.81	-39.29	-102.25	13.97	-157.55	-11.44	-69.64
16.50	-13.43	-132.05	-38.83	-118.12	13.93	-168.97	-11.06	-77.10
17.00	-13.18	-134.80	-38.87	-127.14	13.92	179.41	-11.02	-85.48
17.50	-12.67	-137.46	-38.86	-144.06	13.92	167.15	-11.28	-95.81
18.00	-11.85	-137.37	-37.71	-156.10	13.91	154.49	-12.47	-109.17
18.50	-11.23	-139.77	-37.48	-170.79	13.84	140.84	-16.01	-125.94
19.00	-10.46	-143.04	-37.24	175.70	13.57	125.81	-32.15	-109.28
19.50	-9.39	-147.86	-36.76	157.84	12.86	111.51	-16.15	-15.25
20.00	-8.65	-153.32	-36.48	142.87	12.02	99.83	-11.25	-34.96

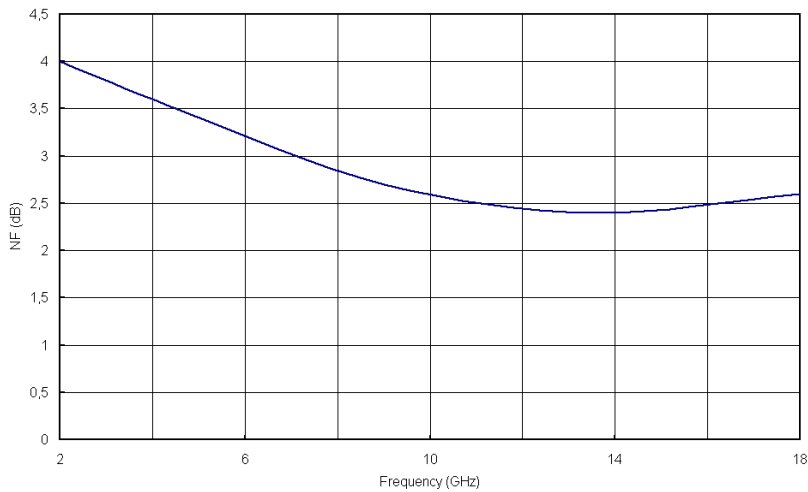
Typical on wafer Measurements

Tamb = +25°C, Vd = 5.0V ; Vg2 = 2V and Vg1 tuned to Id = 95mA

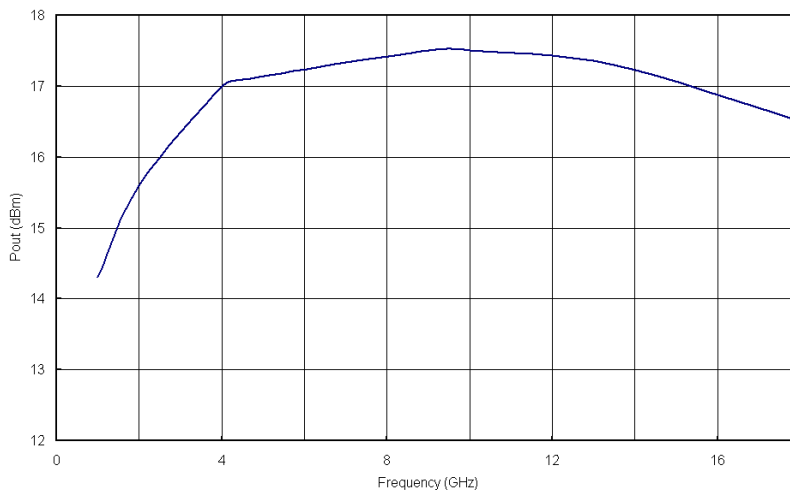
Typical on wafer S parameters



Typical on wafer Noise Figure



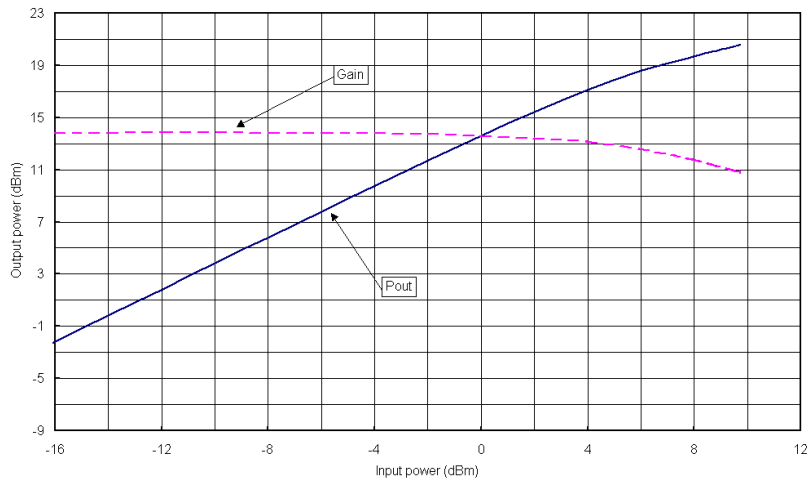
Pout vs Frequency (Pin=4dBm)



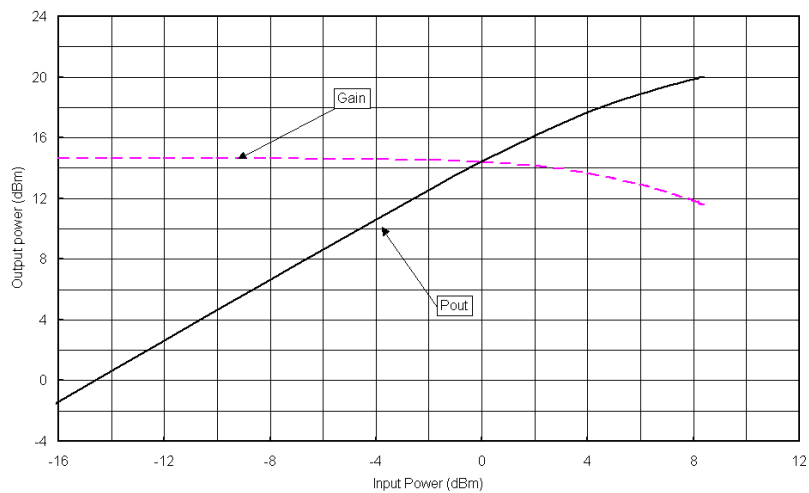
Typical Test Fixture Measurements

Tamb = +25°C, Vd = 5.0V ; Vg2 = 2V and Vg1 tuned to Id = 95mA

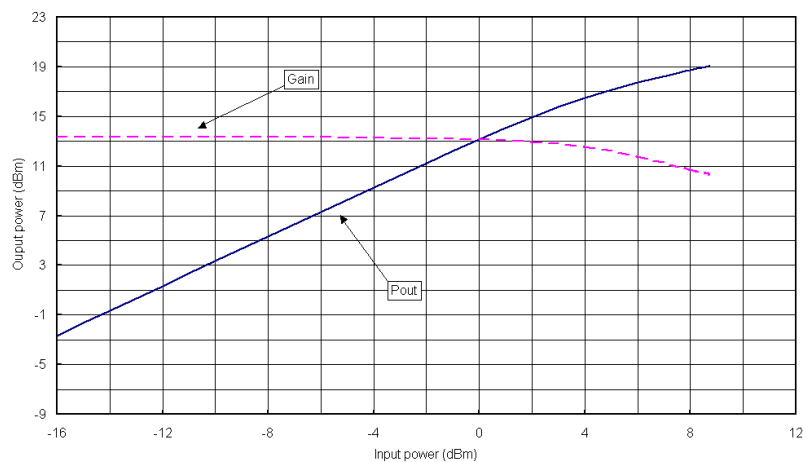
Power compression @ 1GHz



Power compression @ 12GHz



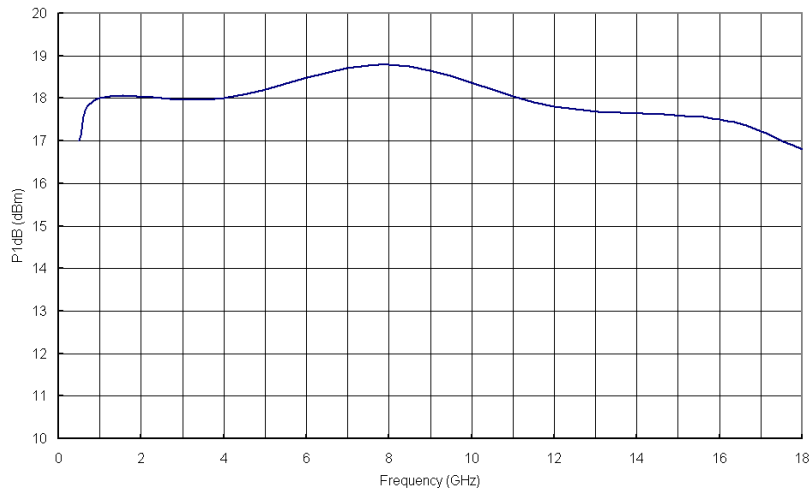
Power compression @ 18GHz



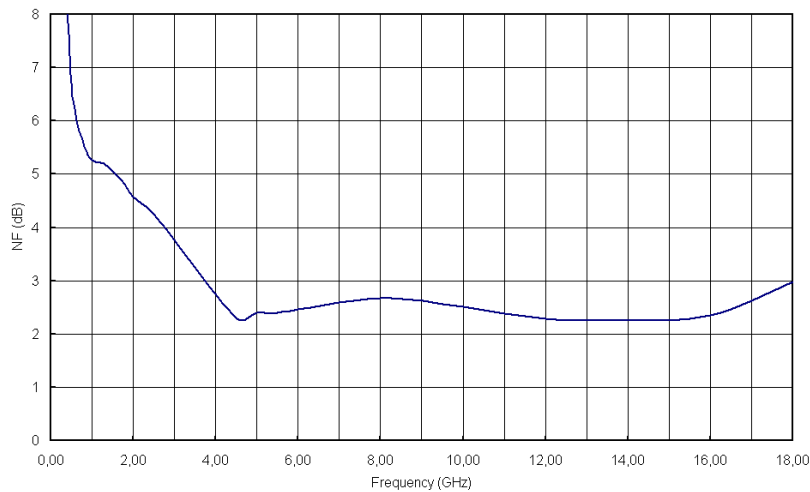
Typical Test Fixture Measurements

Tamb = +25°C, Vd = 5.0V ; Vg2 = 2V and Vg1 tuned to Id = 95mA

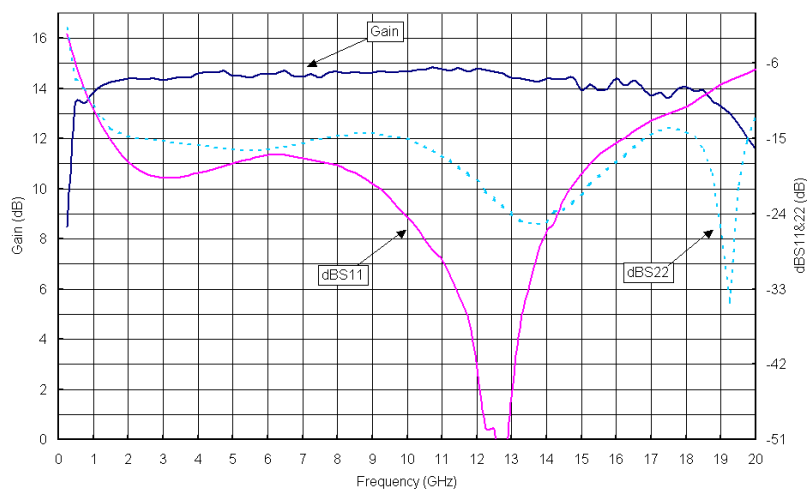
P1dB vs Frequency



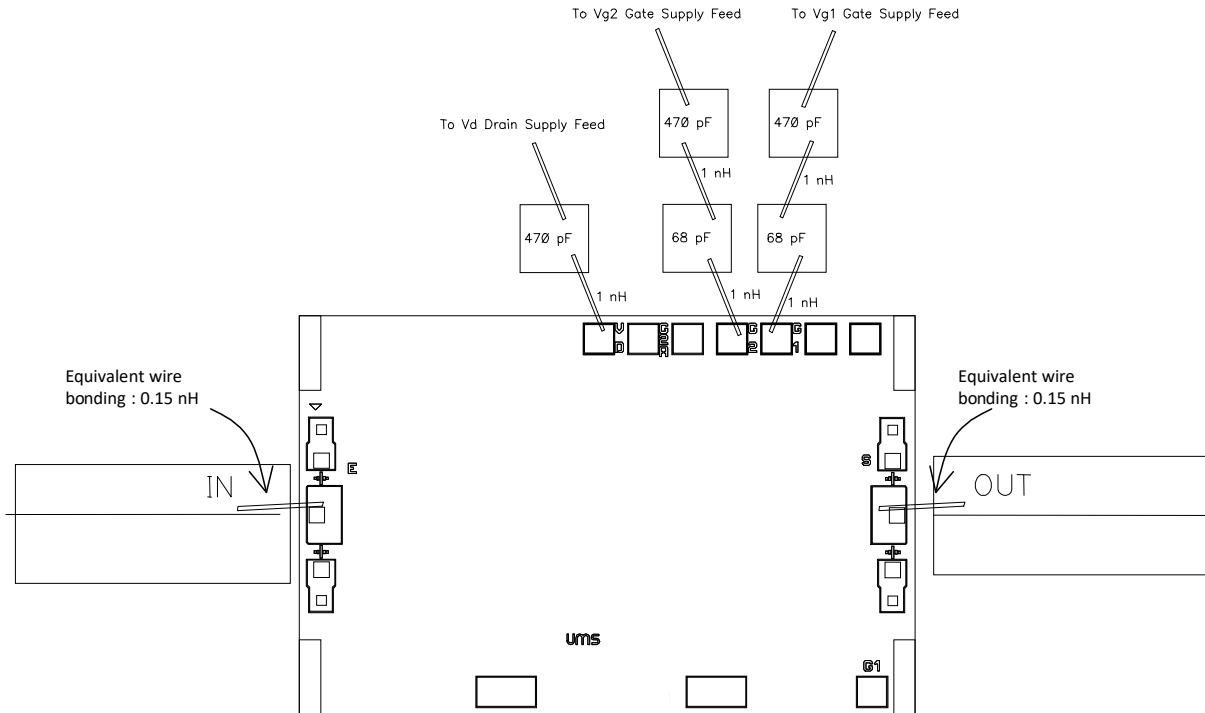
Noise Figure vs Frequency



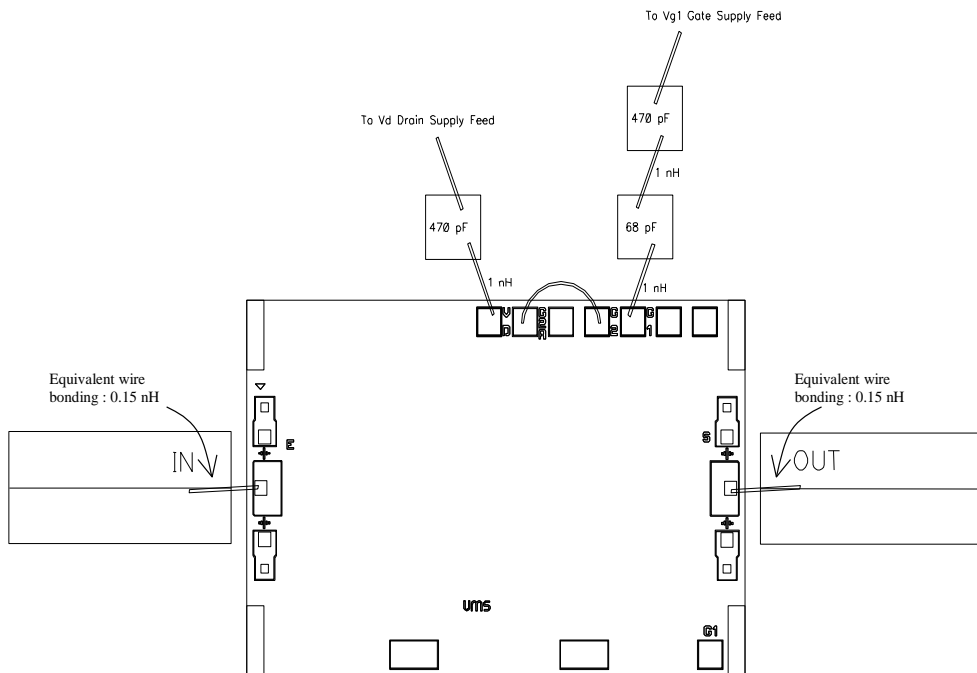
Gain & Return Loss vs Frequency



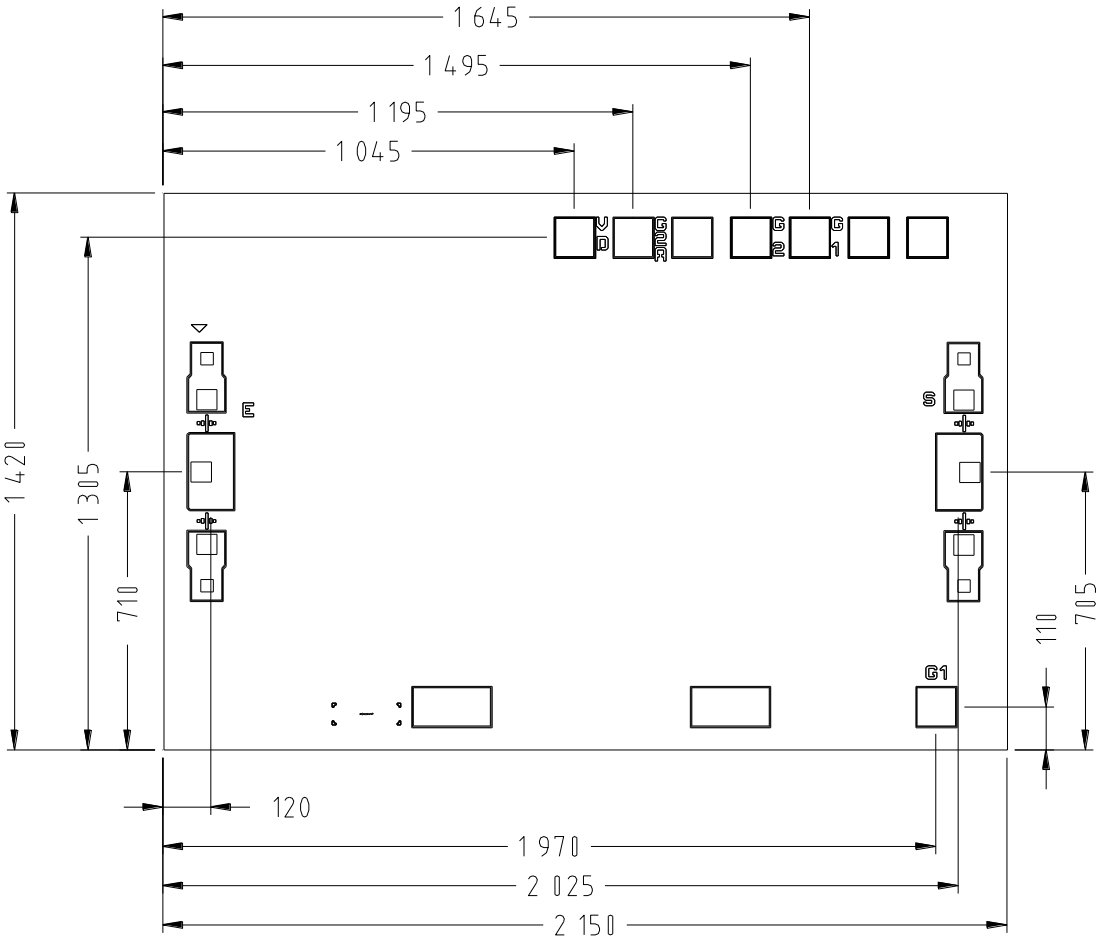
Mechanical data



The CHA3023-99F could be used without Vg2 bias. There is a resistor bridge inside the chip. This one generates the correct value of Vg2 Bias. Pads G2a and G2 must be connected. Equivalent RF Wire Bondings: 0.15 nH (typical length of 200µm for a 25µm diameter wire).



Bonding pad positions



UNITS : μm
Tol : $\pm 35 \mu m$

Chip Thickness: 100um
Chipsize: 2150X1420 $\pm 35 \mu m$



Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Ordering Information

Chip form:

CHA3023-99F/00

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