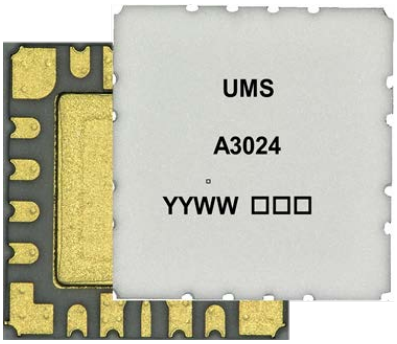
2-22GHz LNA with AGC

GaAs Monolithic Microwave IC in SMD hermetic leadless package

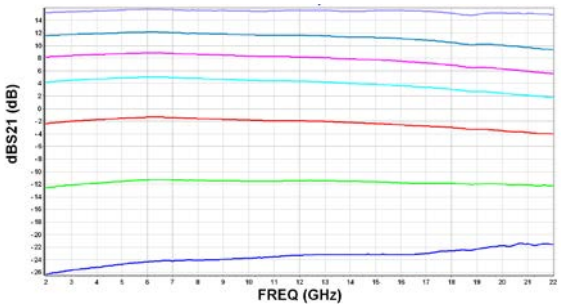
Description

The CHA3024-FDB is a distributed Low Noise Amplifier with Adjustable Gain Control (AGC) which operates between 2 and 22GHz.
It is designed for a wide range of applications, such as electronic warfare, X and Ku Point to Point Radio, and test instrumentation.
The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 2-22GHz
- Typical Linear Gain : 15dB
- Up to 30dB adjustable gain with V_{G2}
- P_{1dB}=18dBm
- P_{SAT}=22dBm
- Typical Noise Figure NF=3dB
- DC bias : V_D=5V@I_D=100mA, V_{G1}=-0.3V and V_{G2}=1.7V



Main Electrical Characteristics

Tamb.= +25°C V_D=+5V V_{G2}=1.7V V_{G1} set to have I_{DQ}=100mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2		22	GHz
Gain	Linear Gain		15		dB
NF	Noise Figure		3		dB
Pout	Output Power @1dB comp.		18		dBm

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Specifications

Tamb.= +25°C V_D=+5V V_{G2}=1.7V V_{G1} set to have I_{DQ}=100mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2		22	GHz
Gain	Linear Gain	14	15		dB
ΔG	Gain control		30		dB
NF	Noise Figure		3		dB
IRL	Input Return Loss		10		dB
ORL	Output Return Loss		10		dB
P_{1dB}	Output power for 1dB Gain Compression		18		dBm
P_{sat}	Saturated output power		22		dBm
I_{DQ}	Quiescent current on Vd		100		mA
V_D	Supply voltage on Vd	4.5	5	5.5	V
I_D	Drain current @3dB gain compression		125		mA

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V_D	Drain bias voltage	7V	V
I_{DQ}	Drain bias current	190	mA
V_{G1}	Gate bias voltage	-2 to 0	V
V_{G2}	Gate bias voltage (AGC)	-2 to 2	V
P_{IN}	Maximum CW input power overdrive	15	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (2) (3)

Tamb = +25°C

Symbol	Parameter	Values	Unit
V_D	Drain bias voltage	5.5	V
I_{DQ}	Drain bias current	150	mA
V_{G1}	Gate bias voltage	-1.5 to -0.2	V
V_{G2}	Gate bias voltage (AGC)	-1 to 1.7	V
P_{IN}	Maximum CW input power overdrive	12	dBm

(2) Electrical performances are defined for specified test conditions
(3) Electrical performances are not guaranteed over all recommended operating conditions

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Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

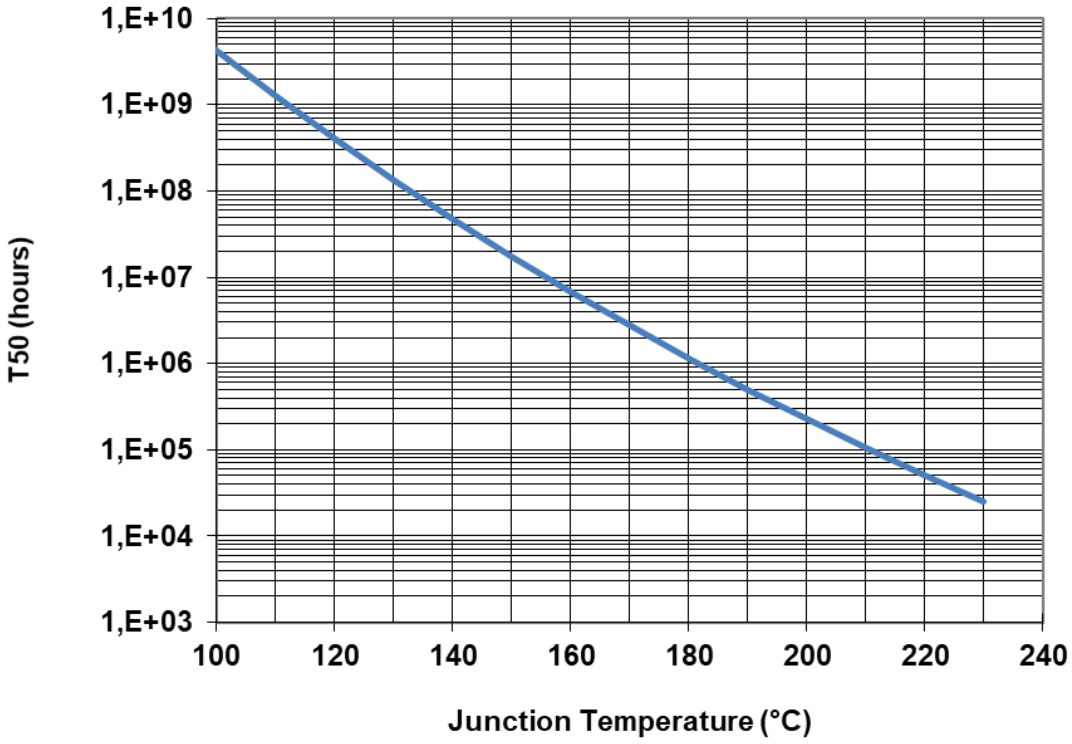
Symbol	Pad Nº	Parameter	Values	Unit
V_{G1}	5	Maximum Gain	-0.3	V
V_{G2}	18	Mean value to reach I_{DQ}=100mA	1.7	V
V_D	14	Drain bias voltage	5	V

Device thermal performances

The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	V_D=5V I_D=100mA P_{DISS}=0.5W	145	40	3E+07

[1] Assuming 85°C Tcase



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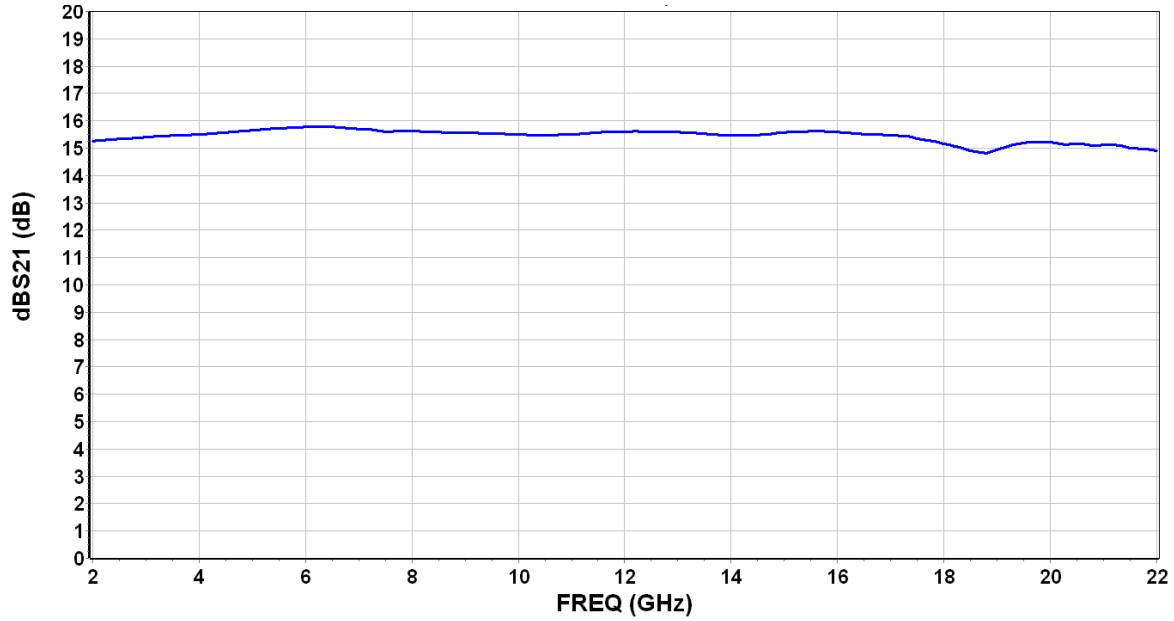
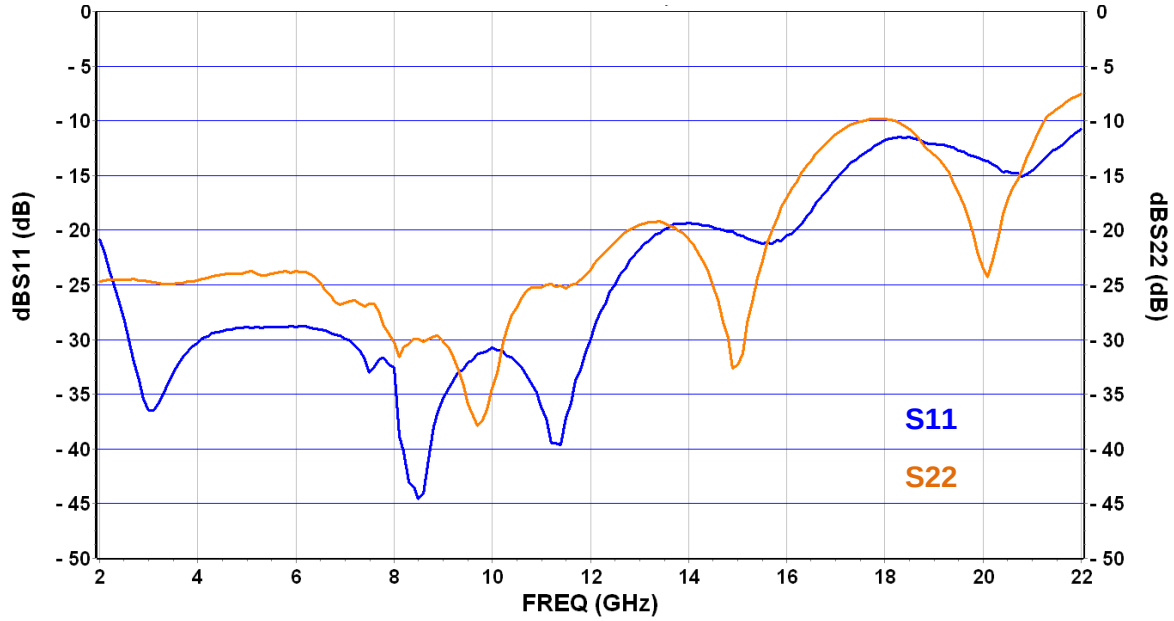
Typical Board Measurements

Tamb.= +25°C V_D=+5V V_{G2}=1.7V V_{G1} set to have I_{DQ} =100mA
Measurements in the package access planes

Linear Gain versus Frequency



Return Loss Versus Frequency



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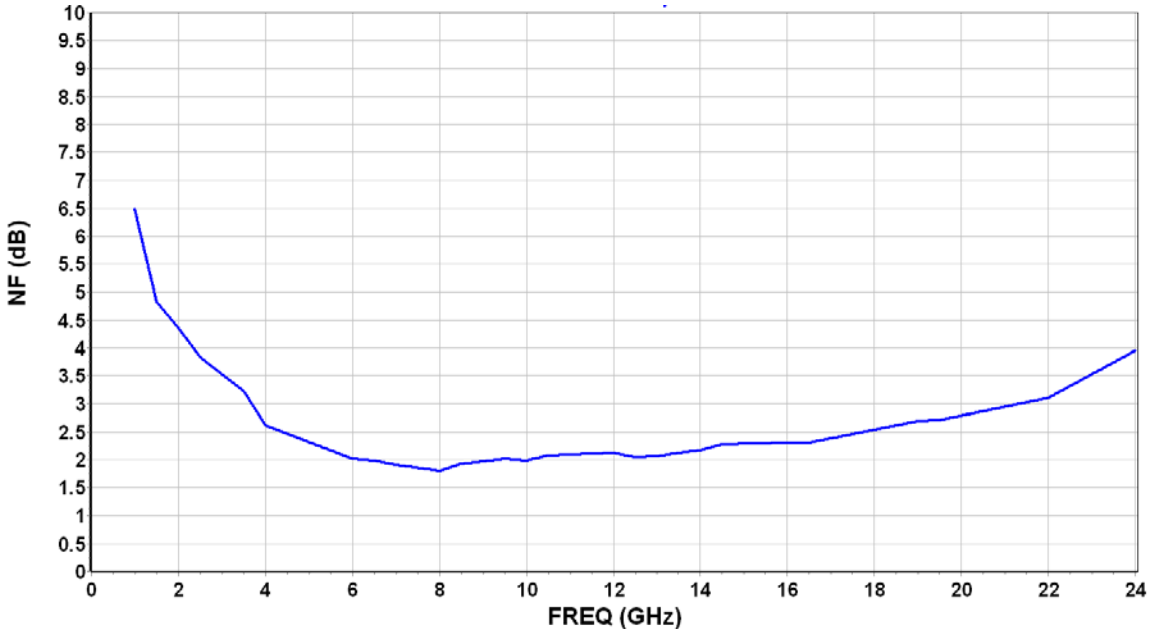
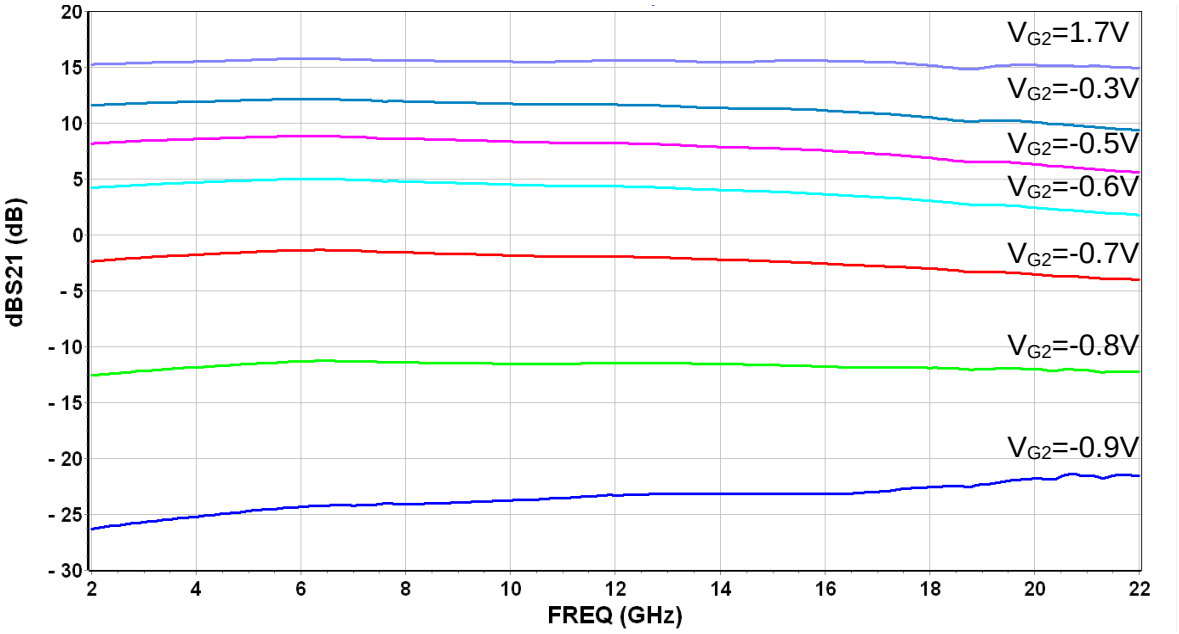
Typical Board Measurements

Tamb.= +25°C V_D=+5V V_{G2}=1.7V V_{G1} set to have I_{DQ} =100mA
Measurements in the package access planes

Noise Figure versus Frequency



Gain tuning with VG2 at VD=+5V and IDQ=100mA



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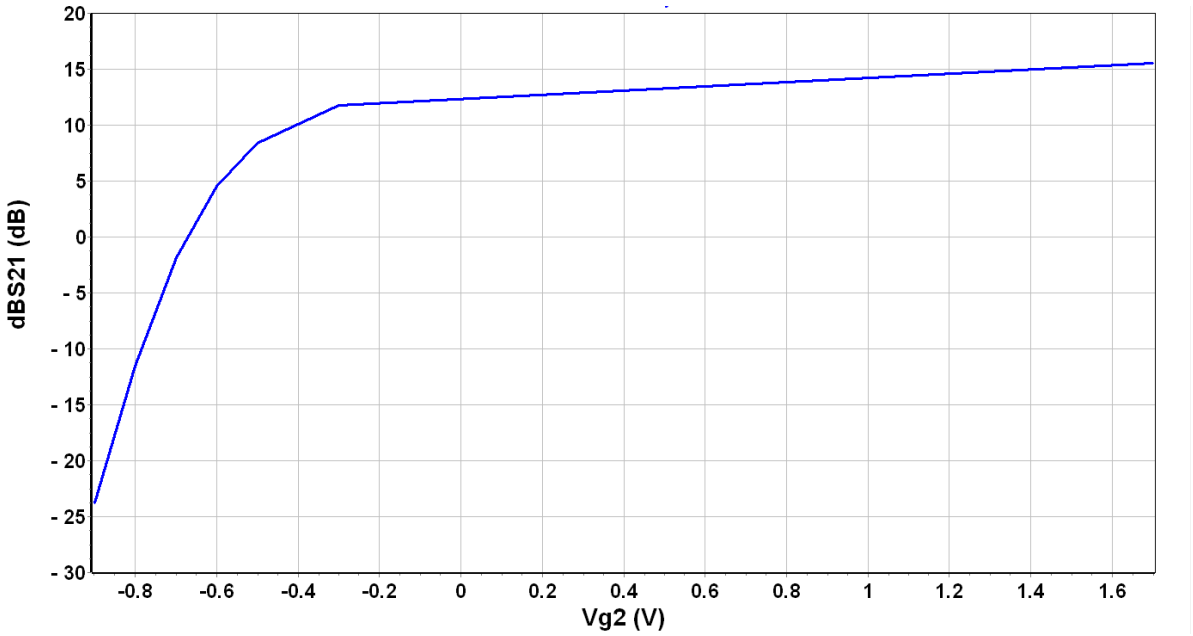
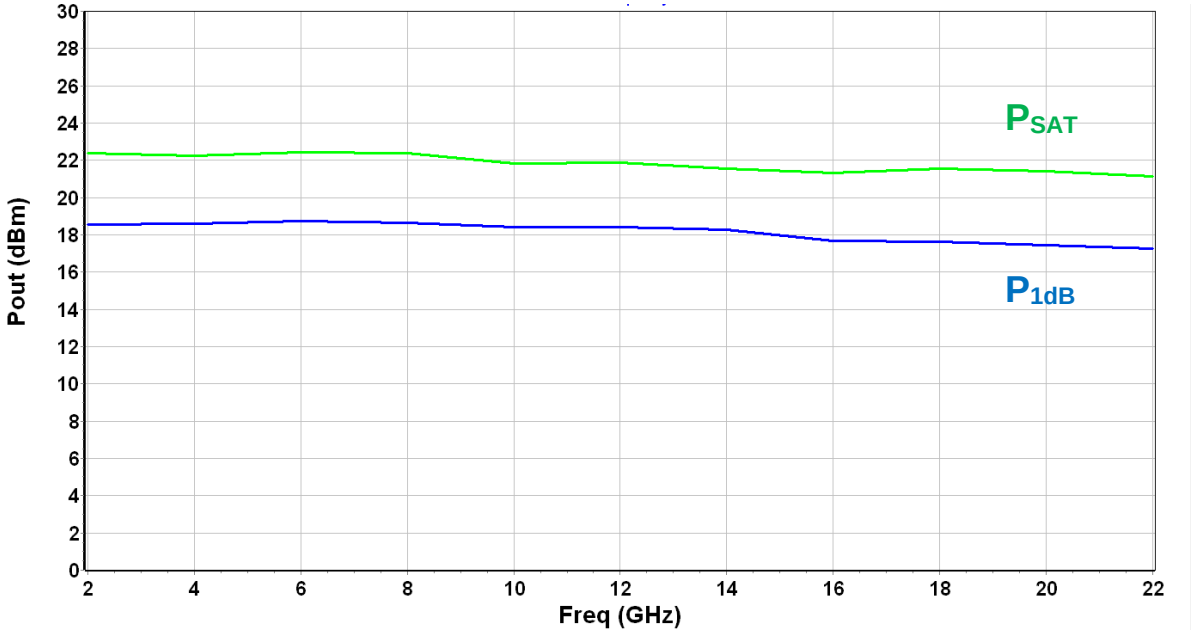
Typical Board Measurements

Tamb.= +25°C V_D=+5V V_{G2}=1.7V V_{G1} set to have I_{DQ} =100mA
Measurements in the package access planes

Linear gain versus V_{G2} control voltage @freq=10GHz



P_{out} compression level versus Frequency



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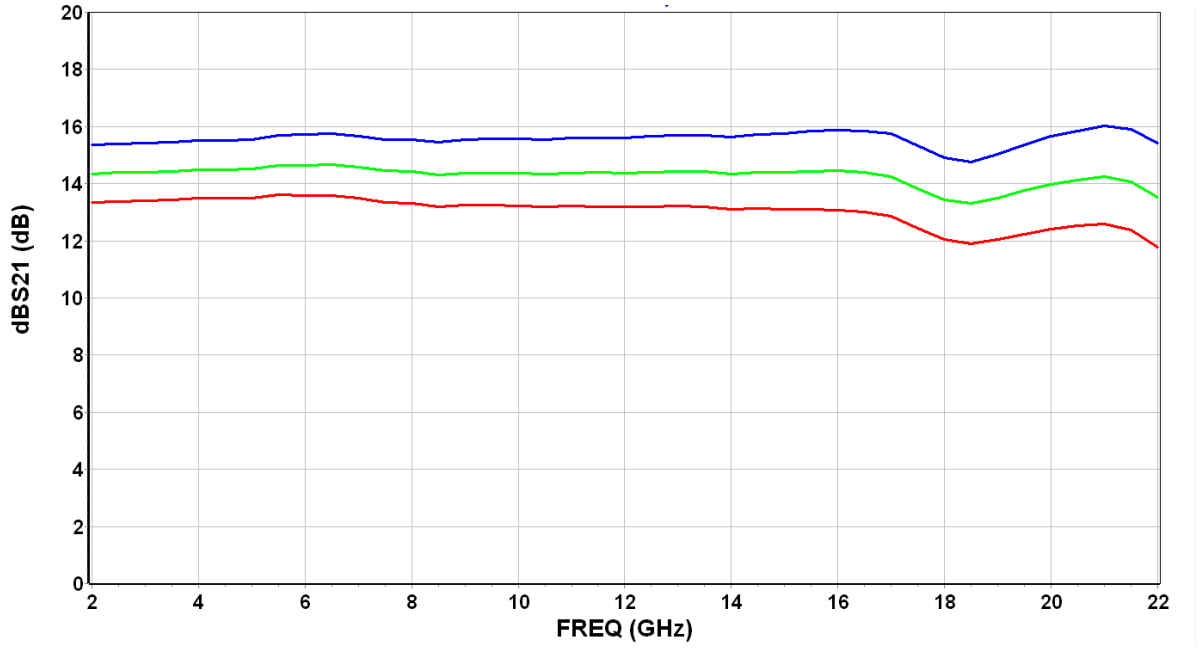
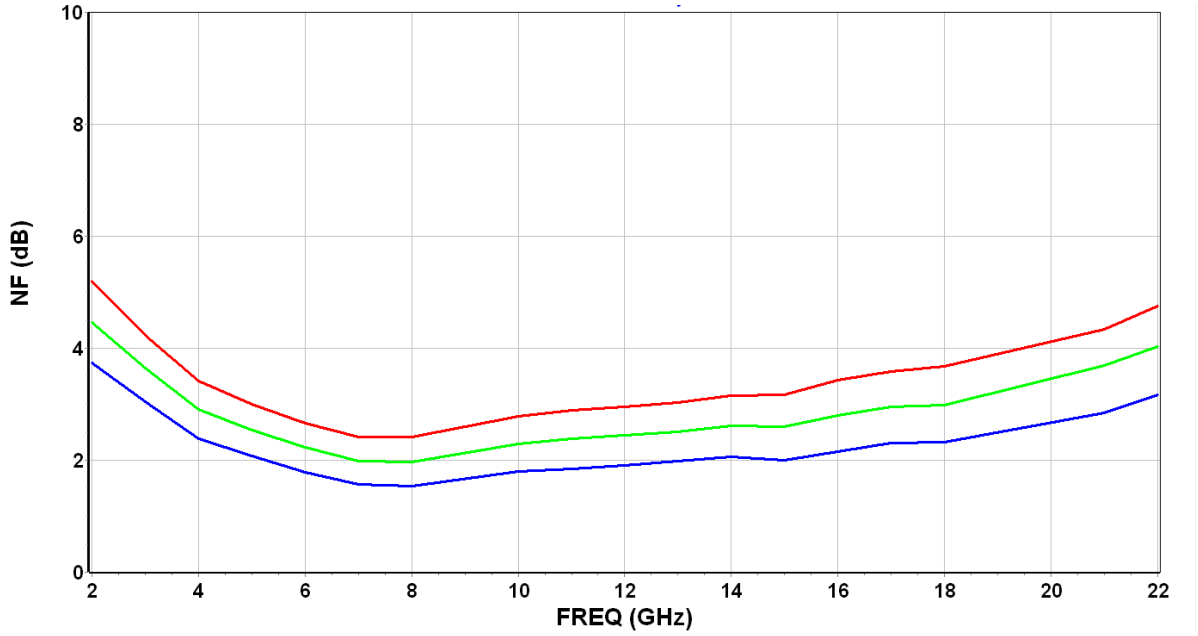
Typical Board Measurements

Tamb.= **-40** / **+25** / **+85**°C V_D=+5V V_{G2}=1.7V V_{G1} set to have I_{DQ} =100mA
Measurements in the Board access planes

Linear Gain versus Frequency



Noise Figure versus Frequency



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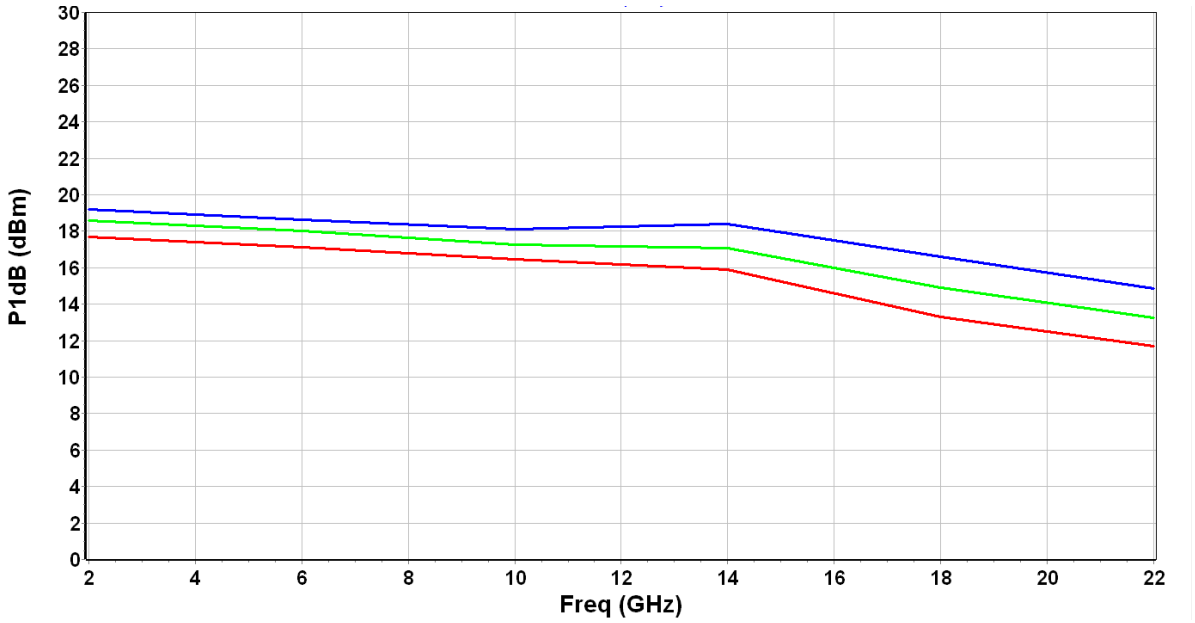
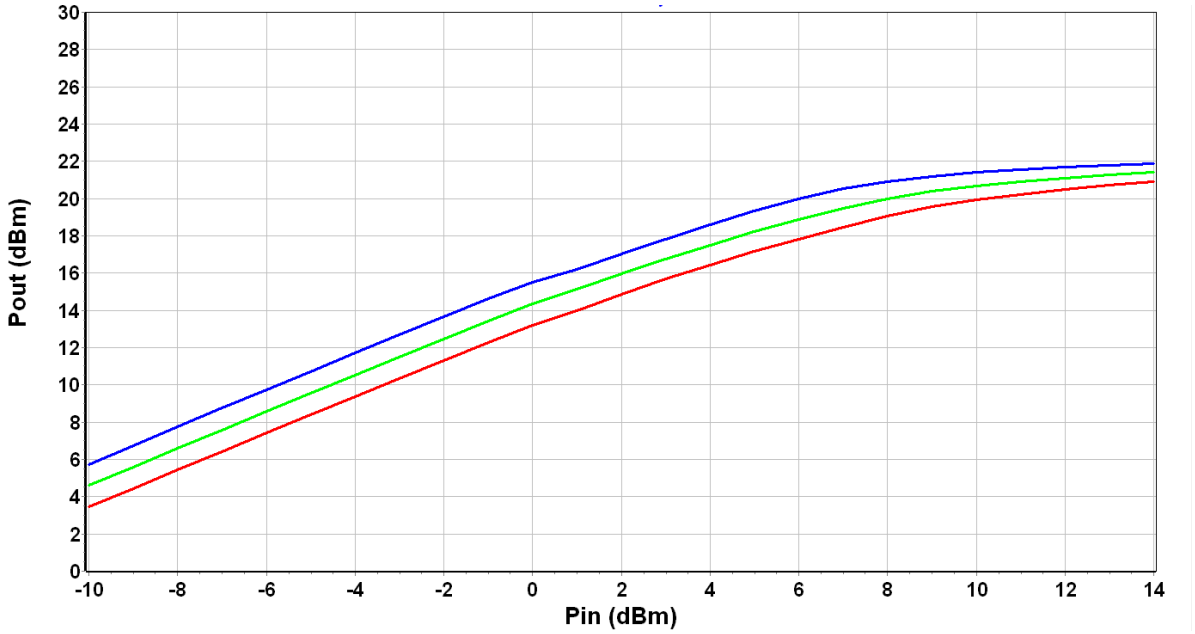
Typical Board Measurements

Tamb.= **-40** / **+25** / **+85**°C V_D=+5V V_{G2}=1.7V V_{G1} set to have I_{DQ} =100mA
Measurements in the Board access planes

Output power at 1dBc versus frequency



Output power versus Input power @freq=10GHz



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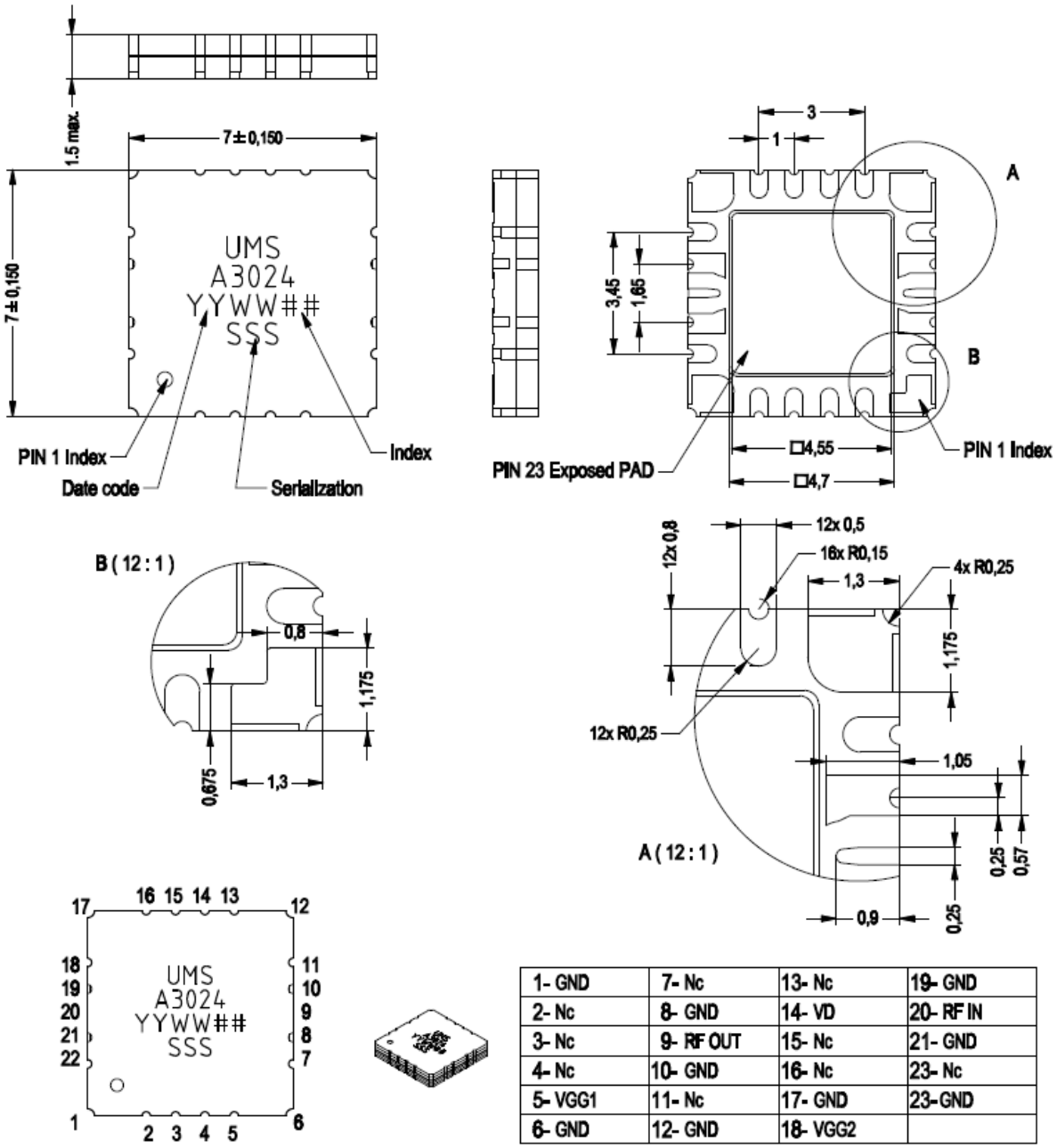
Package outline (1)



1- GND	7- Nc	13- Nc	19- GND
2- Nc	8- GND	14- VD	20- RF IN
3- Nc	9- RF OUT	15- Nc	21- GND
4- Nc	10- GND	16- Nc	23- Nc
5- VGG1	11- Nc	17- GND	23-GND
6- GND	12- GND	18- VGG2	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0029 (https://www.ums-rf.com) for exact package dimensions.

It is strongly recommended to ground all pins marked “Nc” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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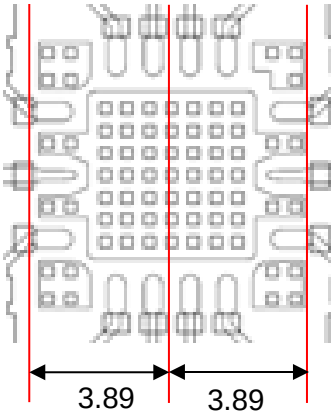
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.89mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Package Information

Parameter	Value
Package body material	RoHS-compliant
Lead finish	Gold
Hermetic sealing (fine leak compliant Mil-Std-883 Method 1014.10 Condition A4, tracer gas He at 1atm)	$1x10^{-8}$ ccHe/s/atm

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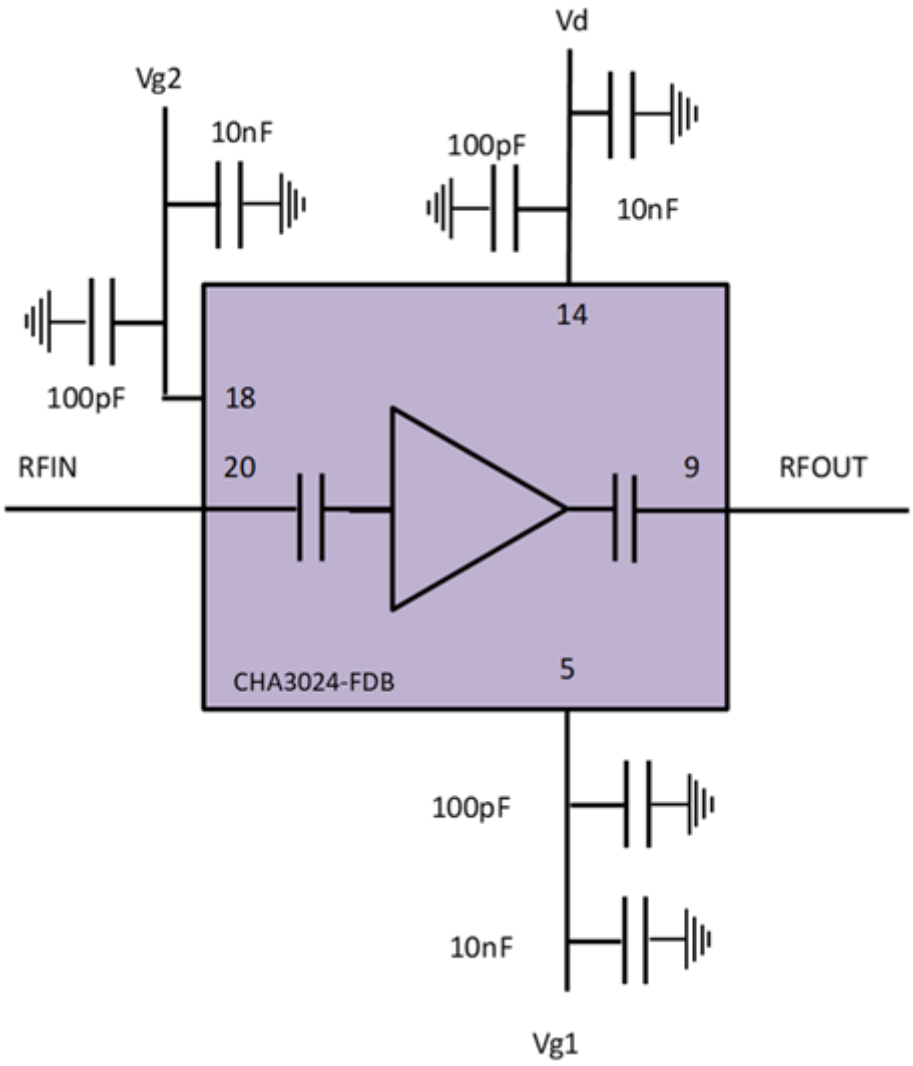
Recommended assembly plan



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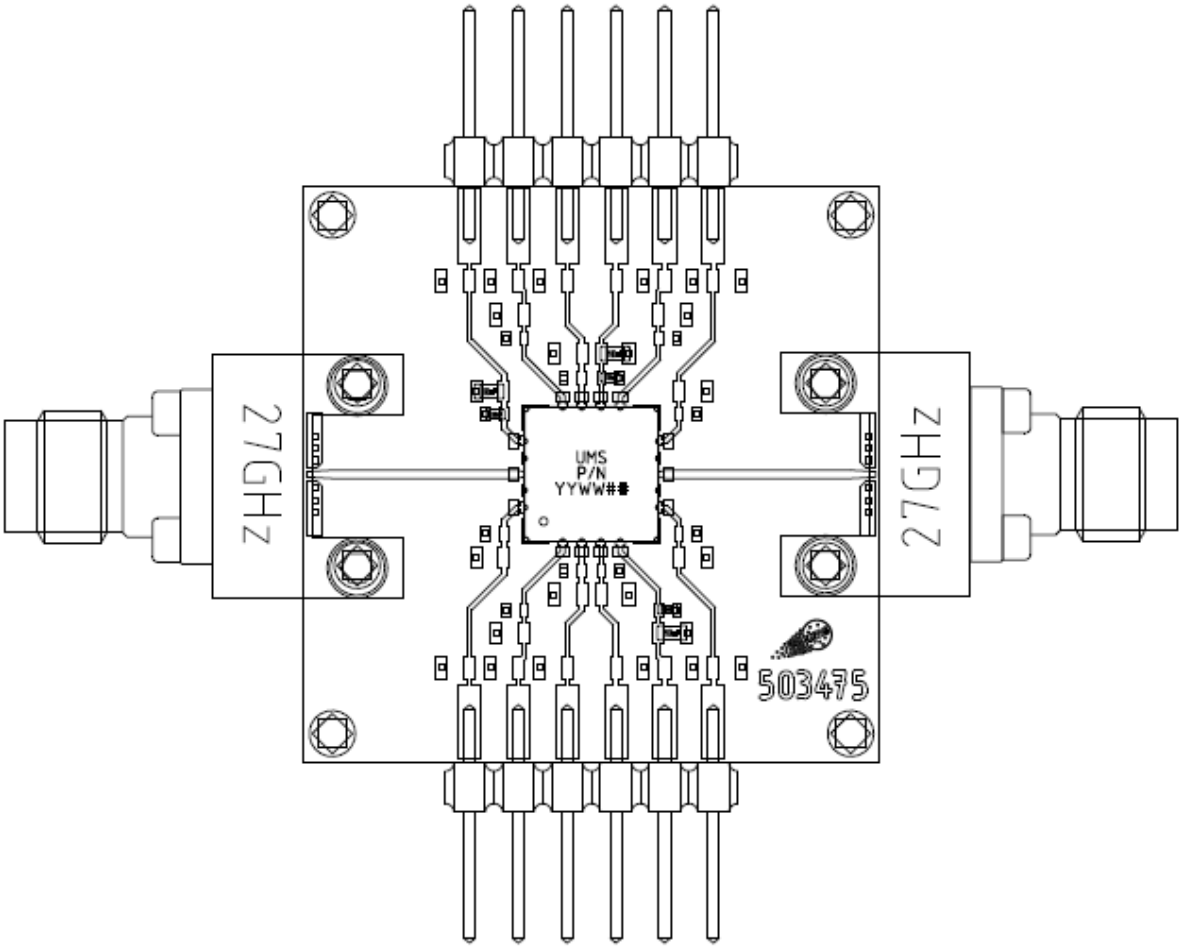
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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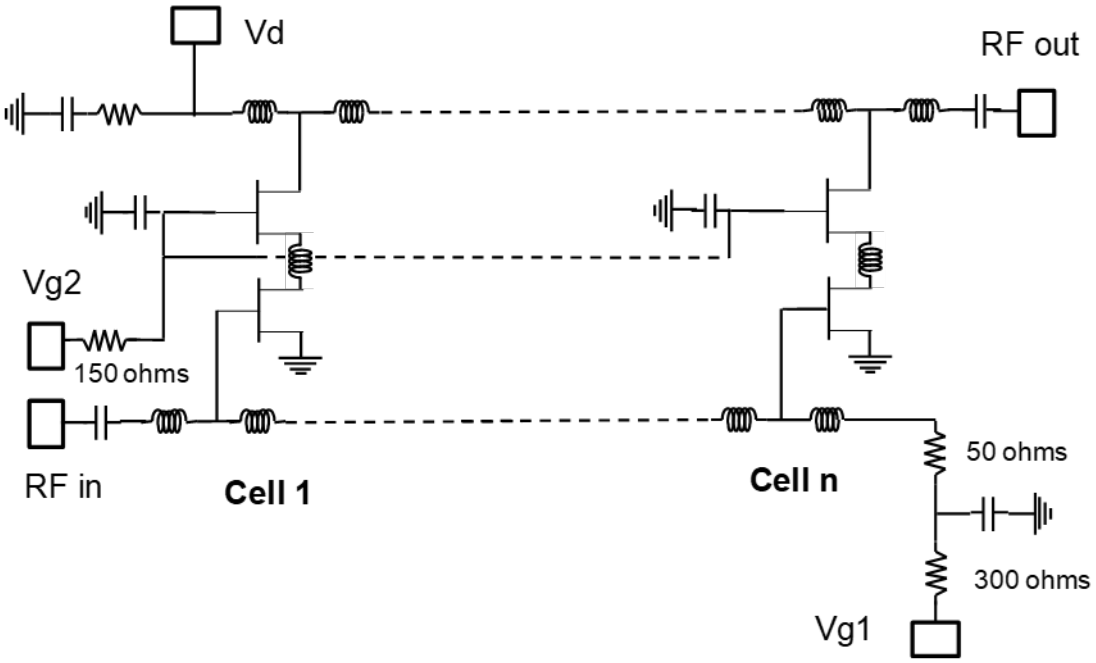
DC Schematic



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Recommended package footprint for FDB Package

Refer to the application note AN0029 available at https://www.ums-rf.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure for FDB Package

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0029 available at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

FDB 7x7 package:	CHA3024-FDB/XY Waffle: XY = 24

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