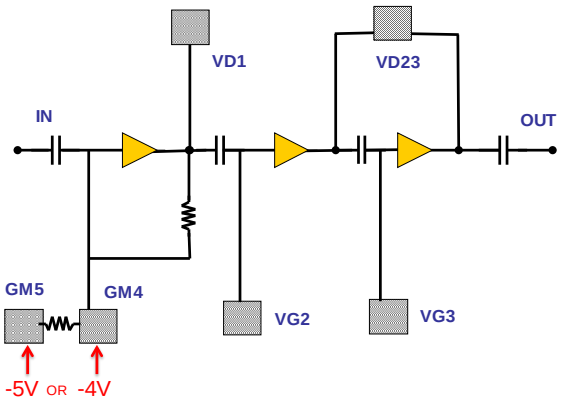
CHA3409-98F

25-45GHz Driver

GaAs Monolithic Microwave IC in bare die

Description

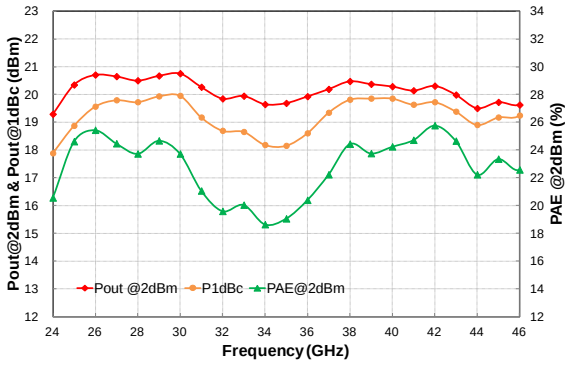
The CHA3409-98F is a 3 stage monolithic Medium Power Amplifier, which produces 23dB linear gain and 19dBm output power. It includes a self-biasing on the first stage, which reduces the impact of temperature and technology variations.
It is well suited for a wide range of application from military to commercial communication systems and test instrumentation.
This product is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in bare die with BCB protection layer.



Main Features

- Broadband performances: 25-45GHz
- 19dBm Pout at 1dB compression
- 23dB linear gain
- 19% of PAE @ 1dBc
- DC bias: Vd=4Volt @ Id=100mA
- Chip size 2x1.3x0.1 (mm)

Output power & PAE vs frequency



Main Electrical Characteristics

Tamb = +25°C, Vg_{stg1}=-4V, Vd=4V, Idq=100mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	25		45	GHz
Gain	Linear Gain		23		dB
P-1dB	Output Power @1dB comp.		19		dBm
Psat	Saturated output power		20		dBm
PAE	PAE @1dB comp.		19		%

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Specifications (CW mode)

Tamb=+25°C, Vd=+4.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	25		45	GHz
Gain	Linear Gain		23		dB
ΔG	Gain variation in temperature		± 0.03		dB/°C
P_{-1dB}	Output power @ 1dB gain compression		19		dBm
Psat	Saturated Output Power		20		dBm
PAE	PAE at saturation		19		%
NF	Noise figure		6.5		dB
RLin	Input Return Loss		-10		dB
RLout	Output Return Loss		-11		dB
Idq	Quiescent Drain current		100		mA
Vg	Gate voltage of 2nd& 3rd stage		-0.4		V
Vg_{stg1}	Gate voltage of the 1rst stage		-4		V

These values are representative of measurement in test fixture with a bonding wire of typically 0.25nH to 0.3nH.

Typical Bias Conditions

Tamb = +25°C

Symbol	Parameter	Values	Unit
GM4	GM4 **OR** GM5 DC Gate voltage : 1st stage	-4	V
GM5		-5	V
G2(1)	DC Gate voltage : 2nd stage	-0.4	V
G3(1)	DC Gate voltage : 3rd stage	-0.4	V
D1	DC Drain voltage : 1st stage	4	V
D23	DC Drain voltage : 2nd & 3rd stage	4	V

(1)Corresponding to Idq=100mA

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Biasing procedure

Device Power Up instructions:

1. Ground the device
2. Bias PA gate voltage at Vgs close to Vpinch-off (example: 1st stage Vgs ≈ -7V and 2nd & 3rd stage Vgs ≈ -1.5V)
3. Apply Vds quiescent bias voltage (Example: Vd = 4V)
4. Increase slowly 1st stage Vgs (GM4) up to -4V and 2nd & 3rd stage Vgs up to quiescent bias drain current Idq (100mA for total Idq current)
5. Apply RF input power

Device Power Down instructions:

1. Remove RF input power
2. Decrease MPA gate voltage down to Vgs -1.5V for the 2nd & 3rd stage Vgs and -7V for the first one
3. Decrease drain voltage down to 0V

Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	8	V
Idq	Drain bias current	200	mA
Vg	Gate bias voltage of 2nd& 3rd stage	-2.5 to 0	V
Pin	Maximum peak input power overdrive	10	dBm
Tj	Junction temperature under ROR conditions	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range (3) (4)

Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	3 to 5	V
Idq	Drain bias current	100	mA
Vg	Gate bias voltage of 2nd& 3rd stage	-2.5 to 0	V
Vg_{stg1}	Gate voltage of the 1rst stage (GM4 or GM5)	-4 or -5	V
Pin	Maximum peak input power overdrive	10	dBm

(3) Electrical performances are defined for specified test conditions

(4) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Tamb	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Device thermal information

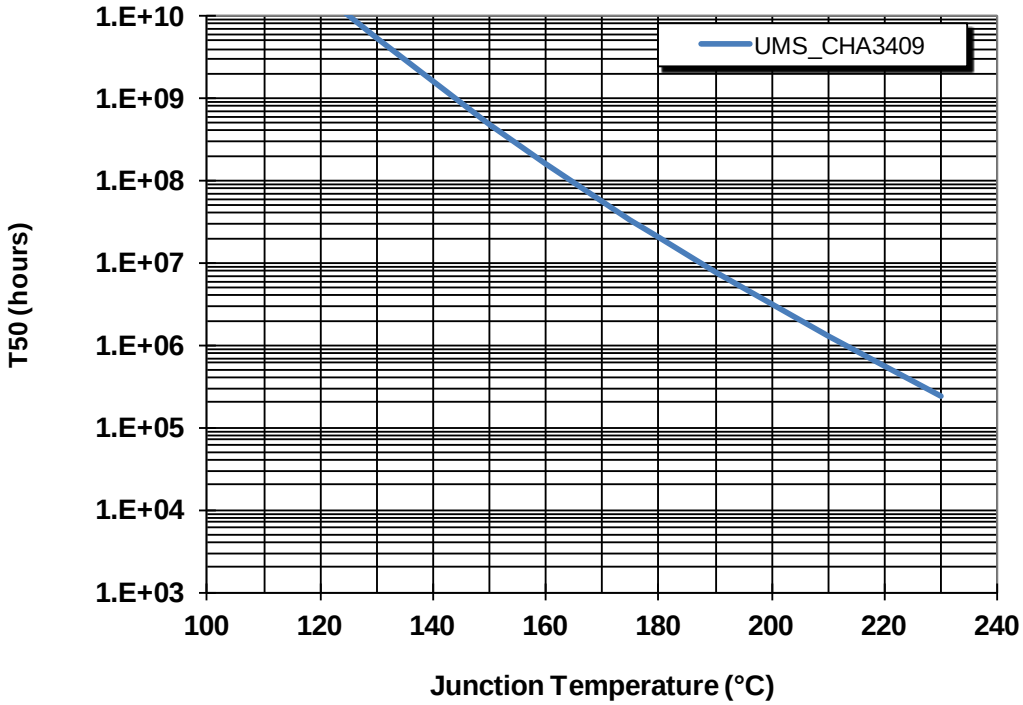
The device thermal performances below are based on UMS rules to evaluate the junction temperature.
The temperature Tb_{chip} is defined as the chip back side. The thermal resistance (Rth_eq) is given for the full circuit, and assumes CW operation mode in the table.

Thermal Resistance(1)	Rth_eq	Tb_{chip} =85°C, Vd=4V, Vg_{stg1}=-4V, Idq=100mA Pin=-10dBm, Pout=11dBm, Pdiss=390mW	116	°C/W
Junction Temperature	Tj		160	°C

(1) Thermal resistance given from junction to back side of the chip

Thermal Resistance(1)	Rth_eq	Tb_{chip} =85°C, Vd=4V, Vg_{stg1}=-4V, Idq=100mA Pin=2dBm, Pout=20dBm, Pdiss=355mW	116	°C/W
Junction Temperature	Tj		154	°C

(1) Thermal resistance given from junction to back side of the chip. Thermal analysis is highly recommended, more details are available on request.

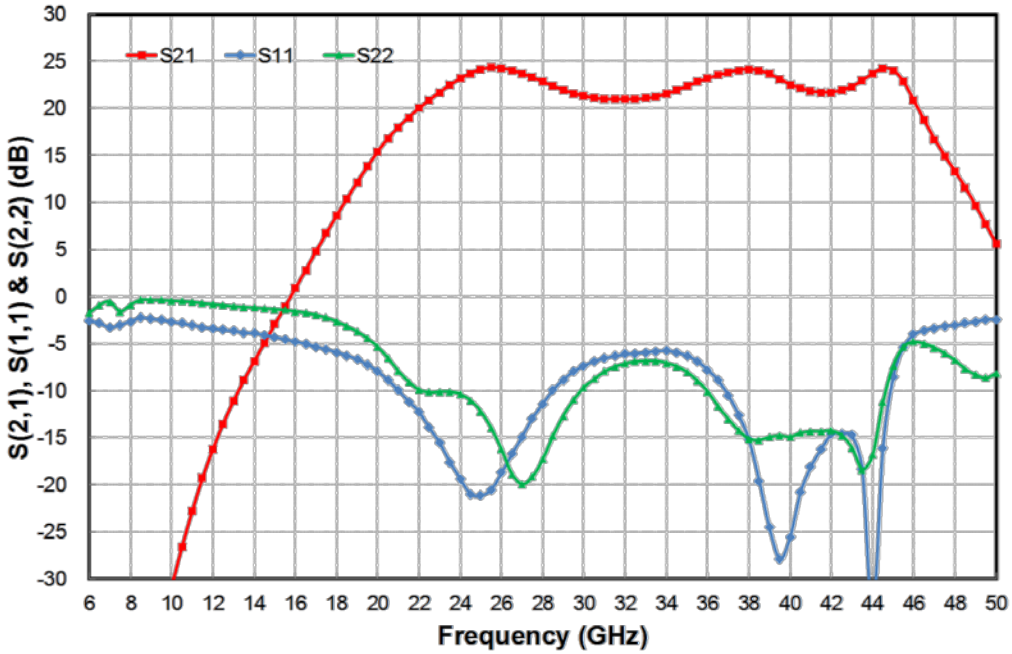


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

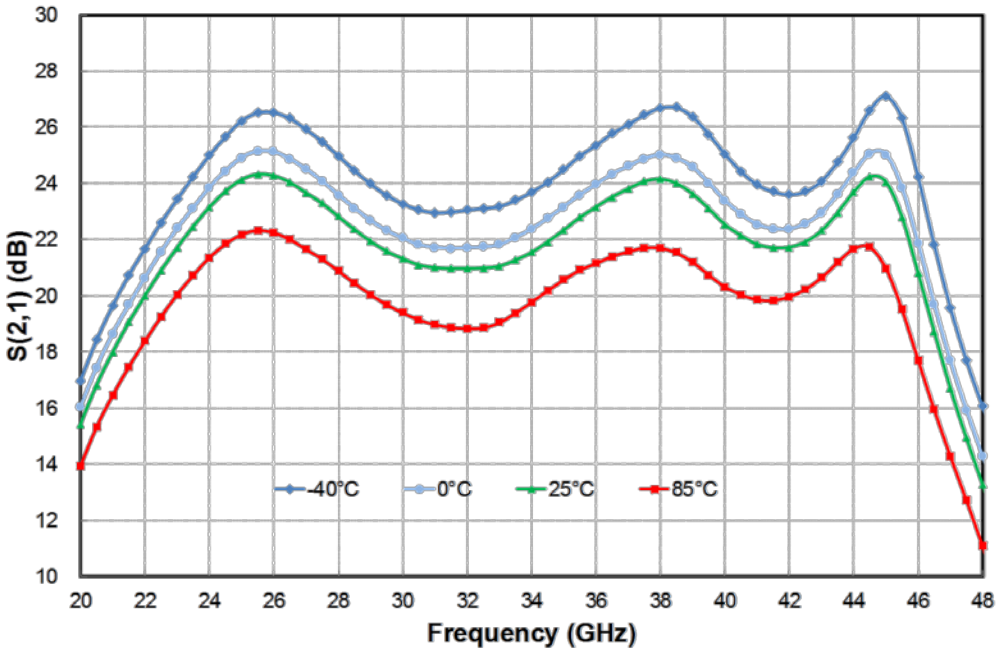
Typical On Board Sij Measurements

Tamb = +25°C, Vd = +4V, Vg1=-4V, other Vg fixed for Idq = 100mA@25°C
Measurement performed on test board in the bonding wire access plans on the PCB.

Small Signal Gain (dB) and Input and Output Return Losses (dB) @25°C



Small Signal Gain (dB) versus Frequency (GHz) and temperature (°C)

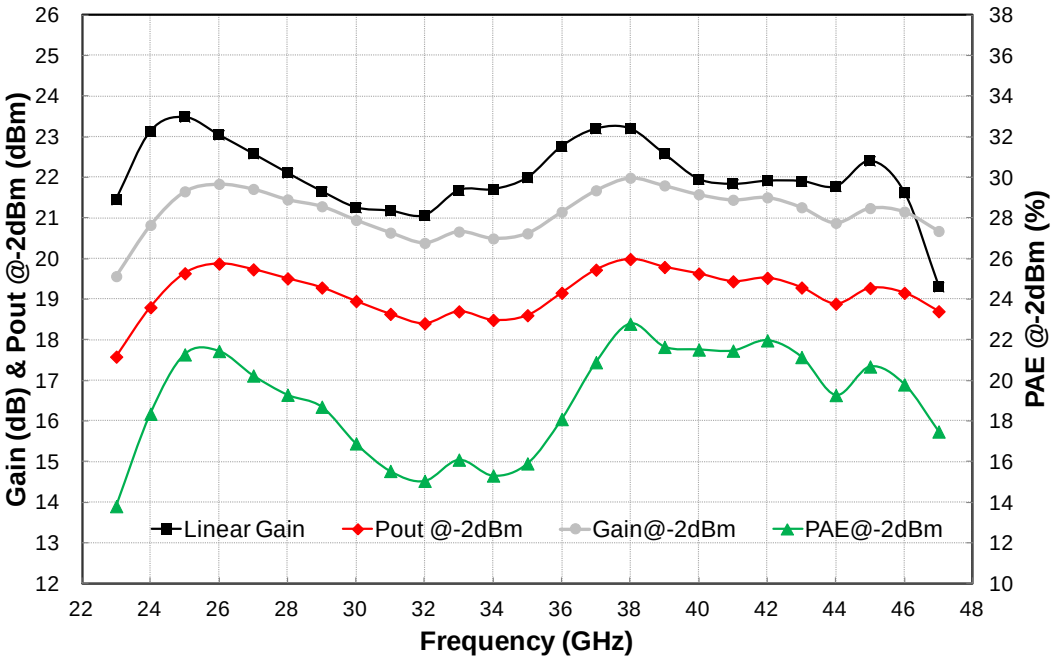


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

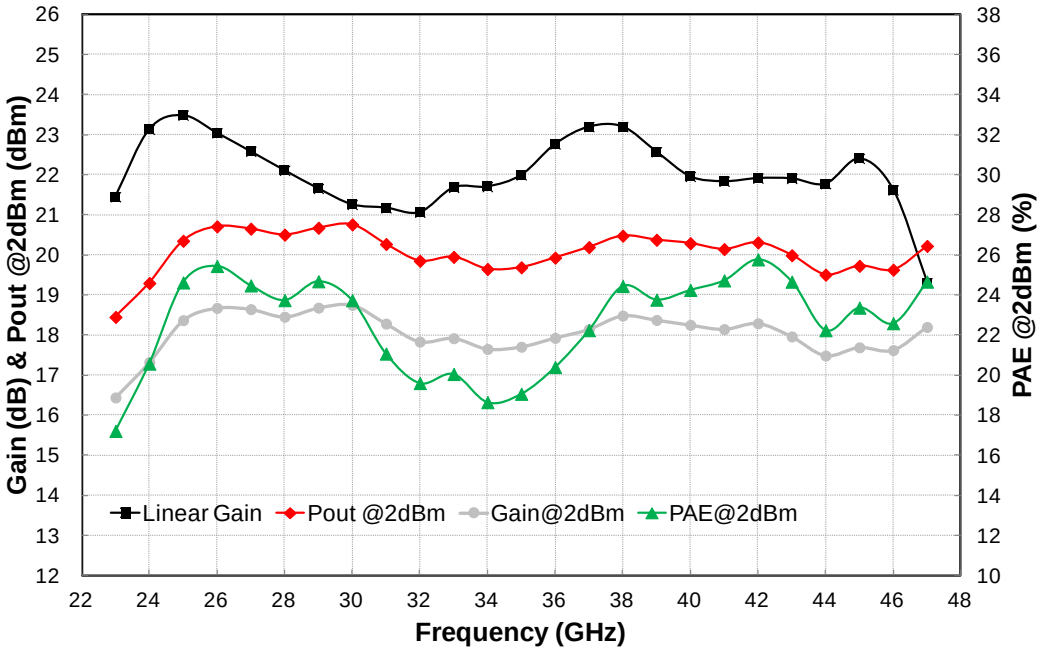
Typical On Board Measurements (CW)

Tamb = +25°C, Vd = +4V, Vg1=-4V, other Vg fixed for Idq = 100mA@25°C
Measurement performed on test board in the bonding wire access plans on the PCB.

Linear Gain & Gain, Pout & PAE versus Frequency @Pin=-2dBm



Linear Gain & Gain, Pout & PAE versus Frequency @Pin=2dBm

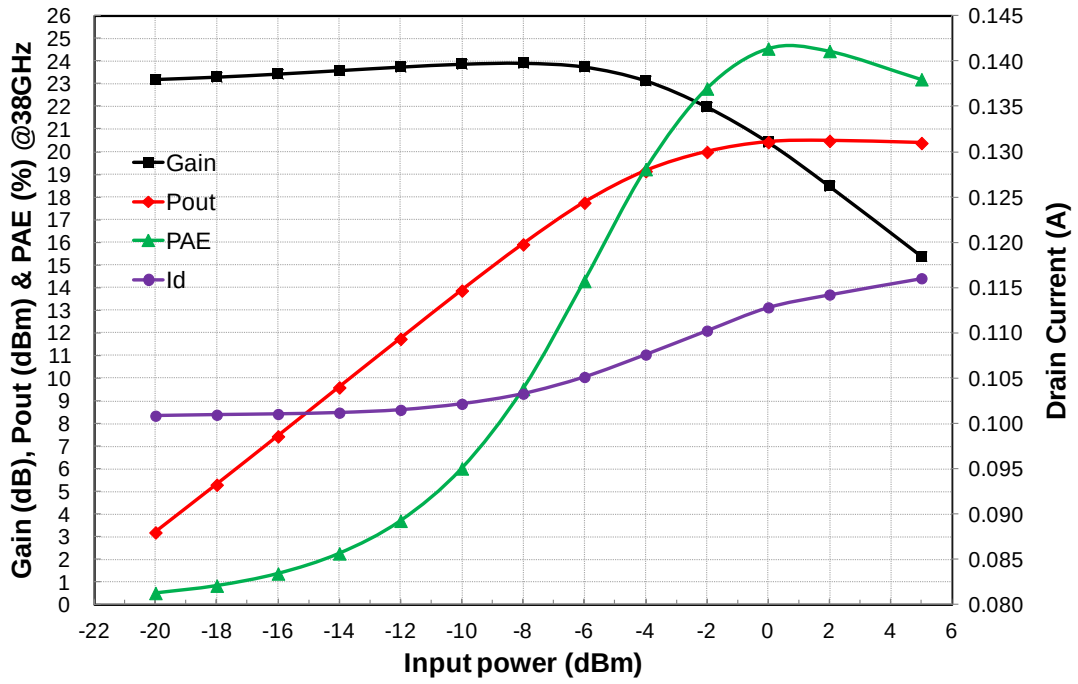


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

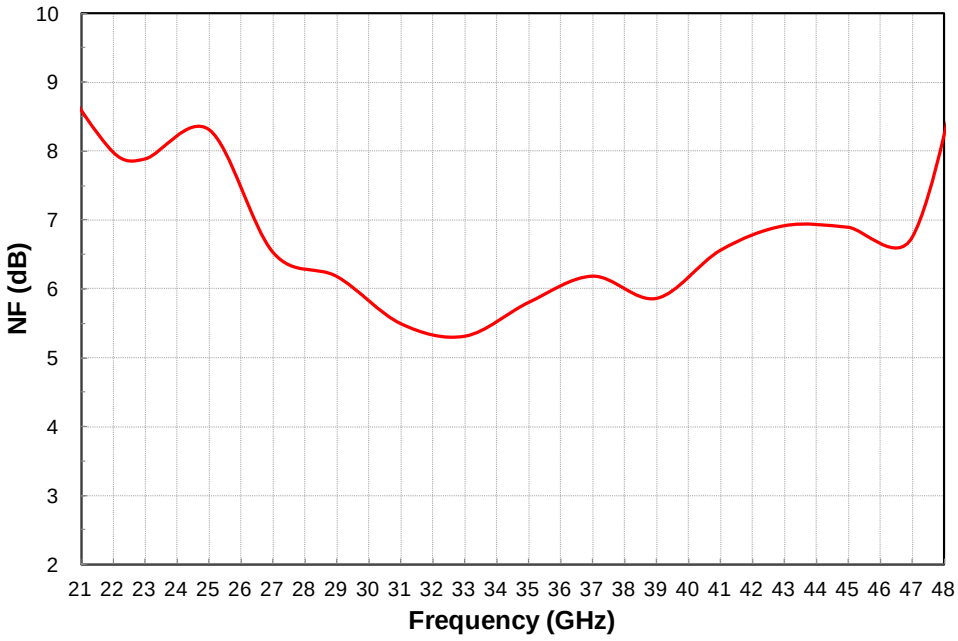
Typical On Board Measurements (CW)

Tamb = +25°C, Vd = +4V, Vg1=-4V, other Vg fixed for Idq = 100mA@25°C
Measurement performed on test board in the bonding wire access plans on the PCB.

Gain, Pout, PAE & Id versus Pin @Freq=38GHz

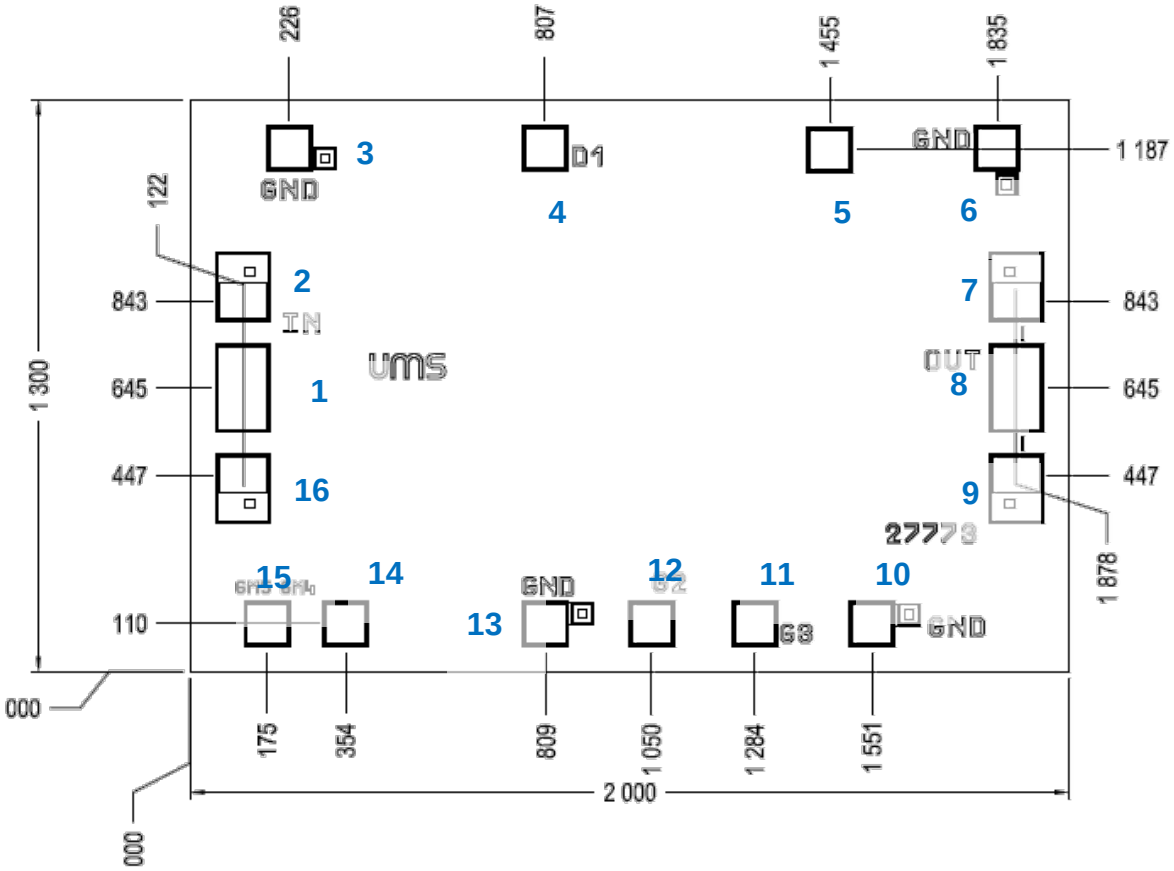


Noise Figure @25°C versus Frequency



Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Mechanical data



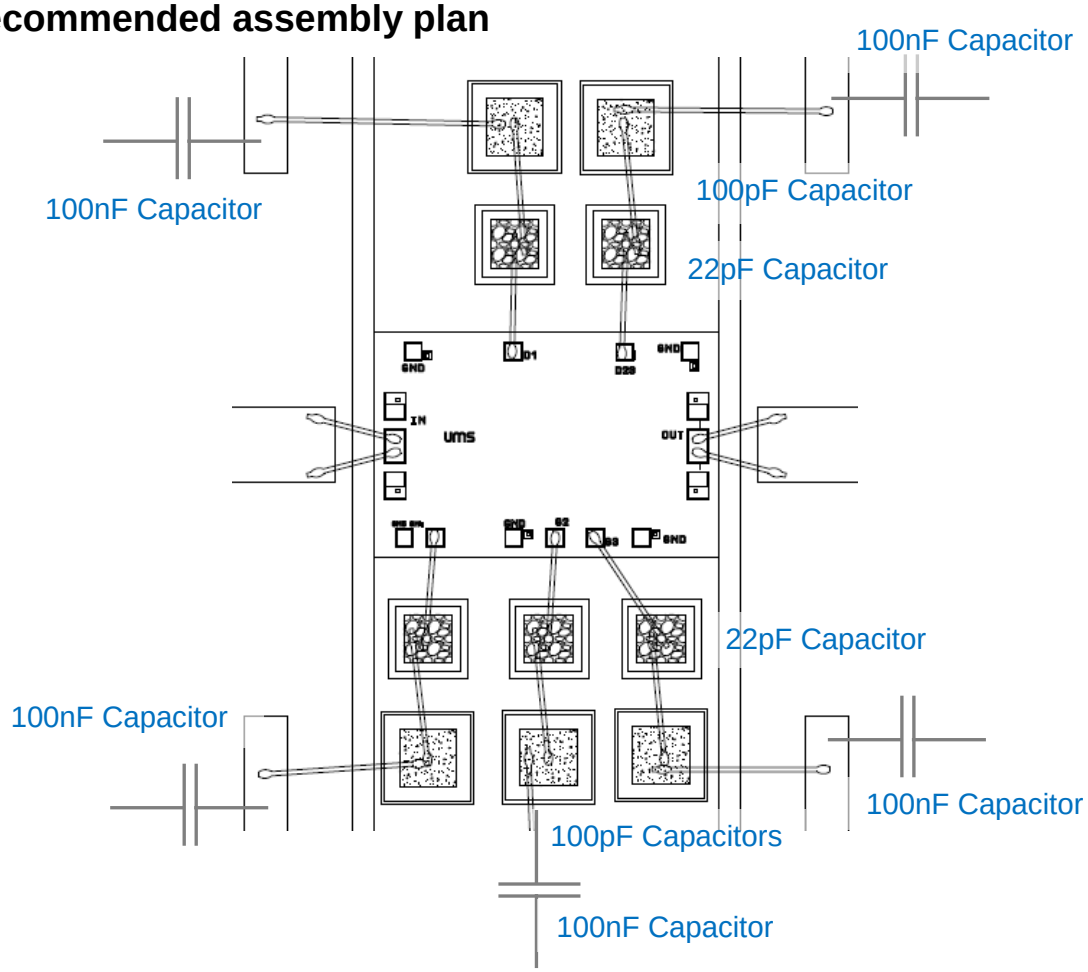
Tolerance chip size : +/-50µm
Chip thickness: 70µm.
All dimensions are in micrometers

PAD Number	Name	Description	Pad size (BCB Opening)
1	IN	Input RF port	186um x 110um
2, 7, 9, 16	GND	Ground cross to RF Pad	82um x 108um
3, 6, 10, 13	GND	Ground	90um x 90um
4	D1	DC Drain voltage 1rst stage	90um x 90um
5	D23	DC Drain voltage 2nd & 3rd stage	90um x 90um
8	OUT	Output RF port	186um x 110um
11	G3	DC Gate voltage 3rd stage	90um x 90um
12	G2	DC Gate voltage 2nd stage	90um x 90um
14	GM4 (1)	DC Gate voltage 1rst stage : If -4V	90um x 90um
15	GM5 (1)	DC Gate voltage 1rst stage : If -5V	90um x 90um

(1): Only 1 pad between GM4 and GM5 has to be connected, depend on external voltage using (-4V or -5V). There is only a resistor between GM4 and GM5 Pads.

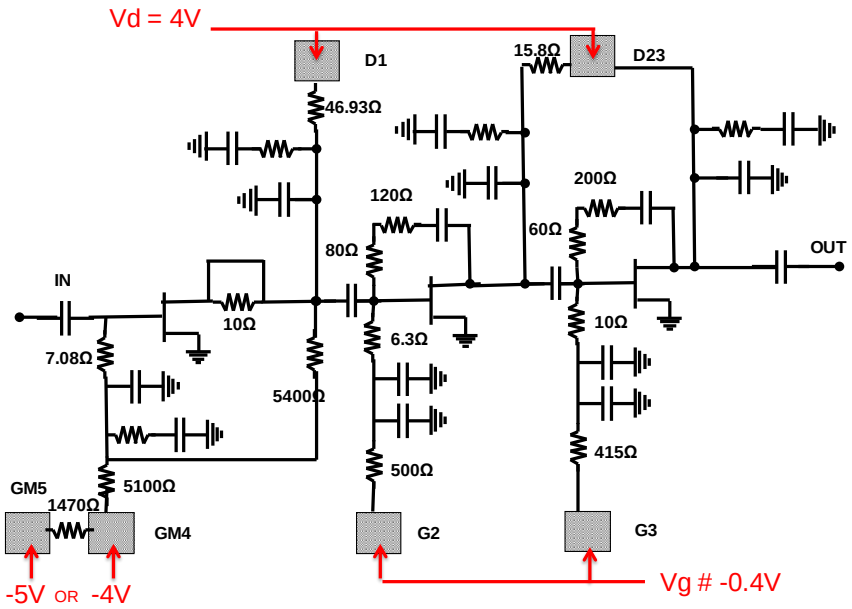
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Recommended assembly plan



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

DC Schematic



Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Chip form:	CHA3409-98F/00

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com