6-18GHz 3 bit Digital Variable Amplifier

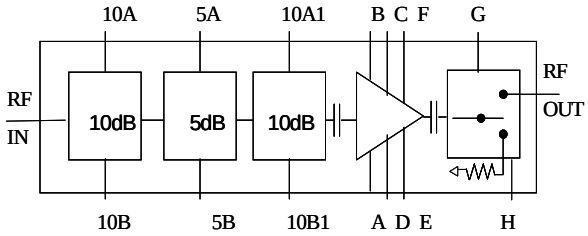
GaAs Monolithic Microwave IC

Description

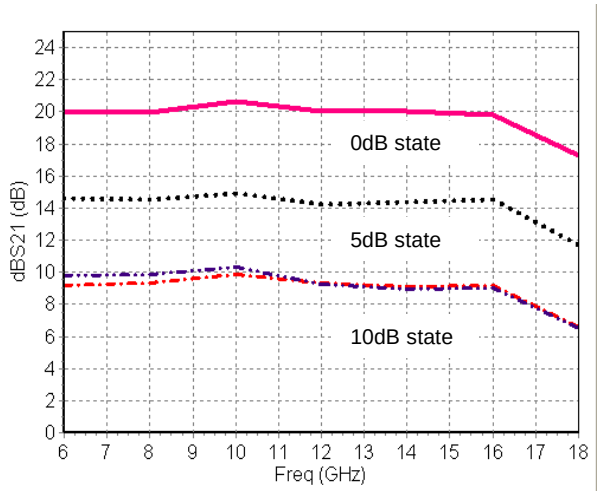
The CHA3513 is composed by a three steps digital attenuator followed by a three stage travelling amplifier and a Single Pole Single Through (SPST) switch. It is designed for defense applications. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Typical on wafer Measurements
Gain versus attenuation states



Main Features

- Performances: 6-18GHz
- 20dBm saturated output power
- 19 dB gain
- 3 bit attenuator for 26dB range
- DC power consumption, 300mA @ 4.5V
- Chip size: 6.68 x 2.46 x 0.1mm

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	6		18	GHz
G	Small signal gain @ Attenuator state 0dB		19		dB
Psat	Saturated Output power @ Attenuator state 0dB		20		dBm
ATT dyn	Attenuator range with 3bit		25		dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics on wafer

Tamb = +25℃
Vd = Pads B, D, F = 4.5V, Vg = Pads A, C, E tuned for Id = 300mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	6		18	GHz
G	Small signal gain @ Attenuator state 0dB (1)				
	6-17GHz	17	19		dB
	17-18GHz	15	16		dB
ATT bit	Attenuator bit: State 5dB	4.5	5	6.5	dB
	State 10 dB 1	9.5	10	12	dB
	State 10dB 2	9.5	10	12	dB
ATT dyn	Attenuator range with 3bit		25		dB
Is	Small signal gain @ Attenuator state 0dB & switch OFF (1)		-35		dB
P1dB	Output power at 1dB compression @ Attenuator state 0dB (1)		18		dBm
Psat	Saturated Output power @ Attenuator state 0dB (1)		20		dBm
NF	Noise figure @ Attenuator state 0dB		12		dB
RL_IN	Input Return Loss all attenuator states		-15	-9	dB
RL_OUT	Output Return Loss all attenuator states & switch ON		-15	-9	dB
Vd	Drain bias DC voltage (Pads B, D, F)		4.5		V
Id	Bias current @ small signal		300	350	mA
Vc	Control voltage for Attenuator bits & SPST switch	-5		0	V

(1) These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

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Absolute Maximum Ratings

Tamb. = 25℃ (1)

Symbol	Parameter	Values	Unit
Vd	Maximum Drain bias voltage (Pads B,D,F)	+5	V
Id	Drain bias current with Vd=4.5V	450	mA
Vg	Gate bias voltage (Pads A,C,E)	-2 to +0.4	V
Vc	Attenuator bits & SPST control voltage	-7 to +0.6	V
Pin	Maximum input power overdrive (2)	+20.0	dBm
Tch	Maximum channel temperature	+175	℃
Ta	Operating temperature range	-40 to +70	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

3bit VGA Control interface

The attenuator states are controlled by 6 voltages. The SPST switch is controlled by 2 voltages.

state	Theoretical attenuation dB	Voltage CONTROL PAD						Switch control	
		10A (V)	10B (V)	5A (V)	5B (V)	10A1 (V)	10B1 (V)	G	H
0	0 référence	-5	0	-5	0	-5	0	-5	0
1	5	-5	0	0	-5	-5	0	-5	0
2	10 config.1	0	-5	-5	0	-5	0	-5	0
3	15 config.1	0	-5	0	-5	-5	0	-5	0
4	15 config.2	-5	0	0	-5	0	-5	-5	0
6	10 config.2	-5	0	-5	0	0	-5	-5	0
7	25	0	-5	0	-5	0	-5	-5	0
8	Isolation	-5	0	-5	0	-5	0	0	-5

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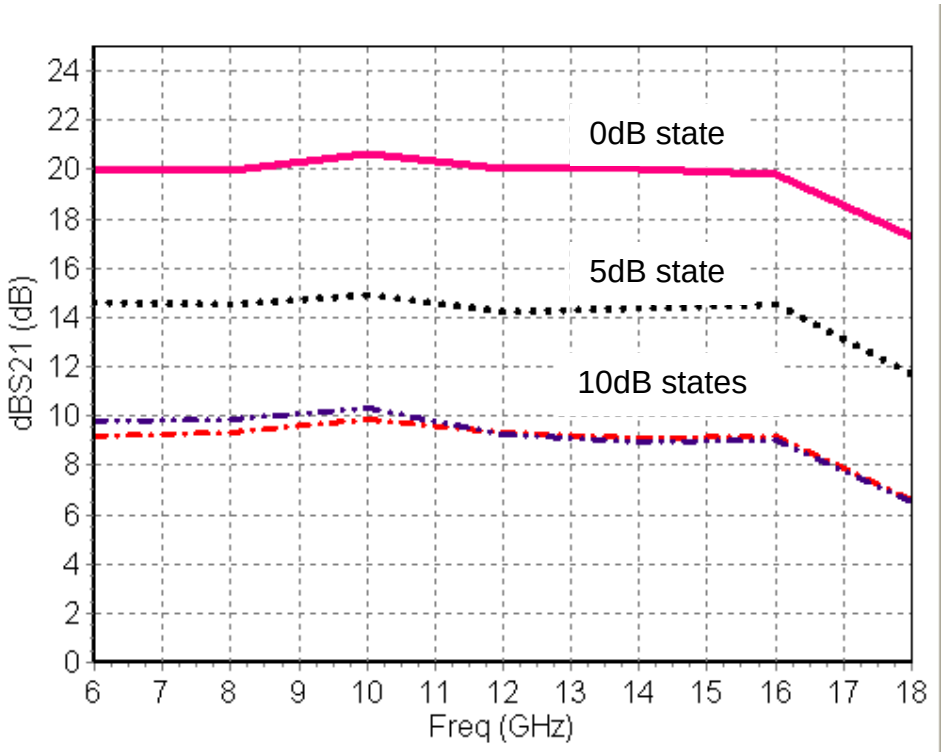
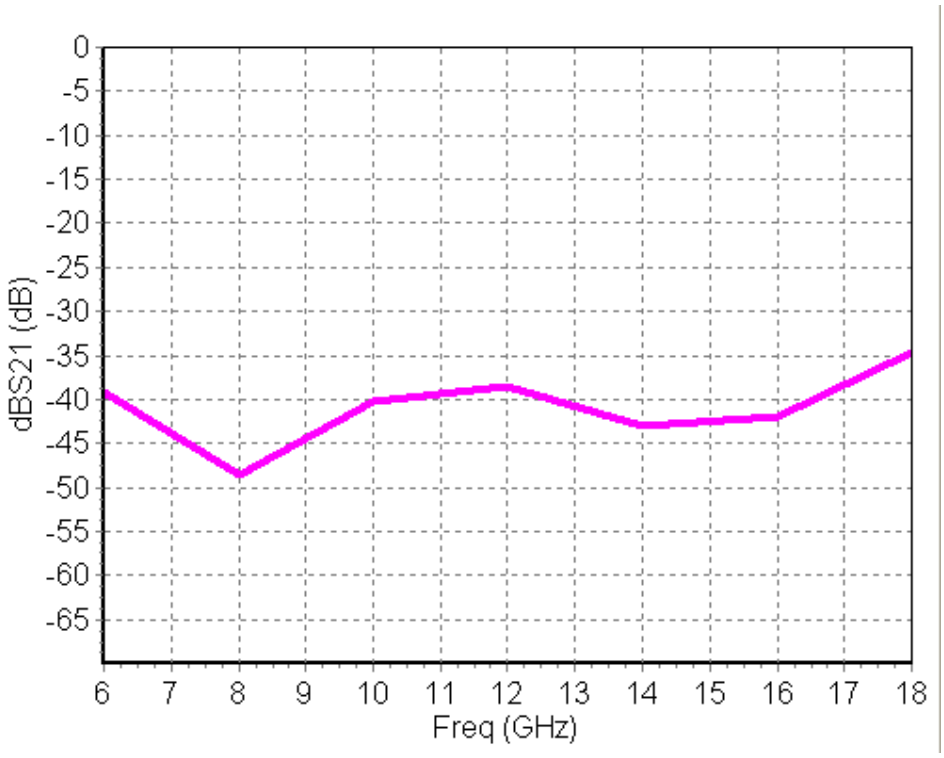
Typical on wafer Measurements @ 25°C

Bias conditions: Vd = 4.5V, Vg tuned for Id = 300mA



Linear Gain versus attenuator states



Linear Gain with SPST switch OFF

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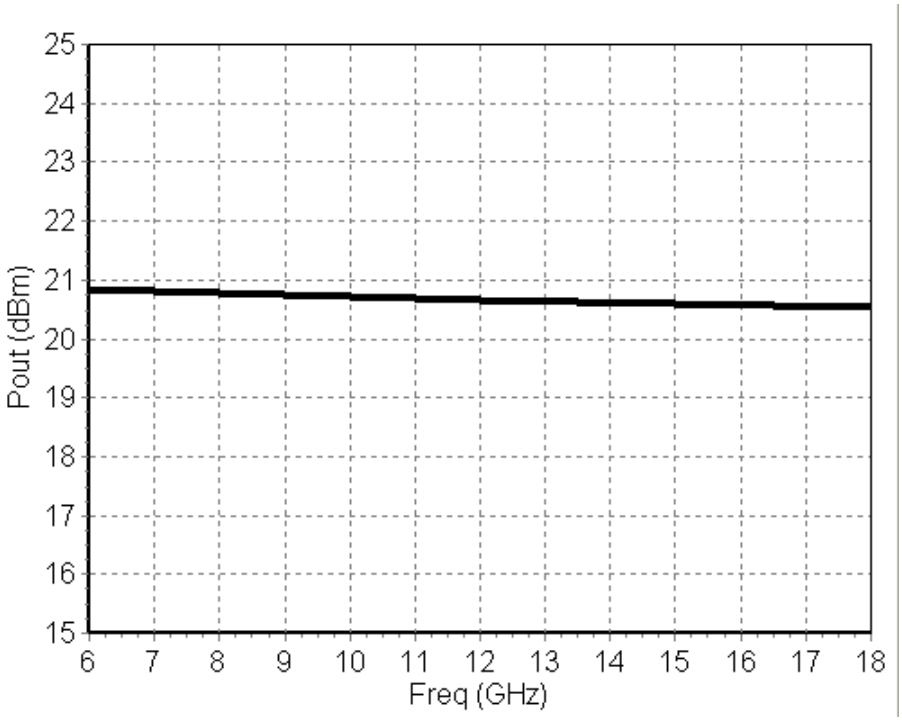
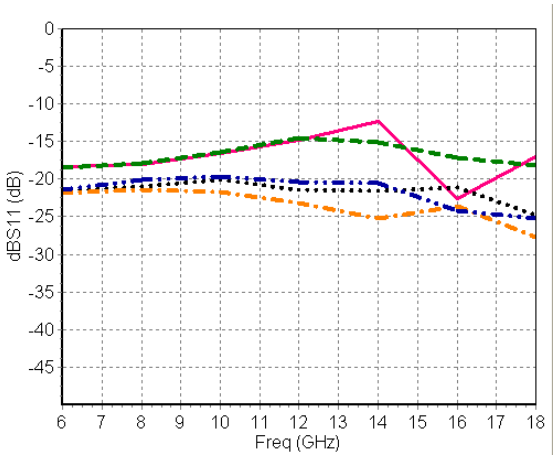
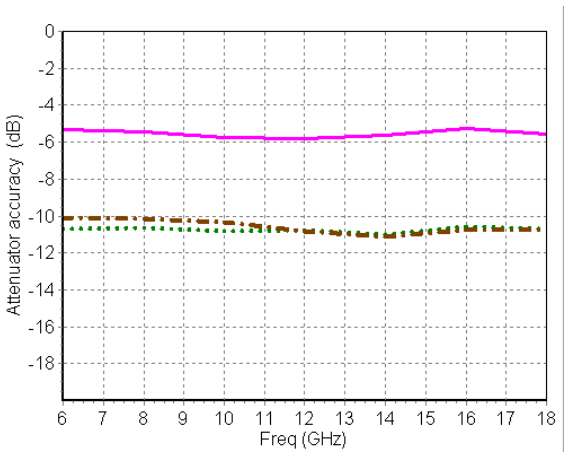


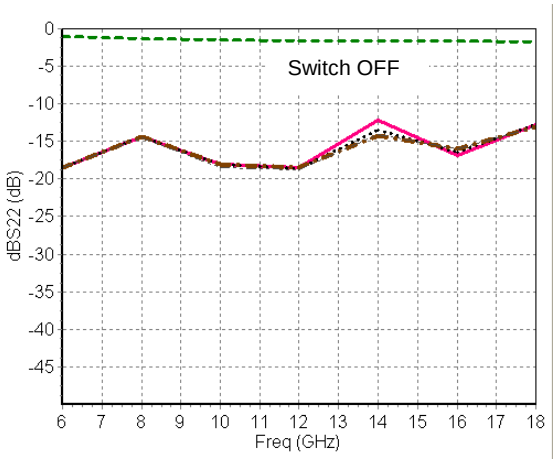
Saturated output power @ nominal state



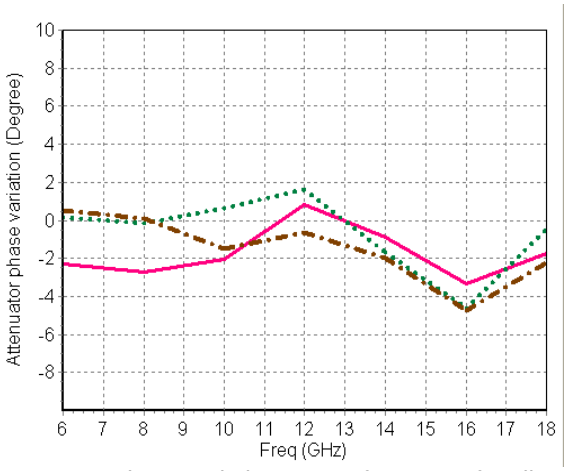
dB(S11) versus frequency for all state



Attenuator value versus frequency for all states



dB(S22) versus frequency for all states



Attenuator phase variation versus frequency for all states

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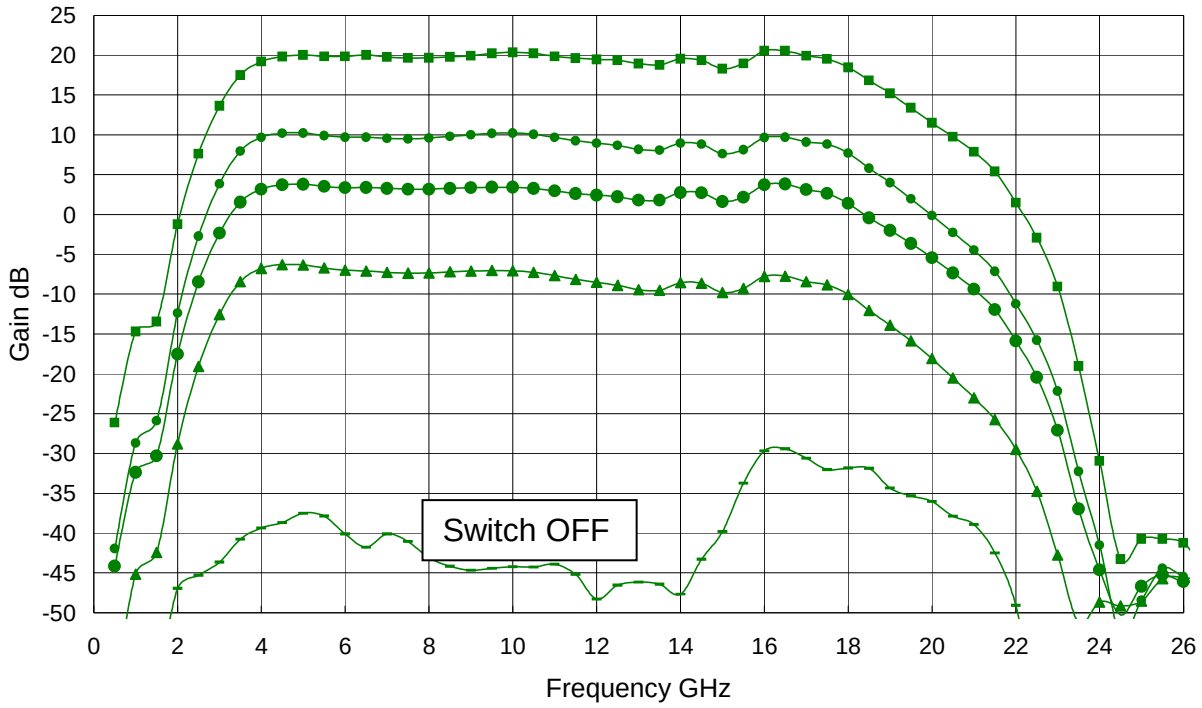
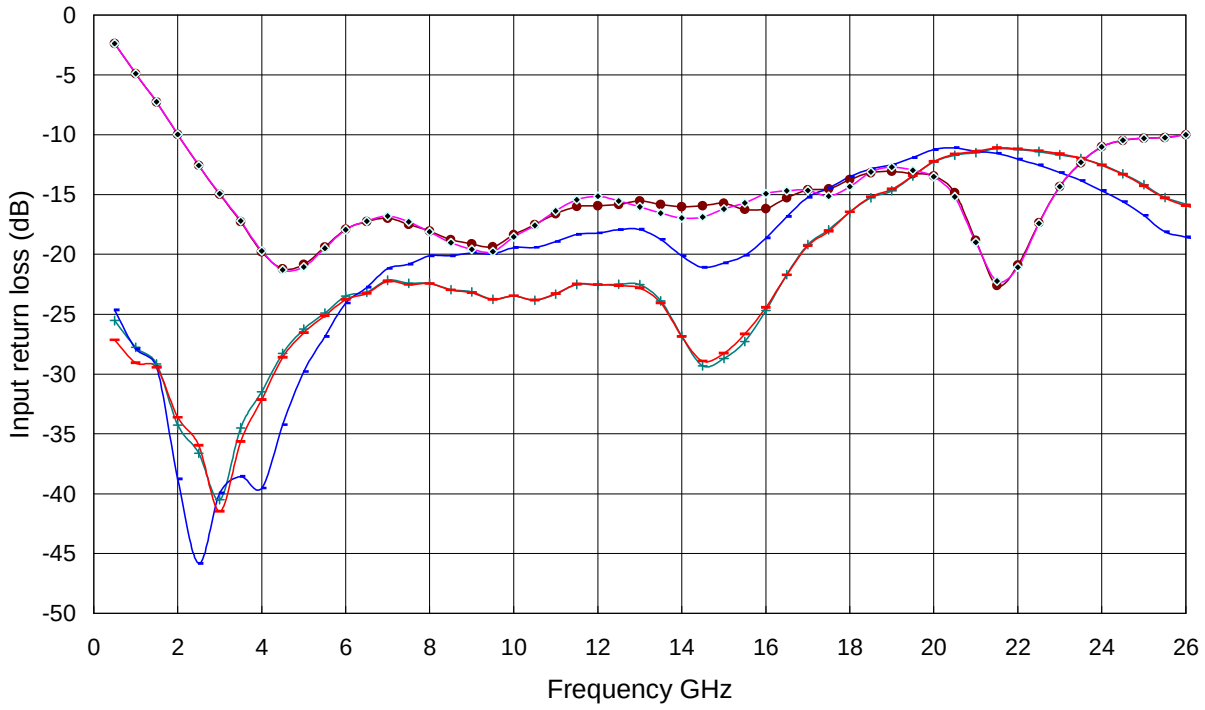
Typical test fixture Measurements @ 25°C

Bias conditions: Vd = 4.5V, Vg tuned for Id = 300mA

Linear Gain versus attenuation states



Input Return Loss versus attenuation states



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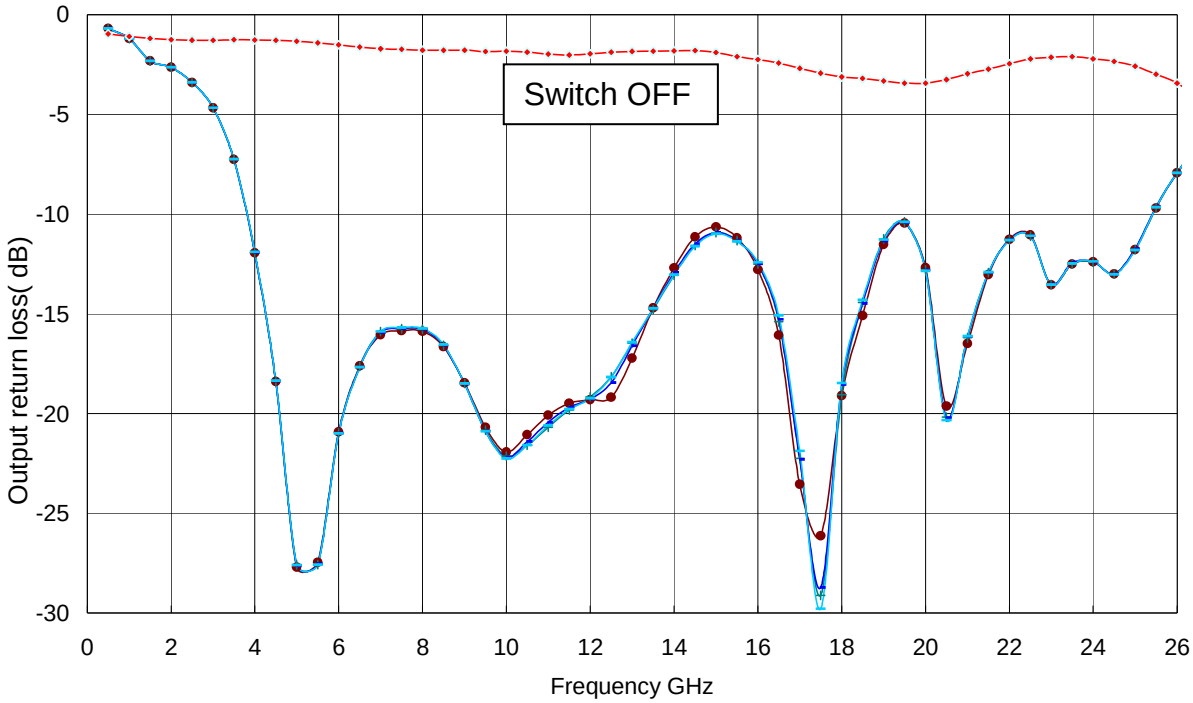
Output Return Loss versus attenuation states



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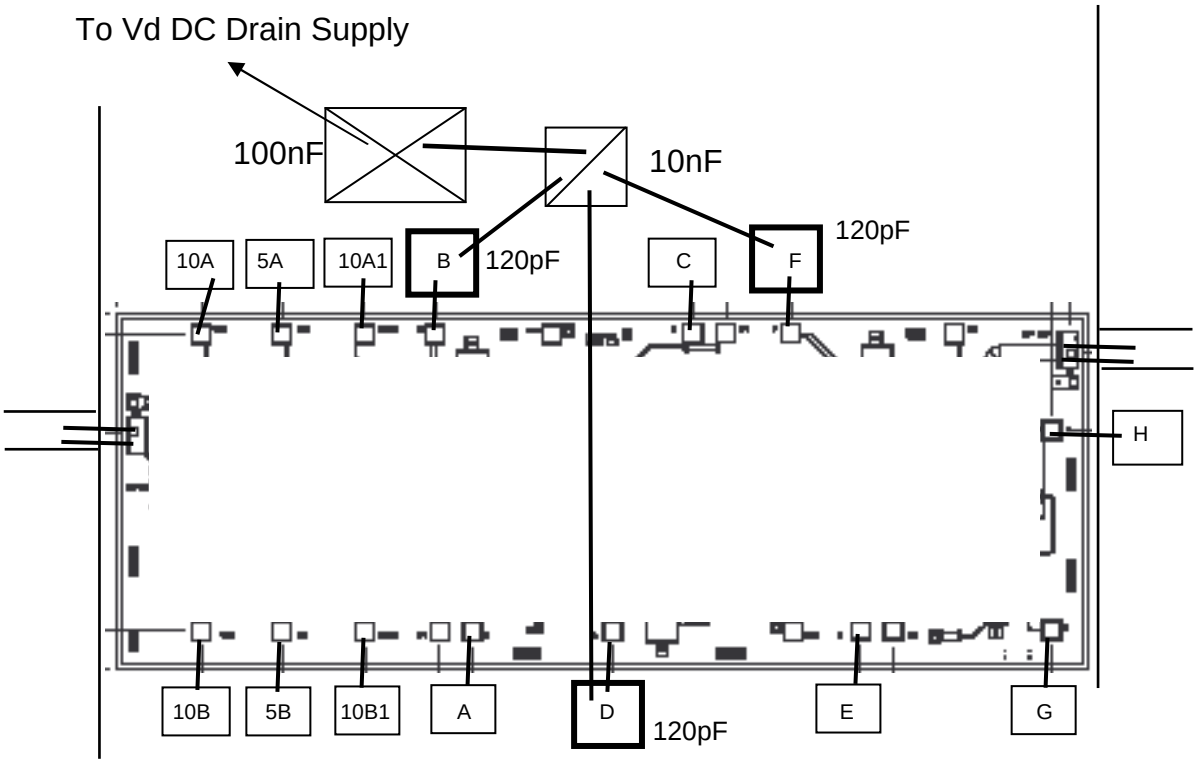
Chip Assembly and Mechanical Data



Note: Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be prefered.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
10A, 10B	Vc	*Not required*	First 10dB pad control
5A, 5B	Vc	*Not required*	5dB pad control
10A1, 10B1	Vc	*Not required*	Second 10dB pad control
B	Vd	120pF / 10nF	Drain Supply
D	Vd	120pF / 10nF	Drain Supply
F	Vd	120pF / 10nF	Drain Supply
A	Vg	*Not required*	Gate Supply
C	Vg	*Not required*	Gate Supply
E	Vg	*Not required*	Gate Supply
H	Vc	*Not required*	Switch control
G	Vc	*Not required*	Switch control

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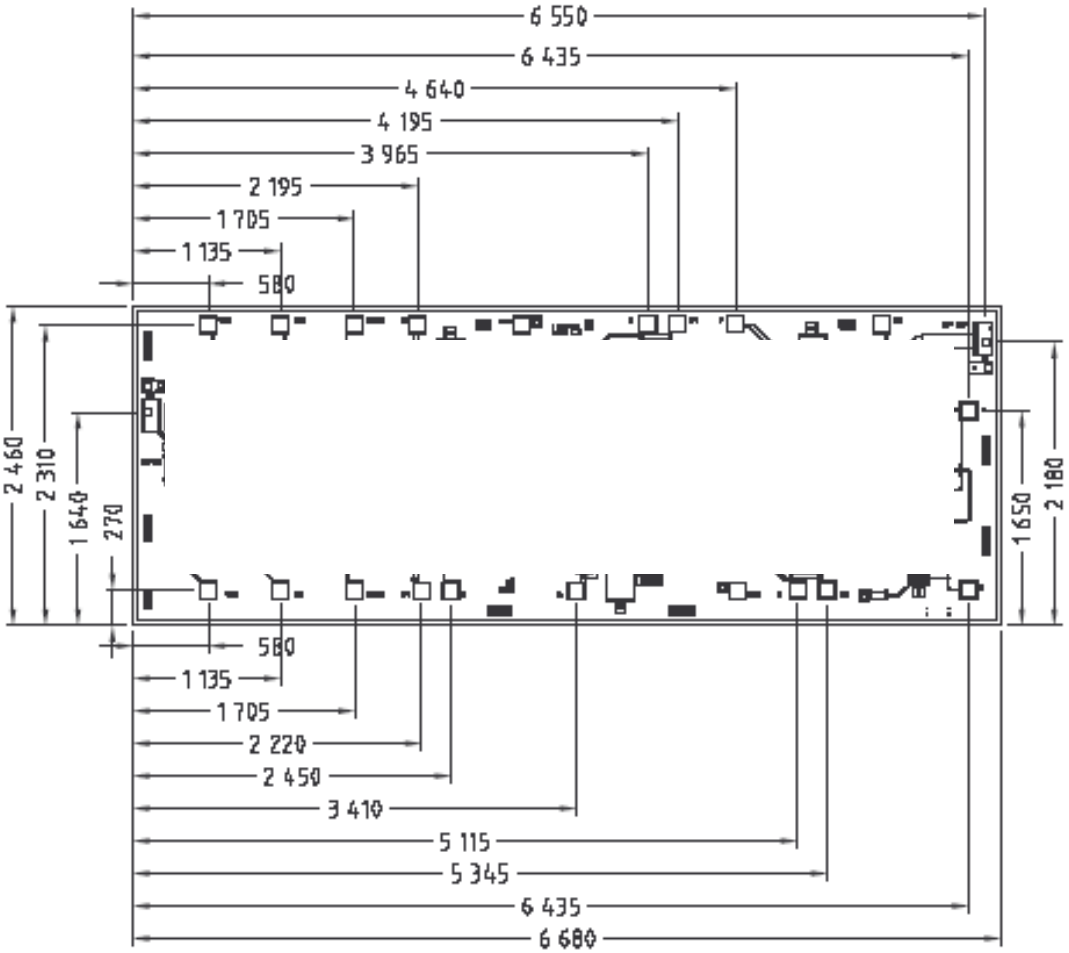
Bonding pad positions



(Chip thickness: 100µm)

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Ordering Information

Chip form : CHA3513-99F/00

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