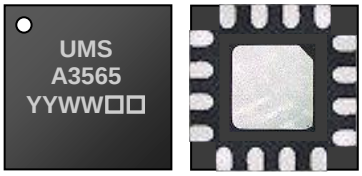
CHA3565-QAG

5-21GHz Driver Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

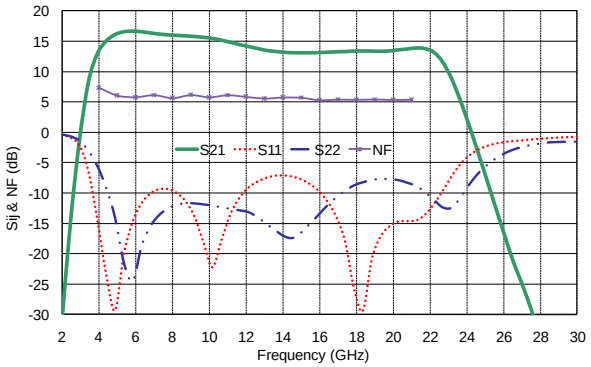
The CHA3565-QAG is a two-stage general purpose monolithic medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a power pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 5-21GHz
- 20.5dBm saturated output power
- 15dB gain
- DC bias: Vd=5Volt @ Id=120mA
- 16L-QFN3x3
- MSL1

Gain, return losses & NF (dB)



Main Characteristics

Tamb.= +25°C, Vd = +5.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5		21	GHz
Gain	Linear Gain	12.5	15		dB
Pout-1dB	Output Power @1dB gain compression	17.5	19.5		dBm
Psat	Saturated Output Power	19	20.5		dBm
Id	Drain current		120		mA

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Electrical Characteristics

Tamb.= +25°C, Vd = +5.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5		21	GHz
Gain	Linear Gain	12.5	15		dB
Pout-1dB	Output Power @1dB gain compression	17.5	19.5		dBm
Psat	Saturated Output Power	19	20.5		dBm
C/I3	C/I3 @ Pin/tone = -8dBm , Vd = 5V 5.0 to 7.5GHz 7.5 to 16.5GHz 16.5 to 20GHz		 40 34 33		 dBc dBc dBc
dBS11	Input Return Loss		-8	-6	dB
dBS22	Output Return Loss		-10	-8	dB
NF	Noise Figure		6		dB
Vd	Drain supply voltage		5		V
Id	Drain current		120		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6.0	V
Id	Drain bias current	175	mA
Vg	Gate bias voltage	-2 to +0.4	V
Ig	Gate bias current	+0.7	mA
Vgd	Maximum negative gate drain Voltage (Vd-Vg/2) (an array of resistor divides gate voltage by 2)	8	V
Pin	Maximum continuous input power	+10	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vd	13	Drain voltage	+5.0	V
Vg	5	Gate voltage	-1 to +0.4	V

Gate voltage is tuned to obtain 120mA drain current.
Vg can be either negative or positive supply bias.

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

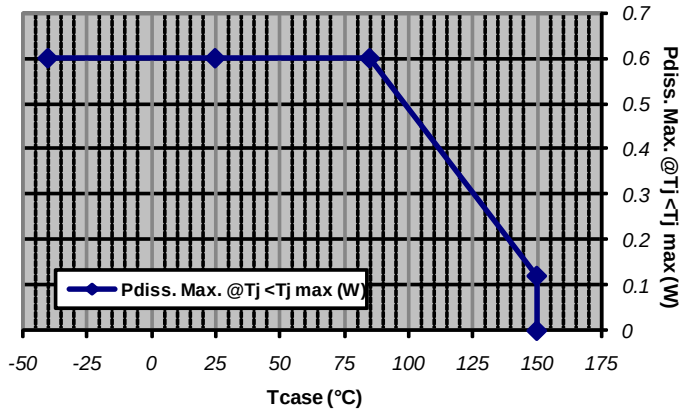
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

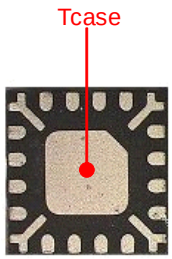
DEVICE THERMAL SPECIFICATION : CHA3565-QAG		
Recommended max. junction temperature (Tj max)	:	166 °C
Junction temperature absolute maximum rating	:	175 °C
Max. continuous dissipated power (Pdiss. Max.)	:	0.6 W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	7 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<135 °C/W
Minimum Tcase operating temperature(3)	:	-40 °C
Maximum Tcase operating temperature(3)	:	85 °C
Minimum storage temperature	:	-55 °C
Maximum storage temperature	:	150 °C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temperature reference point (Tcase) on package's bottom side

6.4

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Typical Package Sij parameters

Tamb.= +25°C, Vd = +5V, Id = 120mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
2	-0.4	-86	-31.3	-60	-58.4	98	-0.4	-71
3	-2.2	-149	-1.2	-121	-49.4	56	-1.4	-114
4	-14.3	136	12.9	99	-43.4	41	-5.5	-164
5	-29.4	45	16.1	-6	-38.0	-26	-14.0	164
6	-14.7	-48	16.6	-100	-37.4	-94	-24.5	-141
7	-10.1	-97	16.3	-170	-37.7	-144	-15.5	-131
8	-9.3	-142	16.0	129	-37.9	171	-12.5	-158
9	-13.9	144	15.8	45	-38.1	102	-11.7	163
10	-22.2	32	15.4	-9	-38.7	56	-12.1	141
11	-13.6	-78	14.8	-62	-40.2	11	-12.6	121
12	-9.2	-126	14.1	-111	-41.7	-26	-13.1	96
13	-7.5	-165	13.5	-159	-43.7	-69	-15.0	61
14	-7.1	158	13.2	154	-44.9	-91	-17.0	13
15	-7.7	121	13.1	107	-46.0	-130	-16.5	-52
16	-9.6	83	13.1	58	-46.3	-170	-13.6	-103
17	-13.9	43	13.2	7	-45.6	149	-10.7	-138
18	-25.7	-163	13.3	-46	-44.1	106	-8.7	13
19	-20.9	-75	13.3	-102	-41.0	64	-7.8	-13
20	-15.5	-131	13.4	-159	-39.4	12	-7.7	-40
21	-14.6	145	13.7	136	-38.0	-40	-8.3	-68
22	-11.8	-49	13.2	16	-39.1	-136	-11.1	-139
23	-7.3	172	8.9	-78	-46.1	131	-12.4	135
24	-3.8	76	1.1	-160	-53.6	19	-8.6	67
25	-2.2	15	-7.8	134	-53.0	-153	-5.4	24
26	-1.6	-26	-16.9	80	-46.5	57	-3.5	-10
27	-1.3	-57	-25.1	29	-39.3	-9	-2.4	-40
28	-1.0	-82	-33.3	-23	-42.4	-61	-1.9	-69
29	-0.8	-104	-37.1	-67	-39.4	-73	-1.6	-96
30	-0.7	-123	-37.7	-103	-38.2	-103	-1.6	-123

Refer to the “definition of the Sij reference planes” section below.

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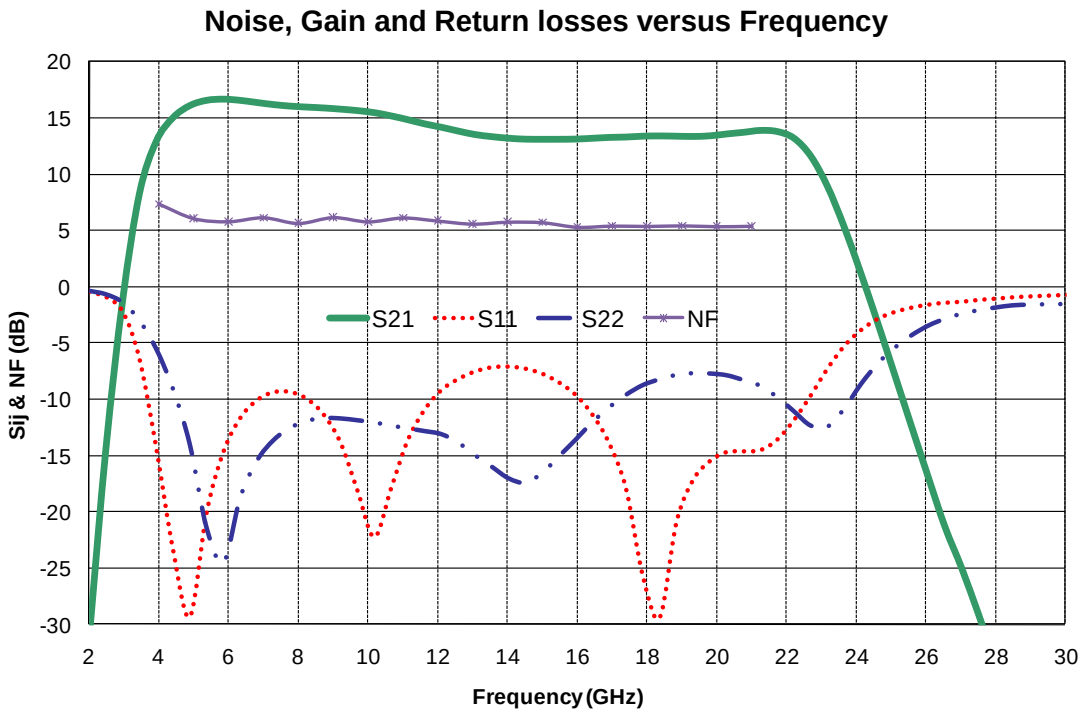
Typical Board Measurements

Tamb.= +25°C, Vd = +5V, Id = 120mA
Losses due to board are de-embedded. Measurements are given in the QFN's access plan.



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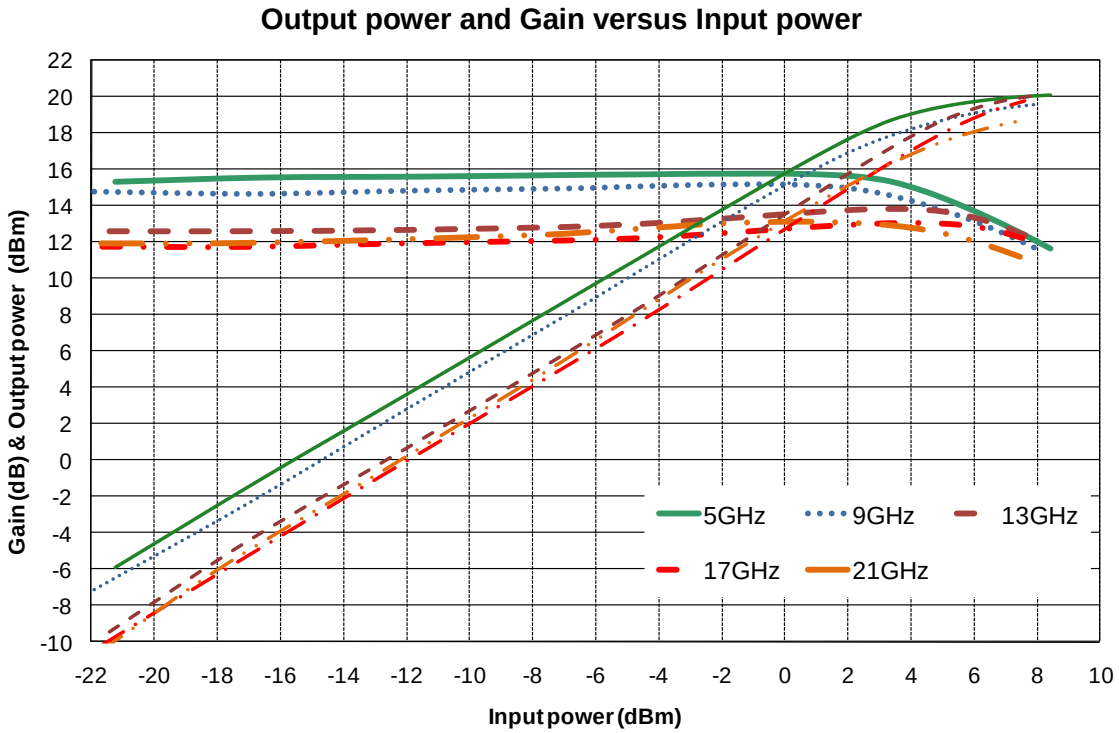
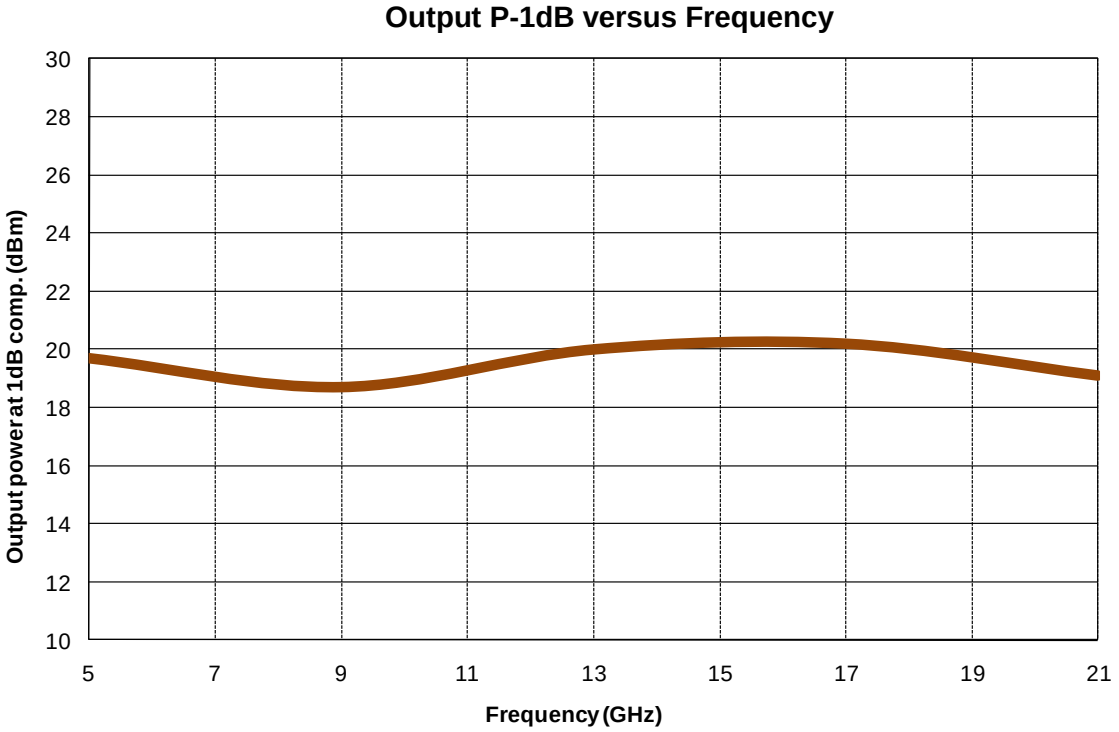
Typical Board Measurements

Tamb.= +25°C, Vd = +5V, Id = 120mA
Losses due to board are not de-embedded. Measurements are given in the connectors' access plan.





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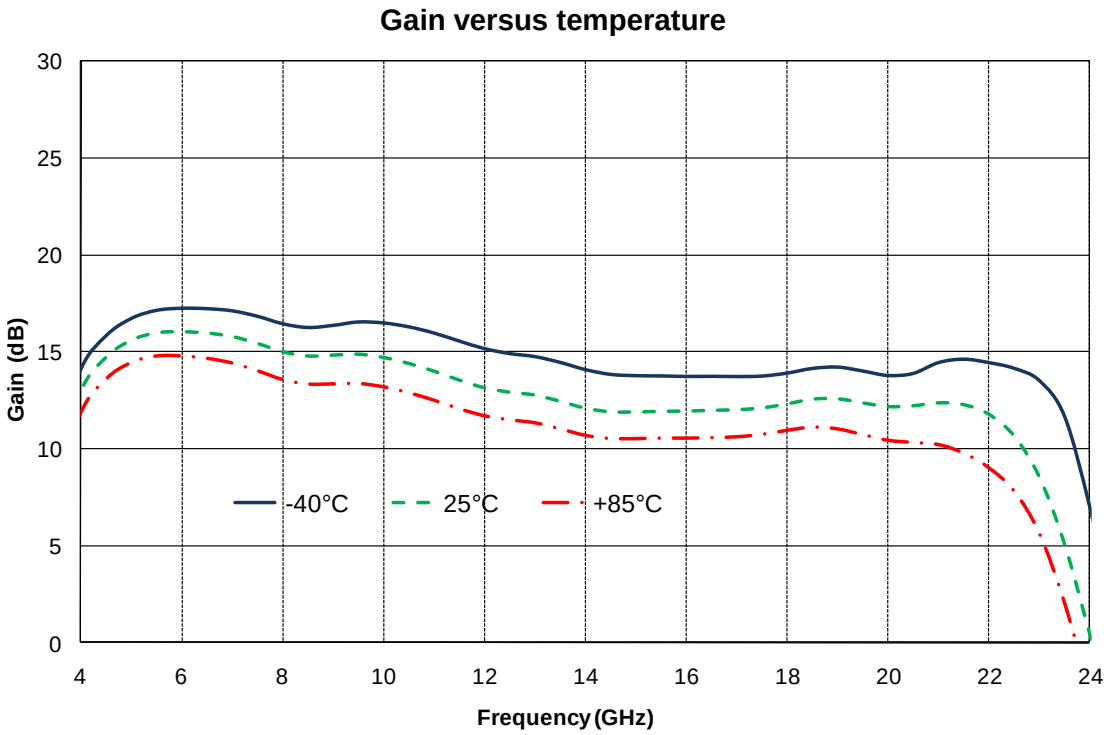
Typical Board Measurements

Tamb.= +25°C, Vd = +5V, Id = 120mA
Losses due to board are not de-embedded. Measurements are given in the connectors' access plan.



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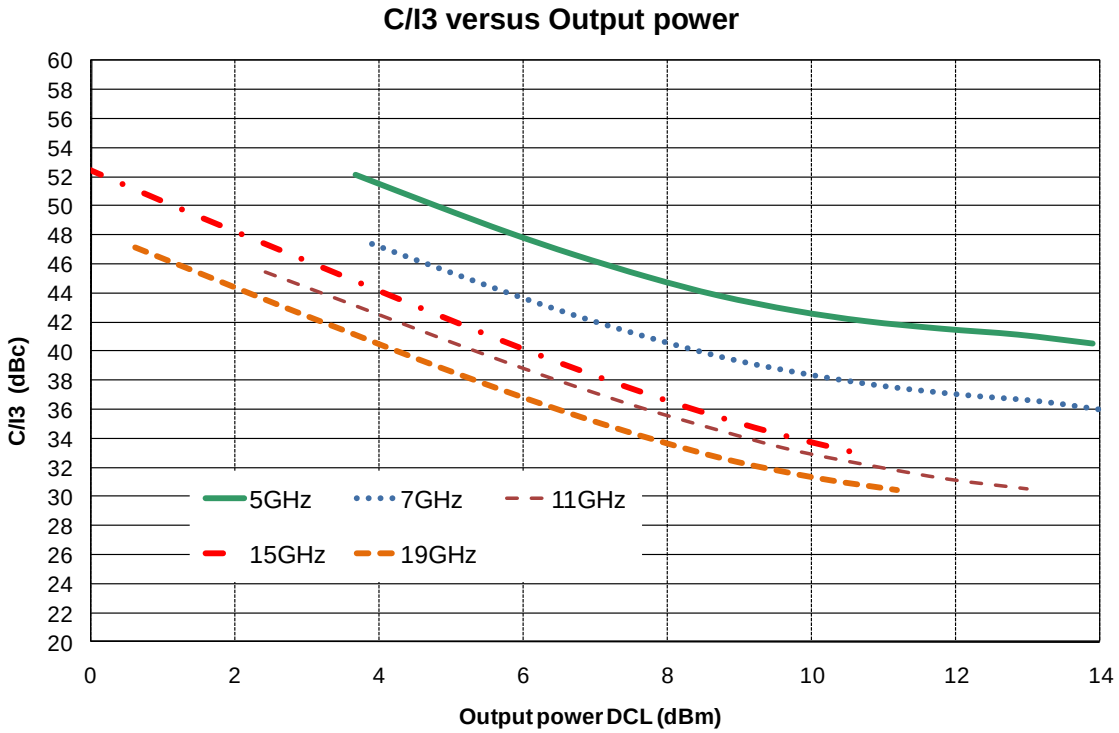
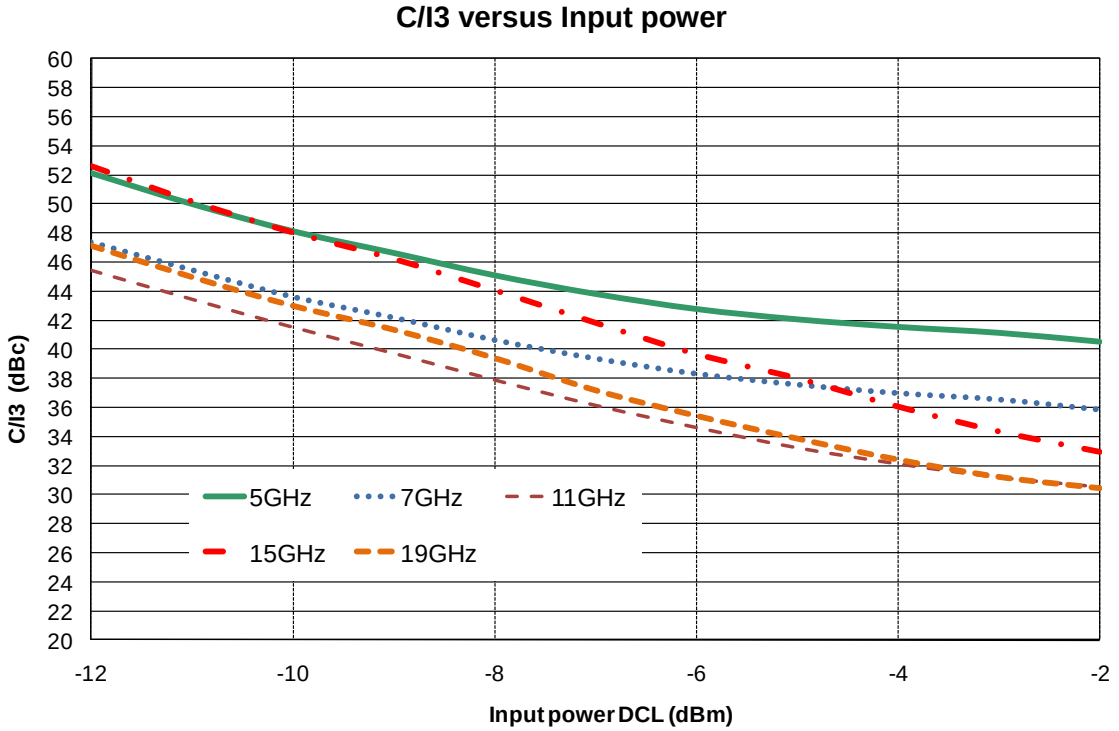
Typical Board Measurements

Tamb.= +25°C, Vd = +5V, Id = 120mA
Losses due to board are not de-embedded. Measurements are given in the connectors' access plan.





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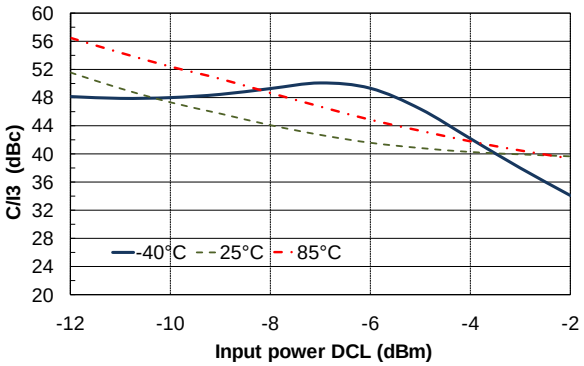
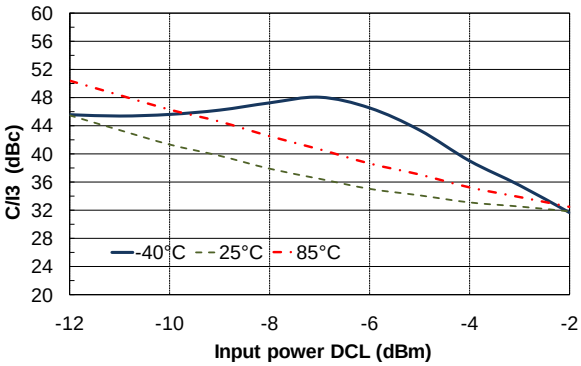
Typical Board Measurements

Tamb.= +25°C, Vd = +5V, Id = 120mA
Losses due to board are not de-embedded. Measurements are given in the connectors' access plan.

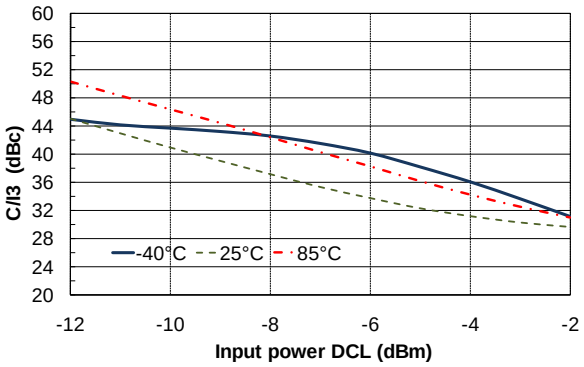
C/I3 versus input power and Temperature at 5GHz



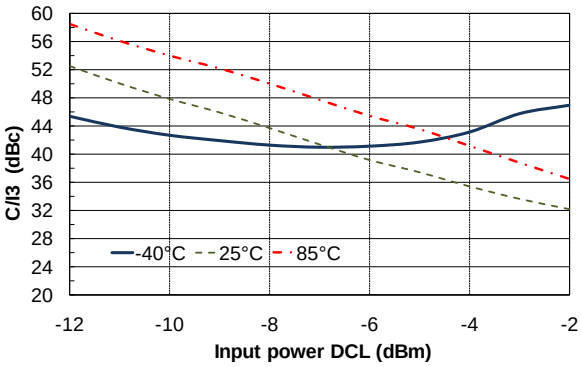
C/I3 versus input power and Temperature at 9GHz



C/I3 versus input power and Temperature at 11GHz



C/I3 versus input power and Temperature at 15GHz



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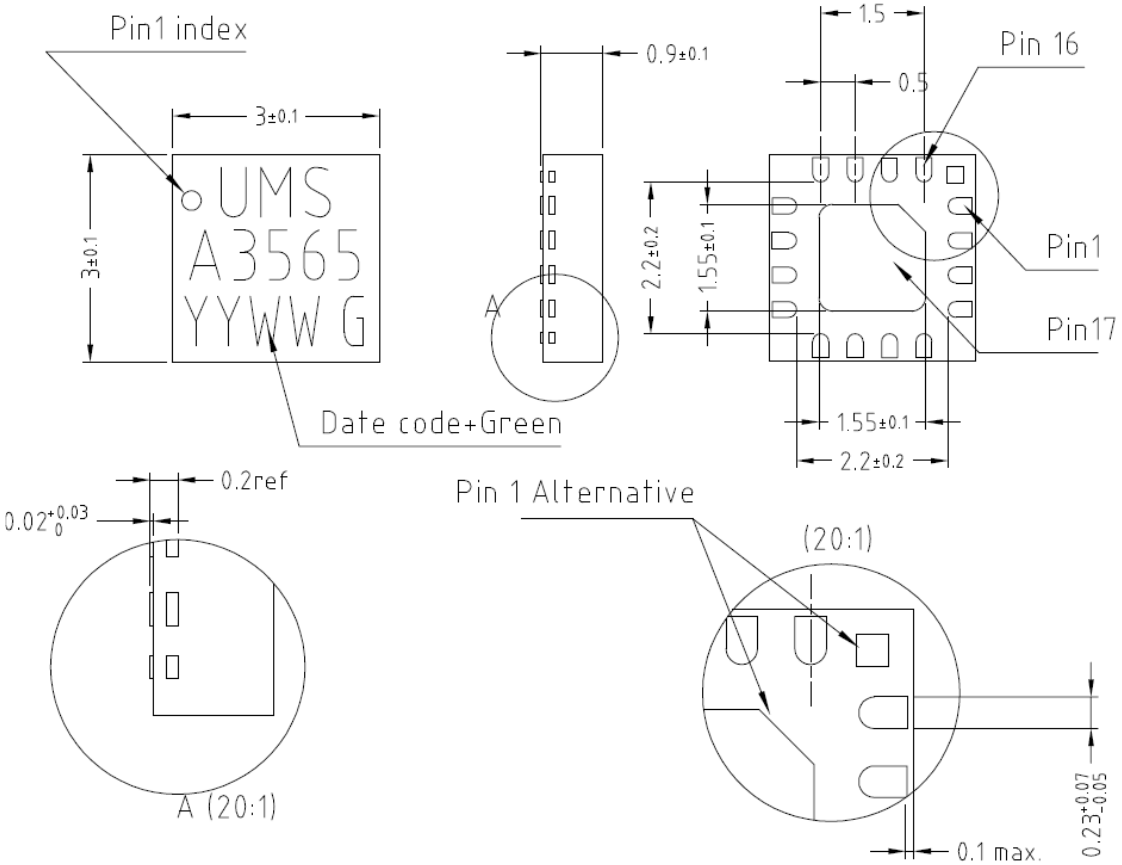
Package outline (1)



Matt tin, Lead Free (Green)		1- Gnd(2)	9- Nc
Units : mm		2- RF in	10- Nc
From the standard : JEDEC MO-220 (VGGD)		3- Gnd(2)	11- RF out
		4- Nc	12- Gnd(2)
17- GND		5- VG	13- VD
		6- Nc	14- Nc
		7- Nc	15- Nc
		8- Nc	16- Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (https://www.ums-rf.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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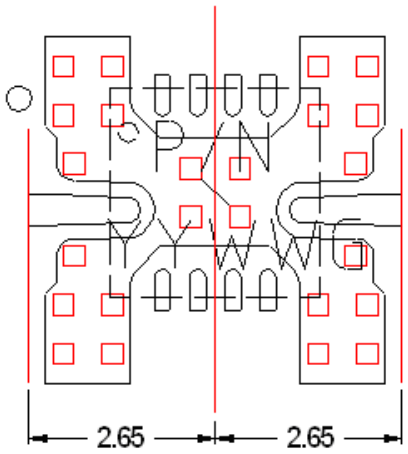
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



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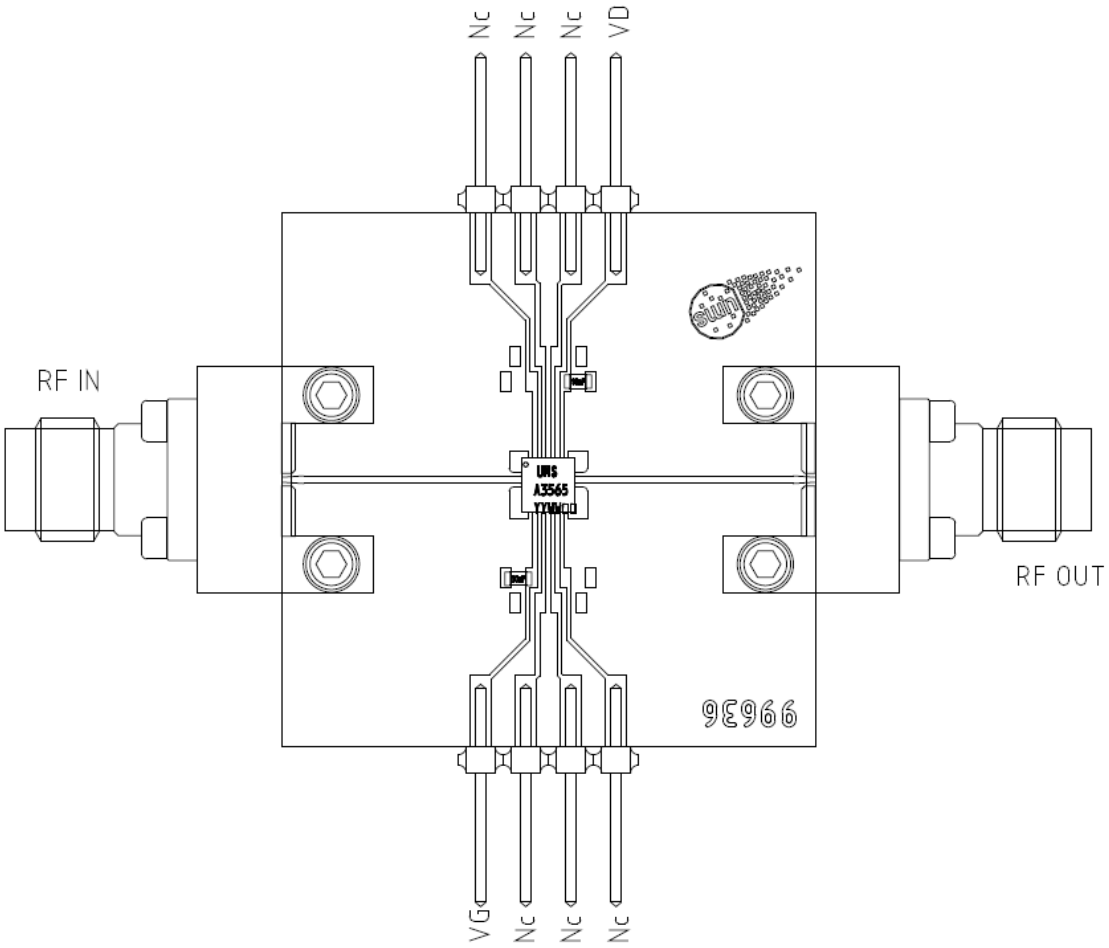
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.comums for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 3x3 RoHS compliant package:	CHA3565-QAG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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