CHA3801-QDG

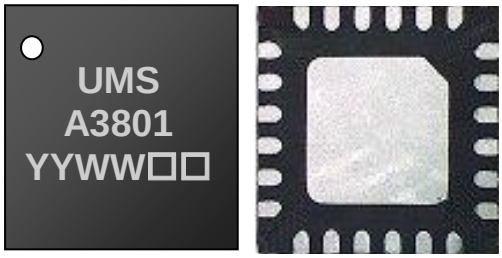
RoHS COMPLIANT

L-Band Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

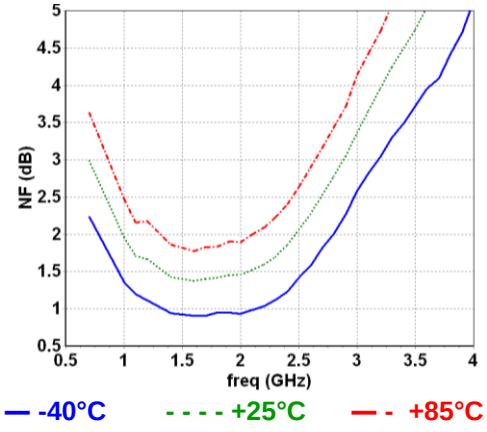
Description

The CHA3801-QDG is an L-Band LNA monolithic circuit including an active bias network. Furthermore a protection network is included in order to allow high input power survivability.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.



Main Features

- L-Band performances: 1-2GHz
- 1.5dB Noise Figure
- 28dB Linear Gain
- 17dBm Saturated Power
- 27dBm Output Third Order Intercept
- DC bias: Vd = 5Volt @ 70mA
- 24L-QFN4x4
- MSL3



Typical Noise Figure versus Temperature

Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1		2	GHz
Gain	Linear Gain		28		dB
NF	Noise Figure		1.5		dB
Pout	Output Power @1dB comp.		15		dBm

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Operating Modes

Mode	Description	Pin #7 Pin #10	Pin #8 Pin #11	Pin #9 Pin #12	Pin #13 Pin #14
1a	Nominal bias current	-5V	n.c.*	n.c. *	+5V
1b	High bias current	n.c.*	-5V	n.c. *	+5V
1c	Low bias current	-5V	-5V	n.c. *	+5V

* Not connected

Input protection state	Pin #6			
enabled	GND			
disabled	-5V			

Electrical Characteristics

Tamb.= +25°C, Vd = +5V under working mode 1a and input protection disabled

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1		2	GHz
Gain	Gain		28		dB
-	Gain flatness		0.5		dBp-p
Rlin	Input Return Loss		-15		dB
Rlout	Output Return Loss		-15		dB
NF	Noise Figure		1.5		dB
|S12|	Reverse Isolation		40		dB
OIP3	Output Third order Intercept Point		27		dBm
OP1dB	Output 1 dB Compression Point		15		dBm
Id_1a	Total drain Current (mode 1a)		72		mA
Id_1b	Total drain Current (mode 1b)		92		mA
Id_1c	Total drain Current (mode 1c)		45		mA
Vd	Drain Voltage		5		V
Vg	Gate Voltage		-5		V

These values are representative of measurements on board

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage (Vg=-5V)	6.5	V
Vctrl	Control voltage	-6 to 0	V
Vg	Gate bias voltage (Vd=+5V)	-6 to 0	V
Pin	Protection switch enabled	+17	dBm
Pin	Protection switch disabled	+6	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pin Nº	Parameter	Values	Unit
Vd	13, 14	Drain voltage	+5	V
Vg	7, 10	See paragraph Operating Modes	–5	V

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

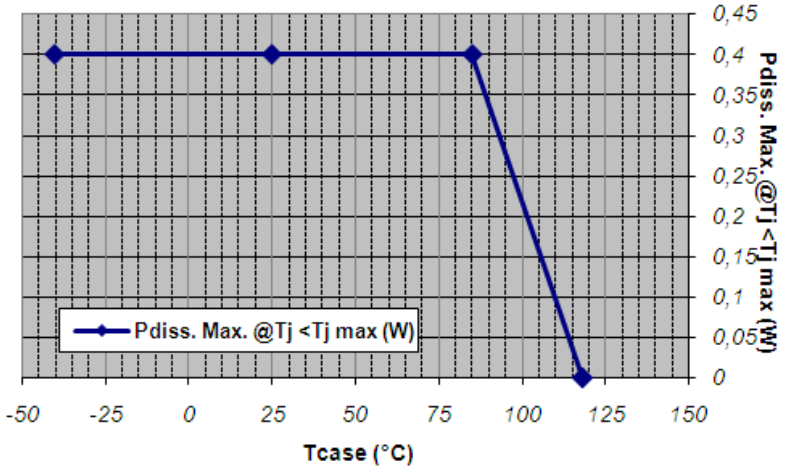
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

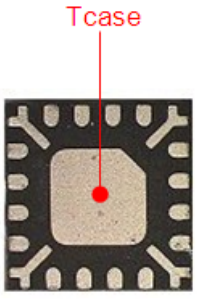
DEVICE THERMAL SPECIFICATION : CHA3801				
Recommended max. junction temperature (Tj max)			:	118 °C
Junction temperature absolute maximum rating			:	175 °C
Max. continuous dissipated power (Pdiss. Max.)			:	0,4 W
=> Pdiss. Max. derating above Tcase(1)=	85	°C	:	12 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)			:	<82 °C/W
Minimum Tcase operating temperature(3)			:	-40 °C
Maximum Tcase operating temperature(3)			:	85 °C
Minimum storage temperature			:	-55 °C
Maximum storage temperature			:	150 °C

(1) Derating at junction temperature constant = Tj max.

*(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temeprature reference point (Tcase) on package's bottom side

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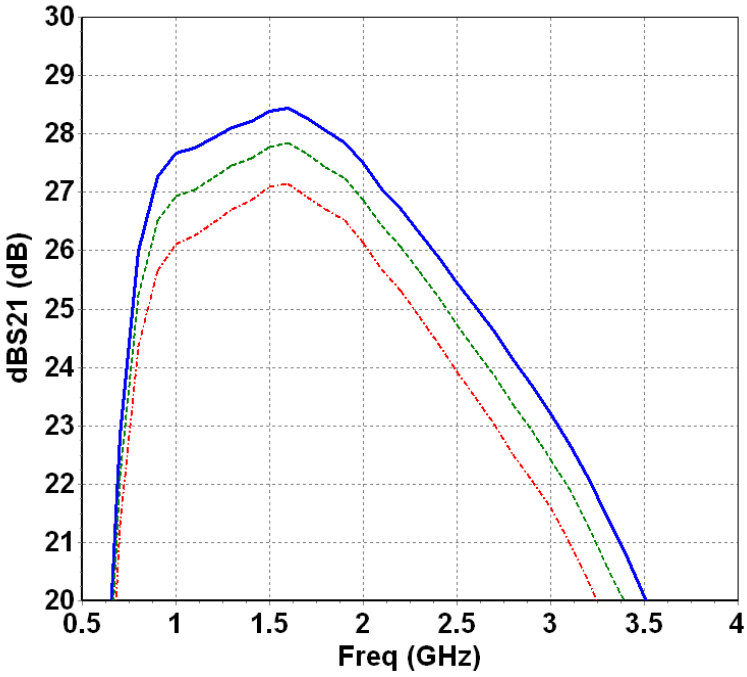
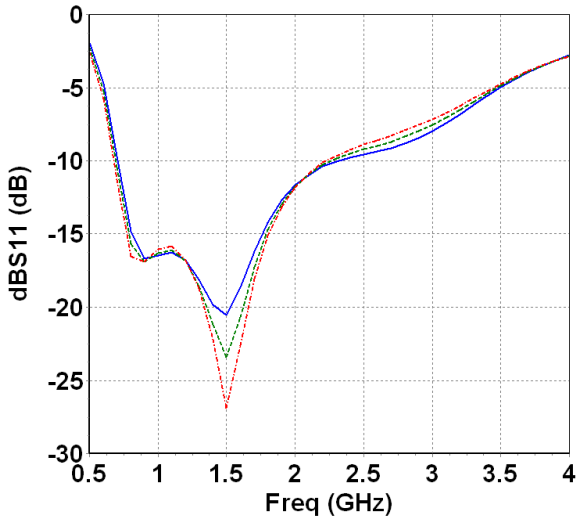
Typical Board Measurements

Temperature -40°C, +25°C, +85°C
Vd = +5V, working mode 1a with input protection disabled

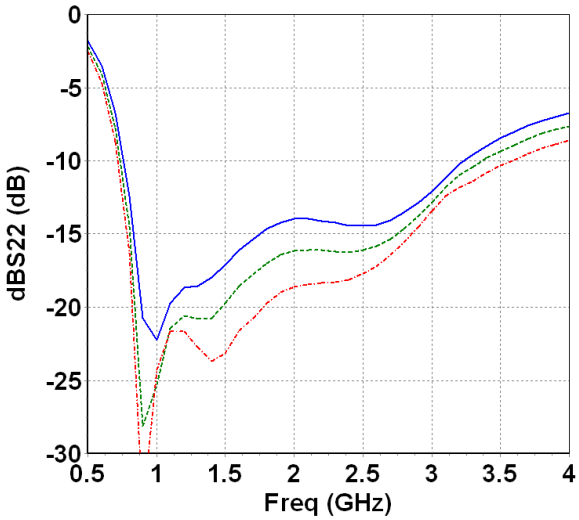
Linear Gain versus Frequency



Input Return Loss versus Frequency



Output Return Loss versus Frequency



— -40°C - - - - +25°C — - +85°C

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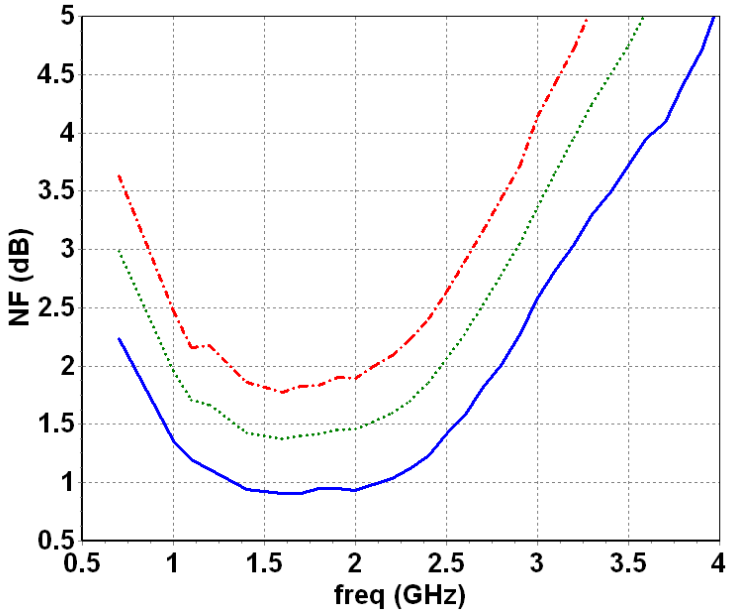
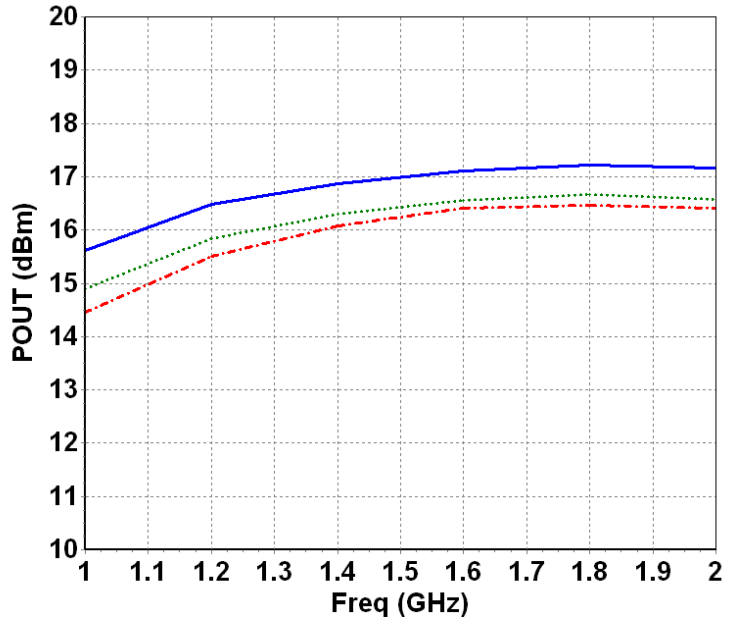
Typical Board Measurements

Temperature -40°C, +25°C, +85°C
Vd = +5V, working mode 1a with input protection disabled

Noise Figure versus Frequency



Output power @ 1dB comp. versus Frequency



— -40°C - - - - +25°C — - +85°C

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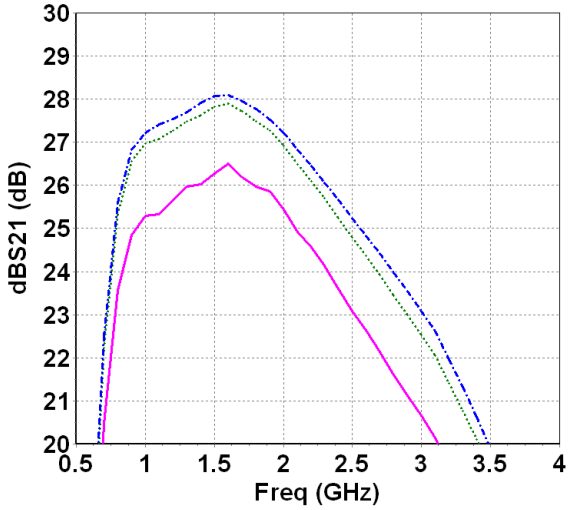
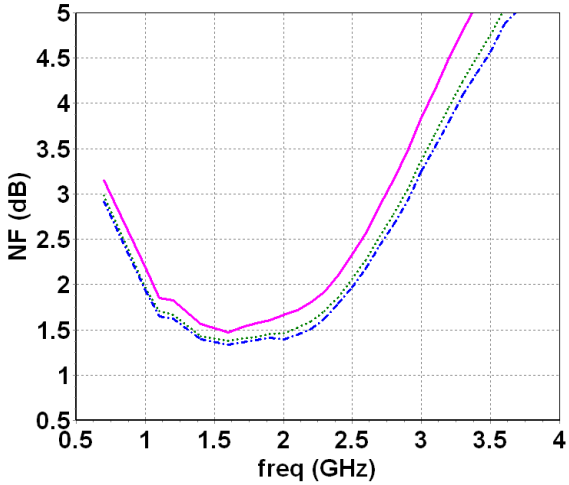
Typical Board Measurements

Tamb.= +25°C, Vd = +5V, working with input protection disabled

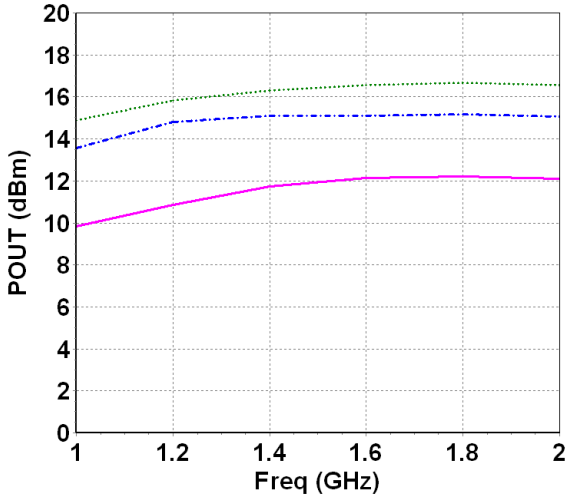
Linear gain



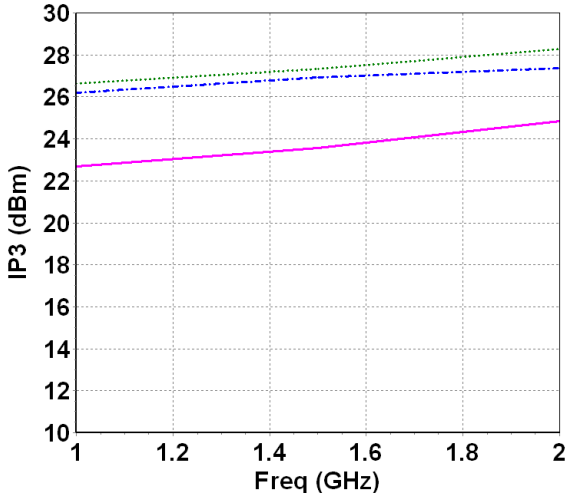
Noise Figure versus Frequency



Output power @ 1dB comp. versus Frequency



Output IP3 versus Frequency



— Mode 1c - - - - Mode 1a — - Mode 1b

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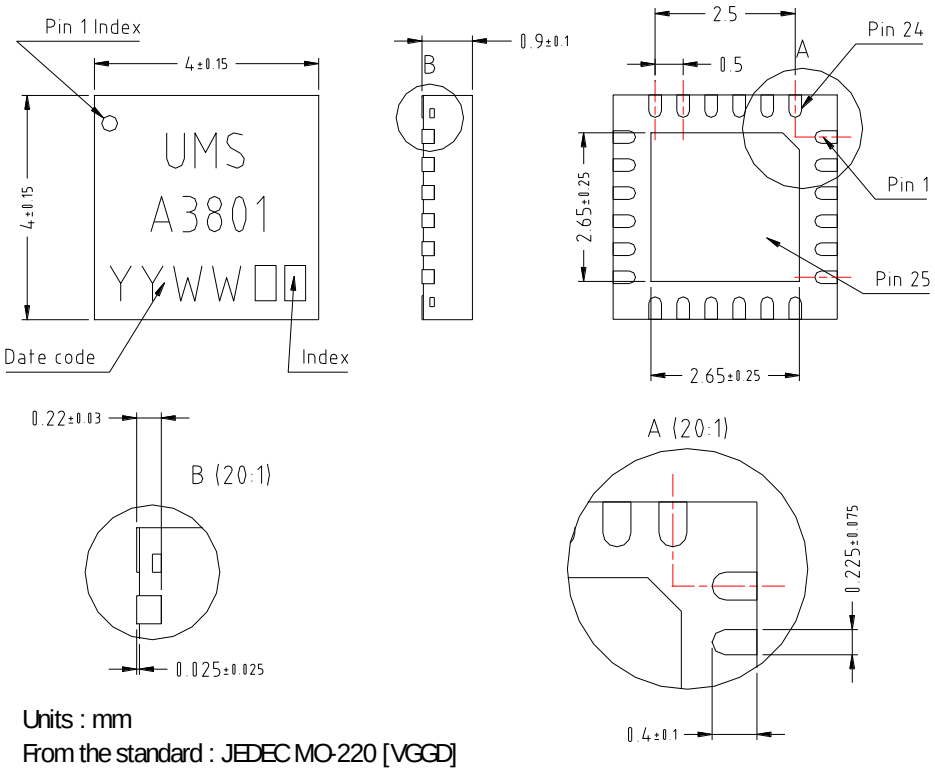
Package outline (1)



Units : mm
From the standard : JEDEC MO-220 [VGGD]

Matt tin, Lead Free (Green)	1- Nc	9- VG1_DISABLE	17- Nc
Units : mm	2- Nc	10- VG2	18- Nc
From the standard : JEDEC MO-220 (VGGD)	3- RF_IN	11- VG2_BIS	19- Nc
	4- Gnd(2)	12- VG2_DISABLE	20- Nc
25- GND	5- Gnd(2)	13- VDD1	21- Nc
	6- V_CTRL	14- VDD2	22- Nc
	7- VG1	15- Gnd(2)	23- Nc
	8- VG1_BIS	16- RF_OUT	24- Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (https://www.ums-rf.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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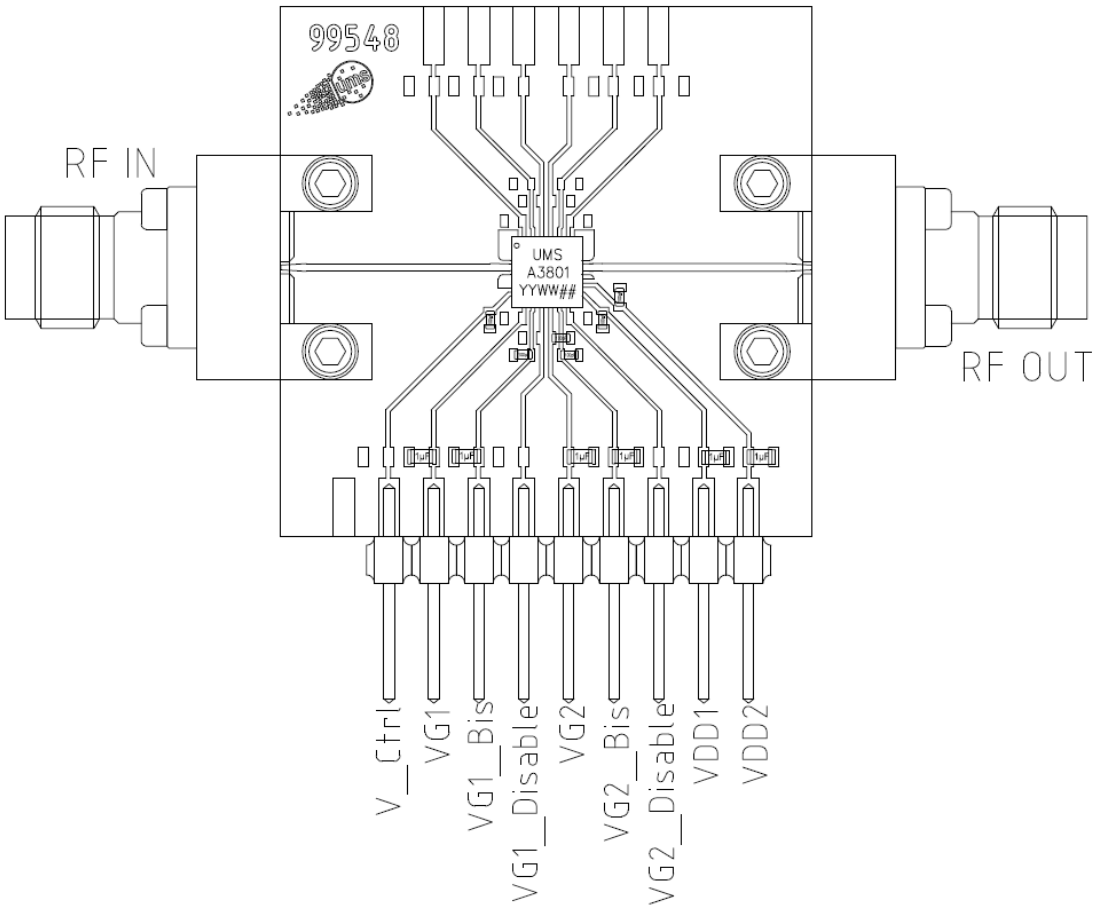
Evaluation Board

Based on typically Ro4003 / 8 mils or equivalent.
Decoupling capacitors of 100pF and 1µF are recommended for all DC access.



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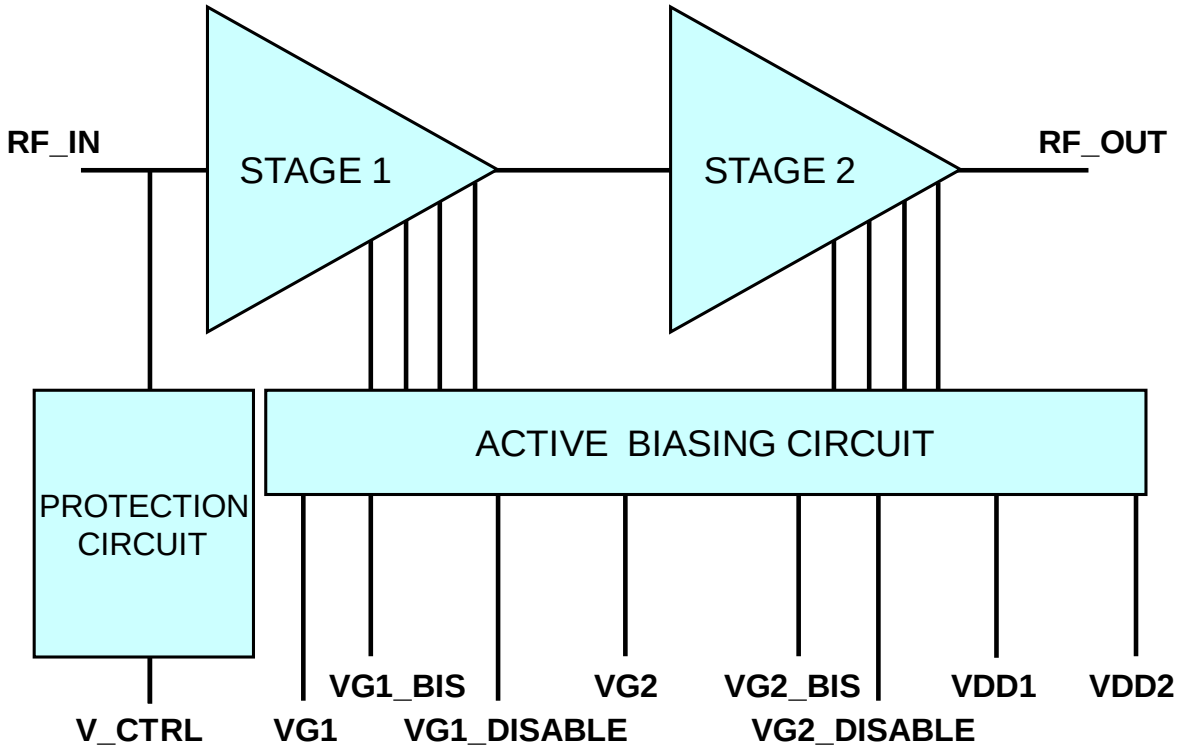
Block Diagram

Block diagram of the LNA



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Note

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at https://www.ums-rf.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 RoHS compliant package:	CHA3801-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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