

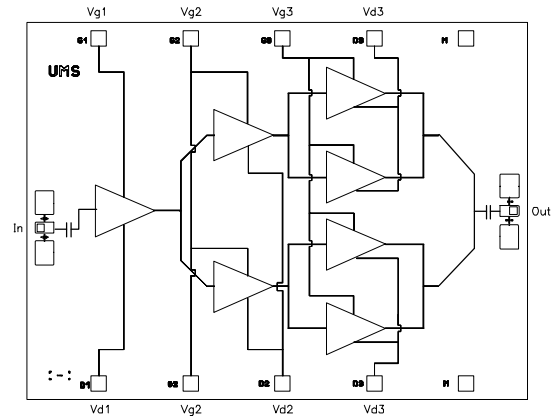
## 22-26GHz High Power Amplifier

### GaAs Monolithic Microwave IC

#### Description

The CHA5093 is a high gain three-stage monolithic high power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

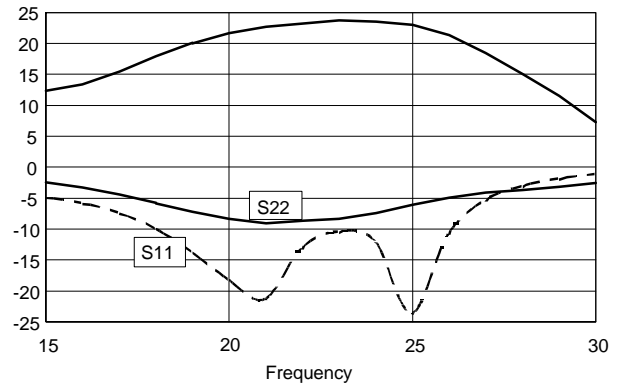
The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.



#### Main Features

- Performances : 22-26GHz
- 29dBm output power
- 20 dB ± 1.5dB gain
- DC power consumption, 600mA @ 6V
- Chip size : 3.27 x 2.47 x 0.10 mm

Gain & RLoss (dB)



Typical on Wafer Measurements

#### Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	22		26	GHz
G	Small signal gain	18	20		dB
P1dB	Output power at 1dB gain compression	28	29		dBm
Id	Bias current		600	900	mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

## Electrical Characteristics

Tamb = +25°C, Vd = 6V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	22		26	GHz
G	Small signal gain (1)	18	20		dB
ΔG	Small signal gain flatness (1)		±1.5		dB
Is	Reverse isolation (1)		50		dB
P1dB	Pulsed output power at 1dB compression (1)	28	29		dBm
P03	Output power at 3dB gain compression		29.5		dBm
IP3	3 <sup>rd</sup> order intercept point (2)		40		dBm
PAE	Power added efficiency at 1dB comp.		19		%
VSWRin	Input VSWR			2.3:1	
VSWRout	Output VSWR			2.3:1	
Tj	Junction temperature for 80°C backside		170		°C
Id	Bias current		600	900	mA

(1) These values are representative for pulsed on-wafer measurements that are made without bonding wires at the RF ports.

(2) Value representative for CW on jig measurement.

## Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6	V
Id	Drain bias current	1200	mA
Vg	Gate bias voltage	-2.5 to +0.4	V
Vgd	Negative gate drain voltage (= Vg - Vd)	-8	V
Pin	Maximum peak input power overdrive (2)	+12	dBm
Ta	Operating temperature range	-40 to +80	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above any one of these parameters may cause permanent damage.

(2) Duration < 1s.

### Typical On Wafer Scattering Parameters

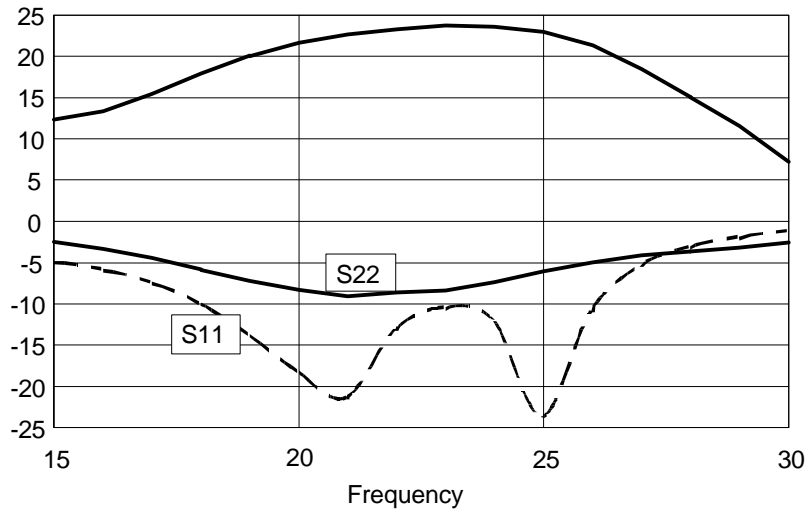
Bias Conditions : Vd = +2V, Vg = -0.1V

Freq GHz	S11 dB	S11 /°	S12 dB	S12 /°	S21 dB	S21 /°	S22 dB	S22 /°
1	-0,59	169,8	-83,89	-9,2	-51,47	60	-0,31	-10,4
2	-0,38	158,6	-94,7	-97,3	-66,17	-14,6	-0,04	-22,2
3	-0,57	146,5	-90,83	40,1	-62,89	156,2	-0,04	-33,3
4	-0,92	131,5	-87,53	-65,9	-55,62	-37,1	-0,07	-44,6
5	-1,81	112,8	-91,02	-172,1	-54,96	70,7	-0,08	-55,8
6	-3,56	88,7	-88,88	-109,5	-49,83	87,6	-0,09	-66,9
7	-6,86	56,1	-93,06	-18,3	-45,68	47	-0,1	-78,2
8	-11,49	2	-89,41	-123,6	-28,33	121,7	-0,12	-90
9	-11,08	-75,8	-77,69	-57,9	-13,56	56,8	-0,2	-102,3
10	-7,5	-122,7	-73,31	-105,8	-4,53	-7,7	-0,29	-114,9
11	-5,5	-150,3	-67,65	-103,5	2,35	-66,5	-0,45	-128,5
12	-4,65	-170,2	-64,52	-128,8	9,41	-125,1	-0,84	-143,5
13	-4,49	174,7	-60,09	-138,2	15,11	147,6	-1,9	-157
14	-4,54	161,9	-57,15	-165,4	13,29	74,3	-2,08	-168,6
15	-5,01	149	-54,69	165,9	12,35	33,4	-2,48	174,5
16	-5,95	137,3	-52,41	131,9	13,33	-1,5	-3,31	155,3
17	-7,54	125,2	-54,05	103,3	15,41	-38,2	-4,38	133,5
18	-10,08	116,3	-54,29	99,6	17,95	-81,4	-5,87	109,1
19	-13,87	114,1	-53,07	70	20,07	-128,3	-7,16	81
20	-18,32	120,1	-55,69	61,4	21,69	179,9	-8,31	49
21	-21,53	-166,1	-55,41	49,3	22,71	128,5	-9,09	15,1
22	-13,29	-152,4	-53,16	28,6	23,28	77,4	-8,63	-13,6
23	-10,62	-174,2	-56,67	-23,7	23,74	24,1	-8,36	-36,8
24	-12,11	161,8	-64,73	-101,8	23,55	-30,6	-7,39	-53
25	-23,82	-175,5	-61,49	109,9	22,98	-88,4	-6,07	-67,6
26	-11,02	-104,7	-55,53	89,3	21,32	-147	-4,94	-82,5
27	-5,56	-127,3	-53,1	73	18,44	157,6	-4,11	-97
28	-3,27	-144,5	-49,46	59,2	15,1	107,4	-3,64	-109,9
29	-2,09	-159,2	-49,07	21,2	11,56	59,1	-3,14	-121,3
30	-1,33	-170,7	-47,23	2,2	7,22	12,8	-2,61	-131,9
31	-0,78	178,1	-47,06	-20,4	2,57	-29,9	-2,29	-143,6
32	-0,62	168,3	-50,11	-56,1	-2,99	-69,1	-2,08	-154,5
33	-0,41	159,5	-55,89	-68,4	-9,66	-104	-1,96	-165,5
34	-0,4	151,3	-61,66	-95,4	-22,01	-110,4	-1,99	-175,4
35	-0,38	144	-66,3	-14,3	-14,55	-69,1	-1,86	175,9
36	-0,37	136,5	-59,52	15,6	-14,65	-130,2	-1,68	164,4
37	-0,42	129,1	-57,63	-6	-18,82	-168,4	-1,73	153,9
38	-0,6	121,2	-46,51	1,1	-23,23	162,3	-1,74	143,6
39	-0,71	114,6	-45,63	-40,8	-27,11	137,4	-1,8	132
40	-0,75	106,8	-50,77	-87,7	-29,94	111,9	-1,92	121,4

**Typical on Wafer Measurements**

Bias Conditions:  $V_d=2V$ ,  $V_g=-0.2V$ ,  $I_d=400mA$

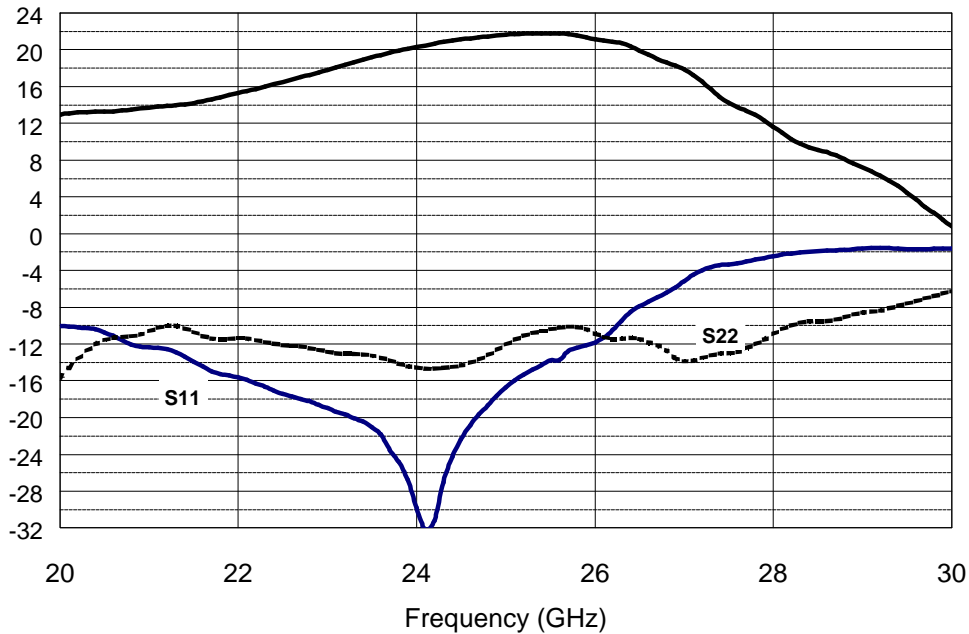
Gain & RLoss (dB)



**Typical on Jig Measurements**

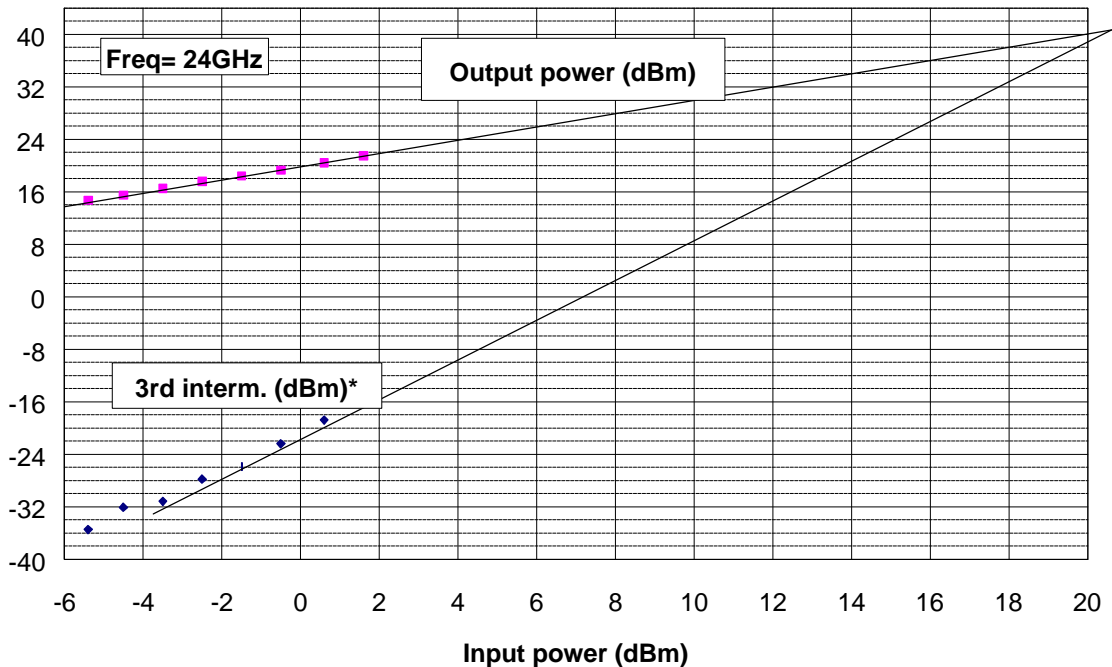
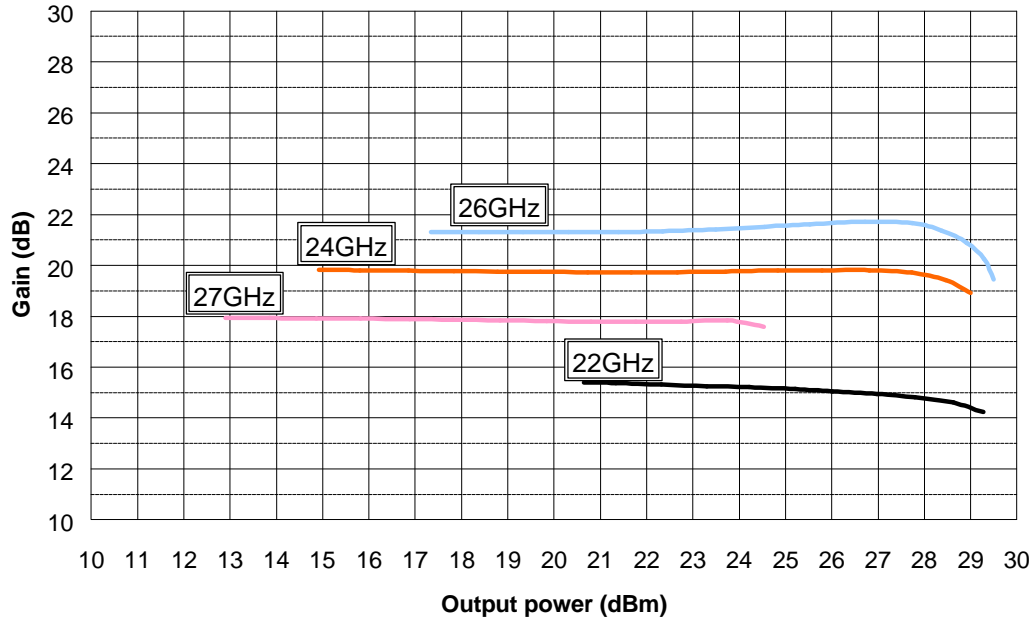
Bias conditions:  $V_d=6V$ ,  $V_g=-0.4V$ ,  $I_d=580mA$

Gain & Rloss. ( dB)



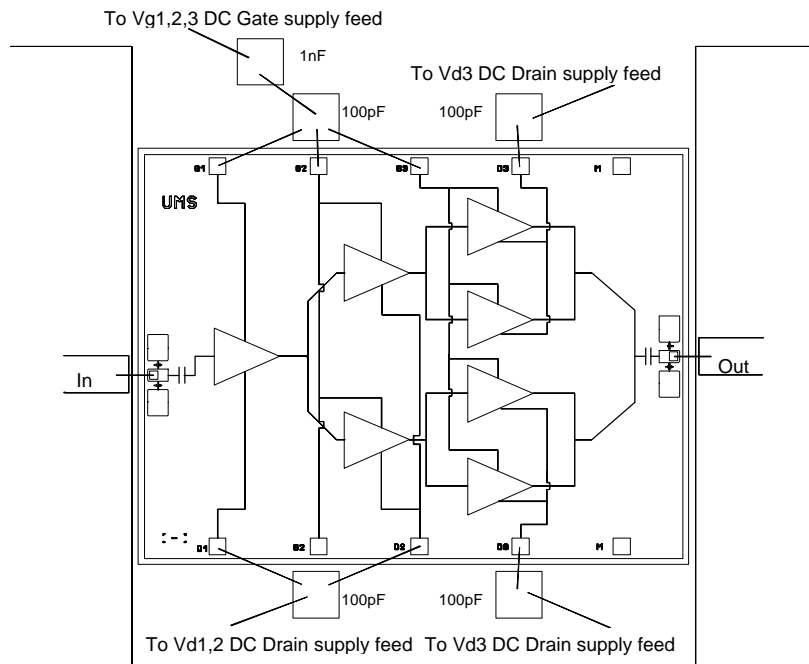
**Typical on Jig Measurements**

Bias conditions:  $V_d=6V$ ,  $V_g=-0.4V$ ,  $I_d=600mA$

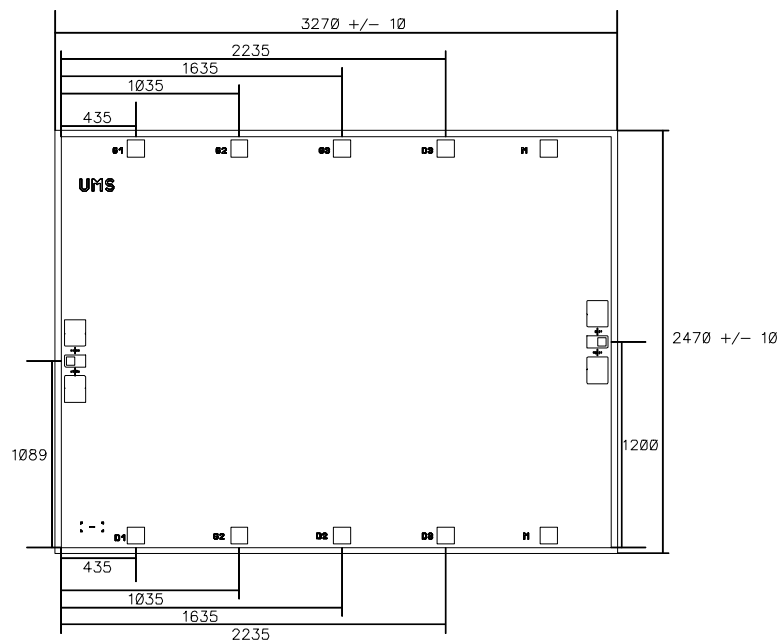


\* It is a standard 2 tones measurement with an input signal  $F_1 + F_2$ , ( $F_2 = F_1 + 10MHz$ ). The third order is measured at the  $2F_2 - F_1$  frequency.

## Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be preferred.



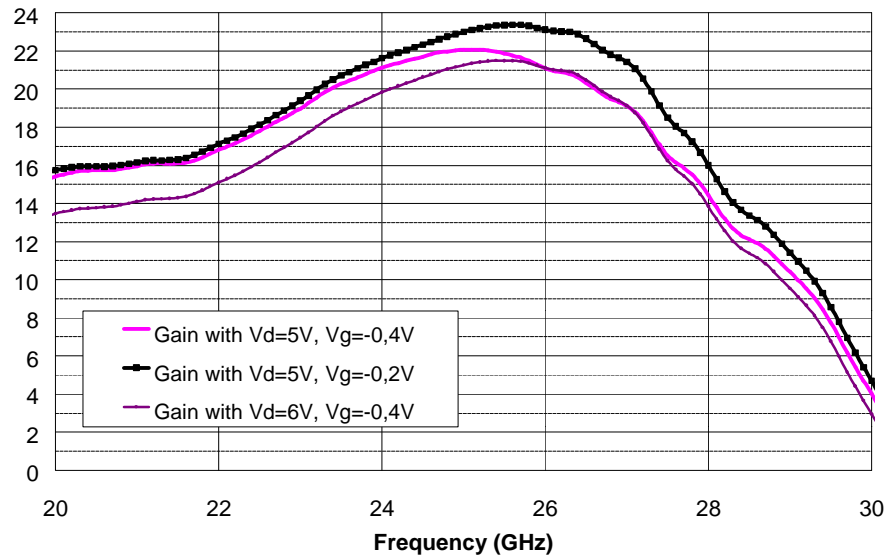
### Bonding pad positions.

( Chip thickness : 100µm. All dimensions are in micrometers )

## Application note

The given DC Bias condition in table or curves are for optimum output power. To optimize the gain a drain voltage of 5V could be apply. With this biasing point , the output power at 1dB compression decreases by around 1dBm.

The curves below show typical jig measurements versus drain & gate voltages.



## Ordering Information

Chip form : CHA5093-99F/00

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