United Monolithic Semiconductors

CHA5266-99F

10-16GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

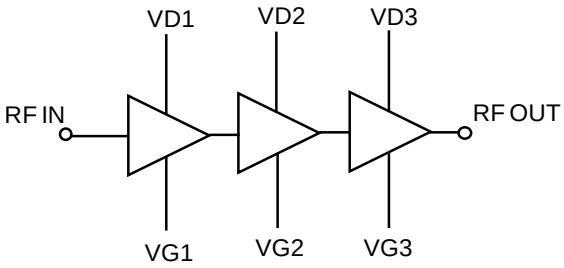
Description

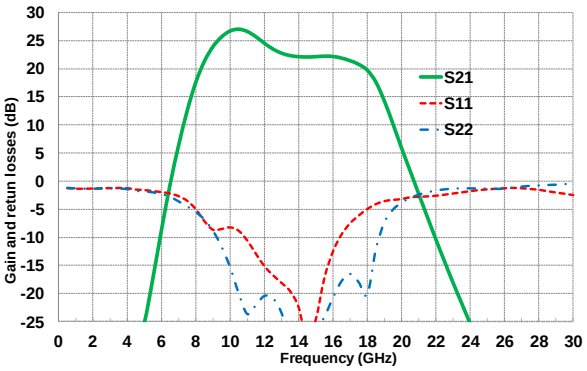
The CHA5266-99F is a three stage monolithic GaAs Medium Power Amplifier that produces 23dB linear gain and 36dBm OIP3.

It is designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.





Main Features

- Broadband performances: 10-16GHz.
- 23dB Linear Gain.
- 26.5dBm output power @ 1dB comp.
- 36dBm OIP3.
- DC bias: Vd=5.0Volt@Id=360mA.
- Chip size 1.81x1.37x0.1mm.

Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	10		16	GHz
Gain	Linear Gain		23		dB
OIP3	Output IP3		36		dBm
Pout	Output Power @1dB comp.		26.5		dBm

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
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Electrical Characteristics

Tamb.= +25°C, Vd = +5.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	10		16	GHz
Gain	Linear Gain		23		dB
RL_in	Input Return Loss		12		dB
RL_out	Output Return Loss		15		dB
P1dB	Output power @ 1dB compression		26.5		dBm
Psat	Saturated output power		27.5		dBm
OIP3	Output IP3		36		dBm
NF	Noise Figure		5.5		dB
Idq	Quiescent Drain current		360		mA
Vg	Gate Voltage		-0.35		V

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.
A bonding wire of typically 0.3nH will improve the matching at the accesses.

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	7V	V
Idq	Drain bias current	0.45	A
Vg	Gate bias voltage	-2 to 0	V
Pin	Input continuous power	20	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Ref.	Parameter	Values	Unit
Vd	VD1	DC Drain voltage 1st stage	5	V
Vd	VD2	DC Drain voltage 2nd stage	5	V
Vd	VD3	DC Drain voltage 3rd stage	5	V
Vg	VG1	DC Gate voltage 1st stage	-0.35	V
Vg	VG2	DC Gate voltage 2nd stage	-0.35	V
Vg	VG3	DC Gate voltage 3rd stage	-0.35	V

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Typical on wafer Sij parameters

Tamb.= +25°C, Vd = +5.0V, Id = 360mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
1.0	-0.9	151.4	-59.0	96.0	-70.0	-164.3	-1.0	153.4
2.0	-1.0	123.9	-49.2	-63.4	-73.7	-15.5	-1.1	126.2
3.0	-1.1	97.2	-53.2	-16.8	-73.9	-91.5	-1.3	96.7
4.0	-1.2	71.4	-45.6	40.0	-71.7	160.2	-1.4	63.1
5.0	-1.5	45.9	-25.9	94.5	-65.0	84.9	-1.6	24.4
6.0	-1.8	20.0	-6.9	46.4	-68.1	-99.9	-2.0	-18.9
7.0	-2.6	-7.7	7.3	-25.3	-72.0	-57.1	-2.9	-64.3
8.0	-4.5	-35.4	17.7	-113.2	-67.2	-16.3	-4.5	-108.8
9.0	-7.4	-51.2	24.6	145.8	-58.1	-43.7	-7.7	-152.3
10.0	-8.8	-60.8	26.3	45.3	-54.6	-63.9	-13.9	164.3
11.0	-9.6	-80.1	25.4	-35.8	-50.3	-100.1	-39.3	118.5
12.0	-10.7	-99.7	24.4	-102.5	-47.1	-128.8	-19.0	-78.8
13.0	-12.8	-139.9	23.6	-168.6	-44.3	-165.4	-17.5	-125.0
14.0	-21.4	-175.2	22.1	130.7	-44.9	168.1	-25.8	-101.1
15.0	-24.0	-53.1	20.7	74.6	-43.2	148.1	-18.4	-52.0
16.0	-13.0	-103.2	20.7	17.4	-47.8	117.2	-13.5	-68.1
17.0	-9.8	-140.8	20.7	-50.8	-43.1	127.8	-11.6	-91.6
18.0	-7.1	-178.0	19.0	-137.8	-43.3	70.2	-13.1	-54.4
19.0	-4.8	150.4	12.6	135.1	-53.6	19.7	-5.9	-73.2
20.0	-3.3	118.6	3.8	69.2	-58.0	172.1	-4.4	-94.9
21.0	-2.4	92.7	-4.7	23.6	-50.6	49.8	-3.8	-111.2
22.0	-1.9	71.4	-12.3	-19.1	-51.2	82.8	-3.6	-122.6
23.0	-1.4	52.8	-20.4	-56.1	-55.6	69.3	-3.7	-131.3
24.0	-1.1	36.2	-28.1	-89.0	-50.2	-115.7	-3.6	-138.3
25.0	-1.0	21.6	-35.8	-115.0	-51.8	-78.2	-3.4	-145.2
26.0	-1.0	8.4	-39.8	-147.1	-57.4	-133.4	-3.4	-152.8
27.0	-1.0	-3.3	-41.7	-171.5	-43.7	160.7	-3.6	-158.9
28.0	-1.0	-13.8	-43.3	139.2	-44.5	129.2	-3.7	-162.4
29.0	-1.2	-23.7	-43.1	146.5	-44.3	138.4	-3.5	-166.8
30.0	-1.3	-32.4	-38.8	129.4	-42.3	130.8	-3.3	-172.0
31.0	-1.5	-40.0	-38.3	105.2	-38.8	98.8	-3.4	-176.7
32.0	-1.6	-46.8	-38.3	79.3	-38.5	74.0	-3.4	177.7
33.0	-1.6	-52.6	-37.9	52.1	-37.8	53.6	-3.6	174.3
34.0	-1.3	-59.8	-40.6	40.3	-42.1	47.8	-3.4	171.1
35.0	-1.6	-68.1	-39.2	41.1	-39.3	45.1	-3.0	165.0
36.0	-1.9	-72.8	-42.6	-11.1	-42.8	10.2	-2.8	158.7
37.0	-1.6	-76.8	-50.9	-13.7	-45.1	-13.0	-2.6	151.0
38.0	-1.3	-84.4	-60.5	69.1	-47.6	54.2	-2.5	142.1
39.0	-1.8	-92.7	-45.0	61.5	-46.1	46.9	-2.5	132.5
40.0	-2.0	-97.8	-49.0	2.5	-45.7	24.0	-2.3	119.4

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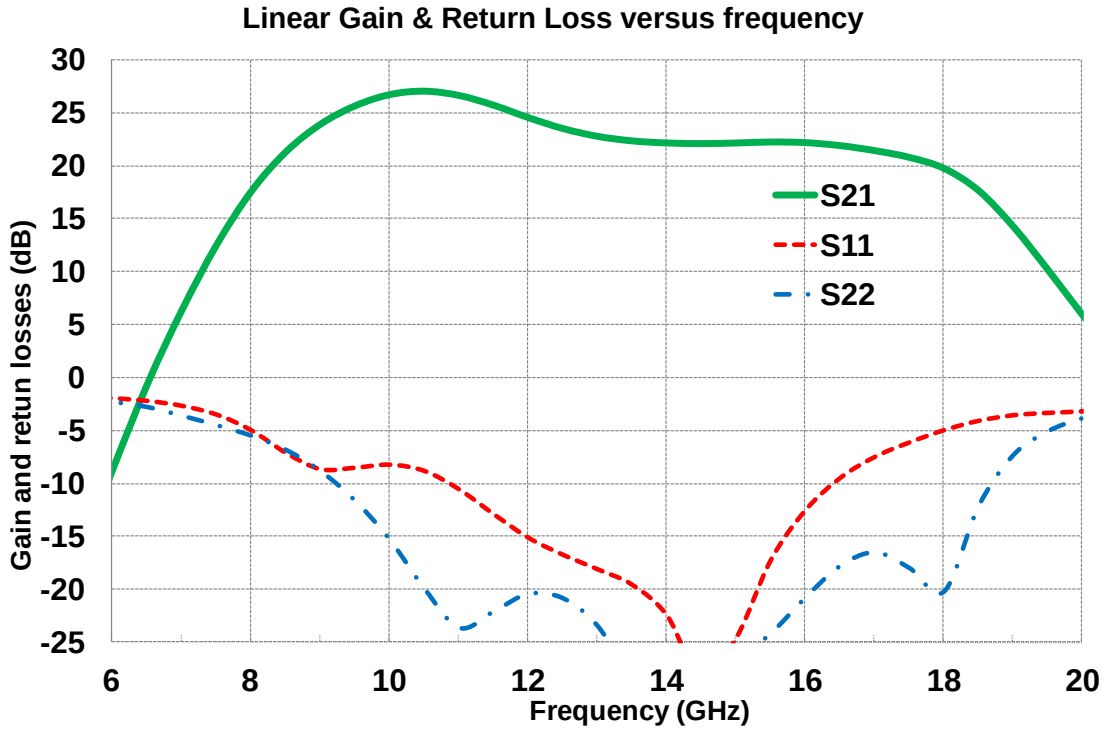
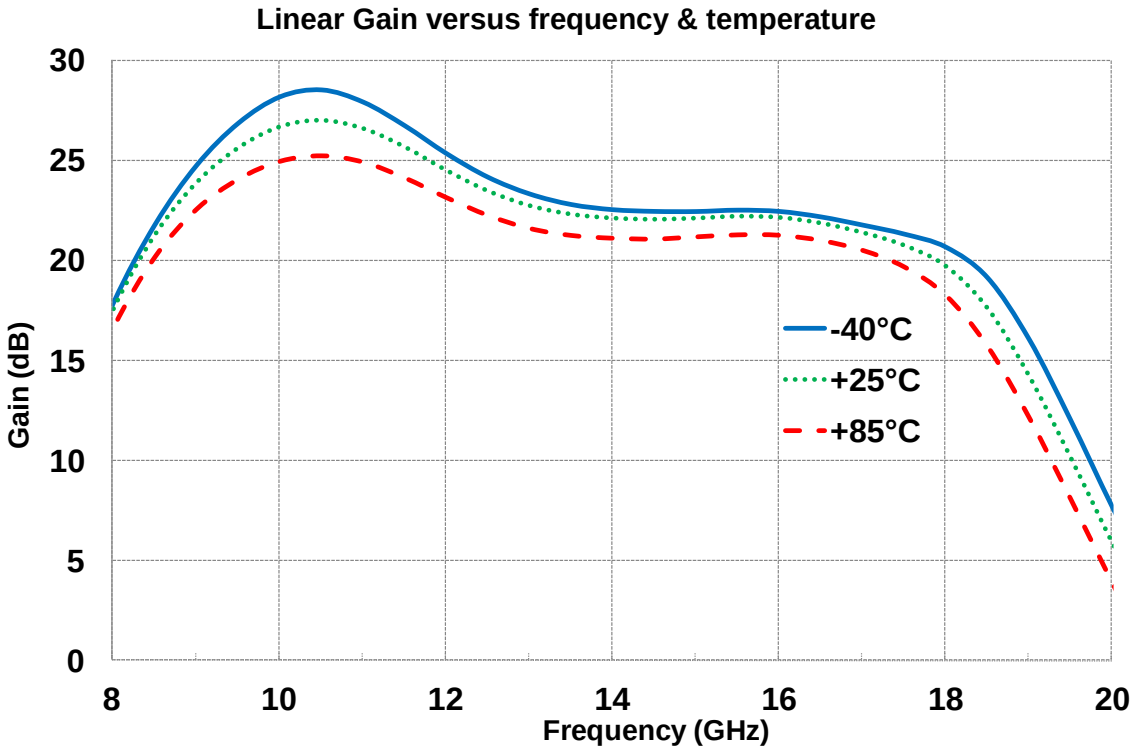
Typical test fixture Measurements

Tamb.= +25°C, Vd = +5.0V, Id = 360mA





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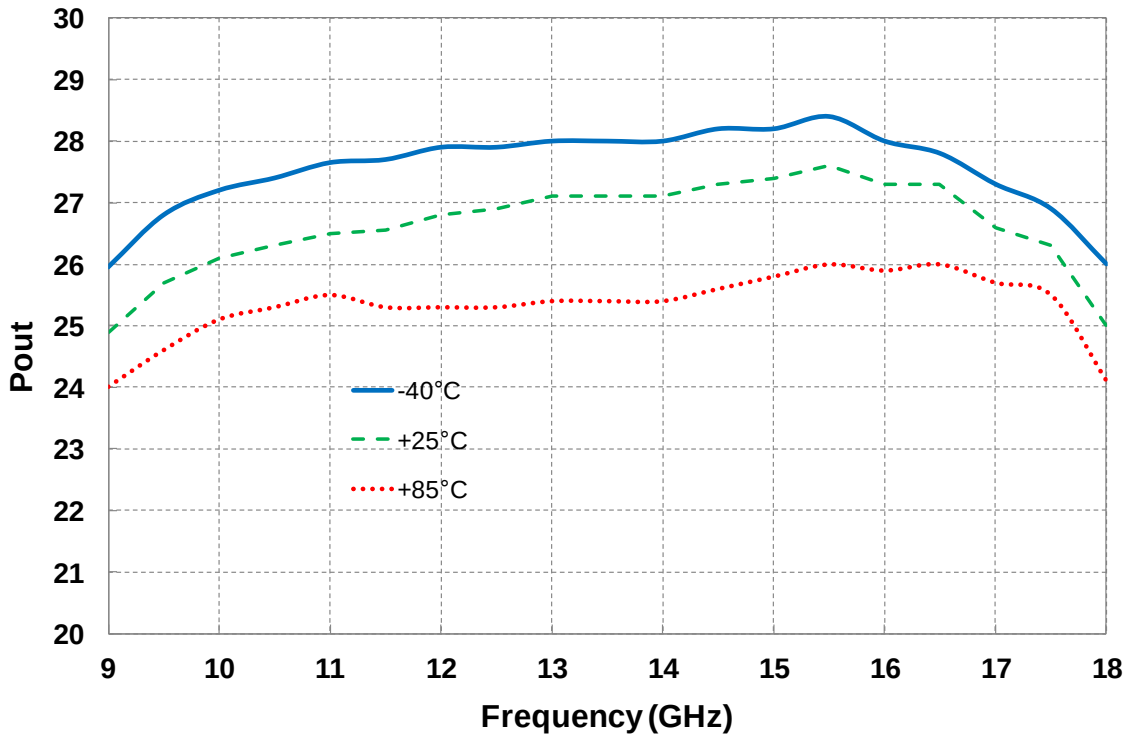
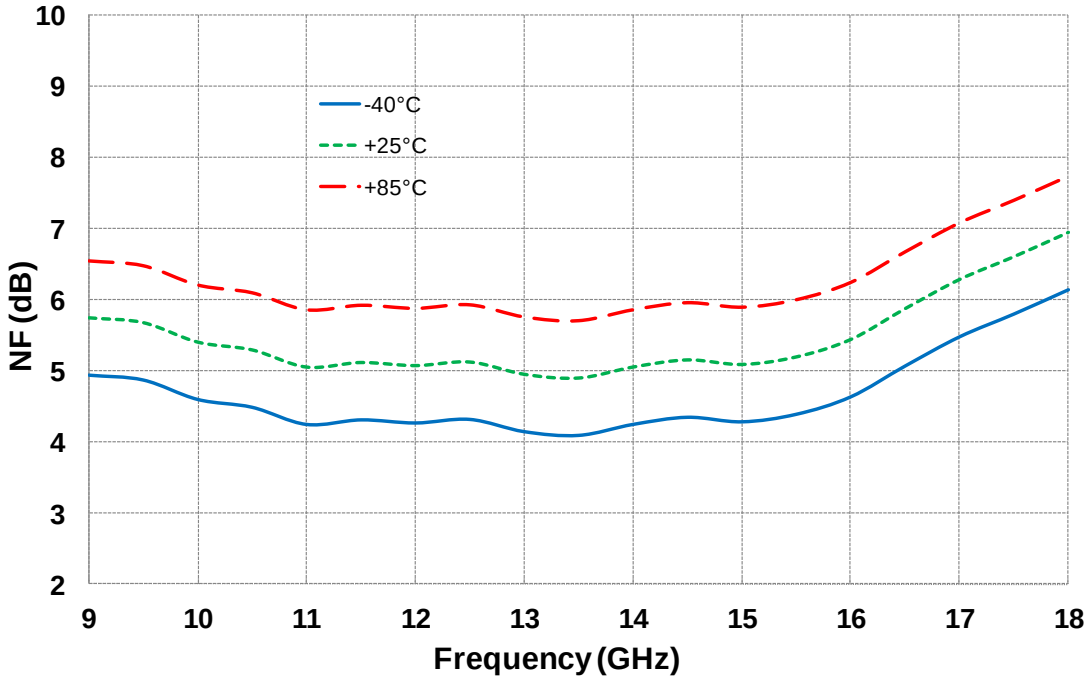
Output Power at 1dB compression versus frequency & temperature



Noise Figure versus frequency & temperature



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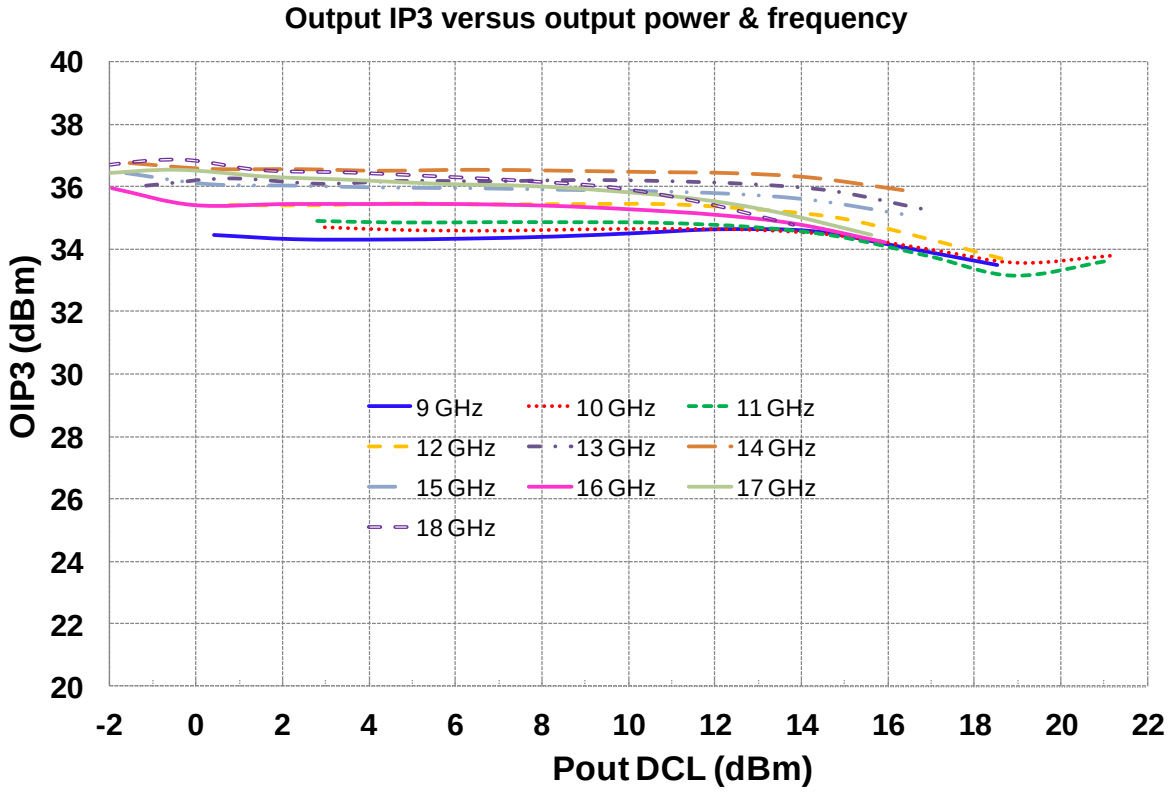

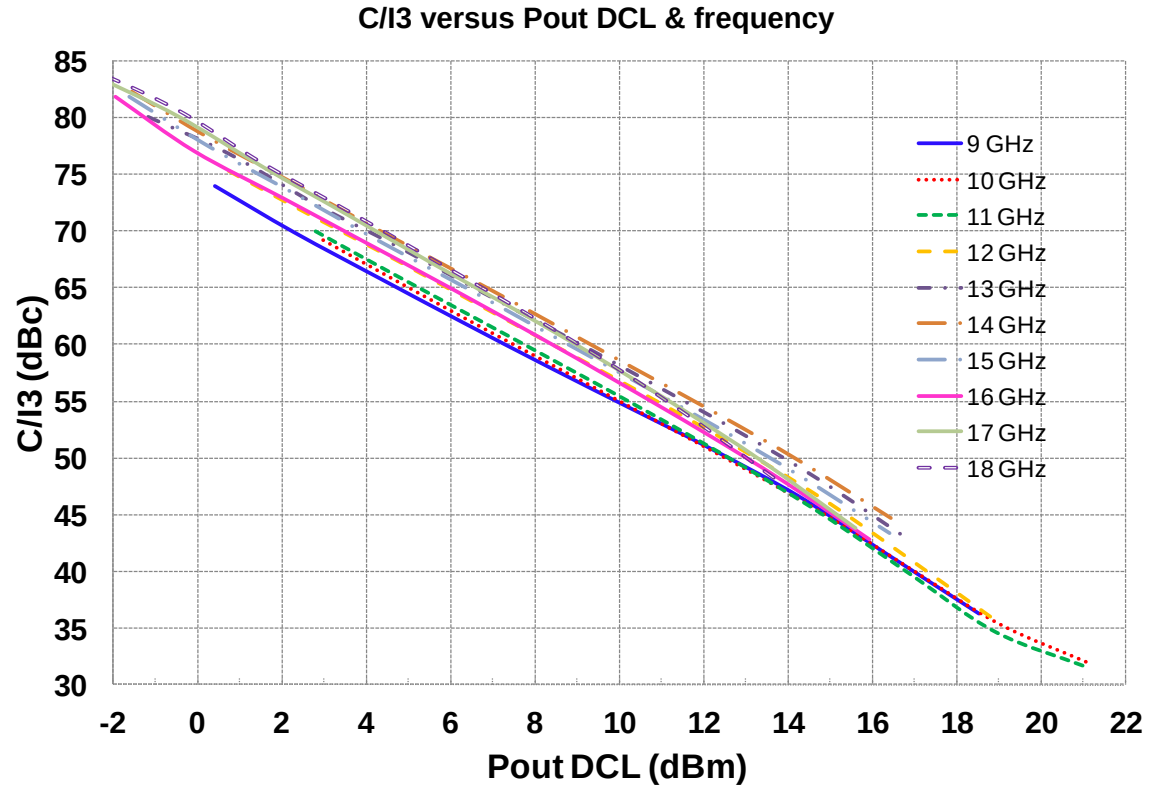

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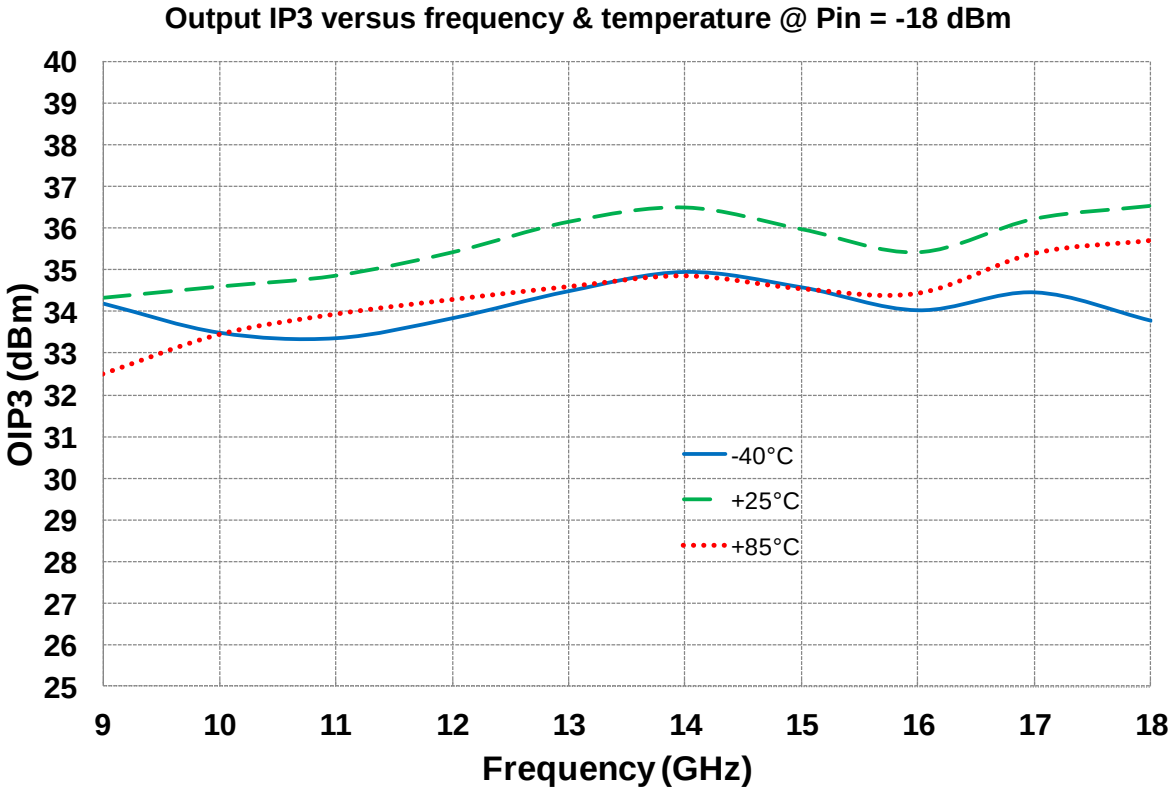
Typical Board Measurements

Vd = +5.0V, Id = 360mA



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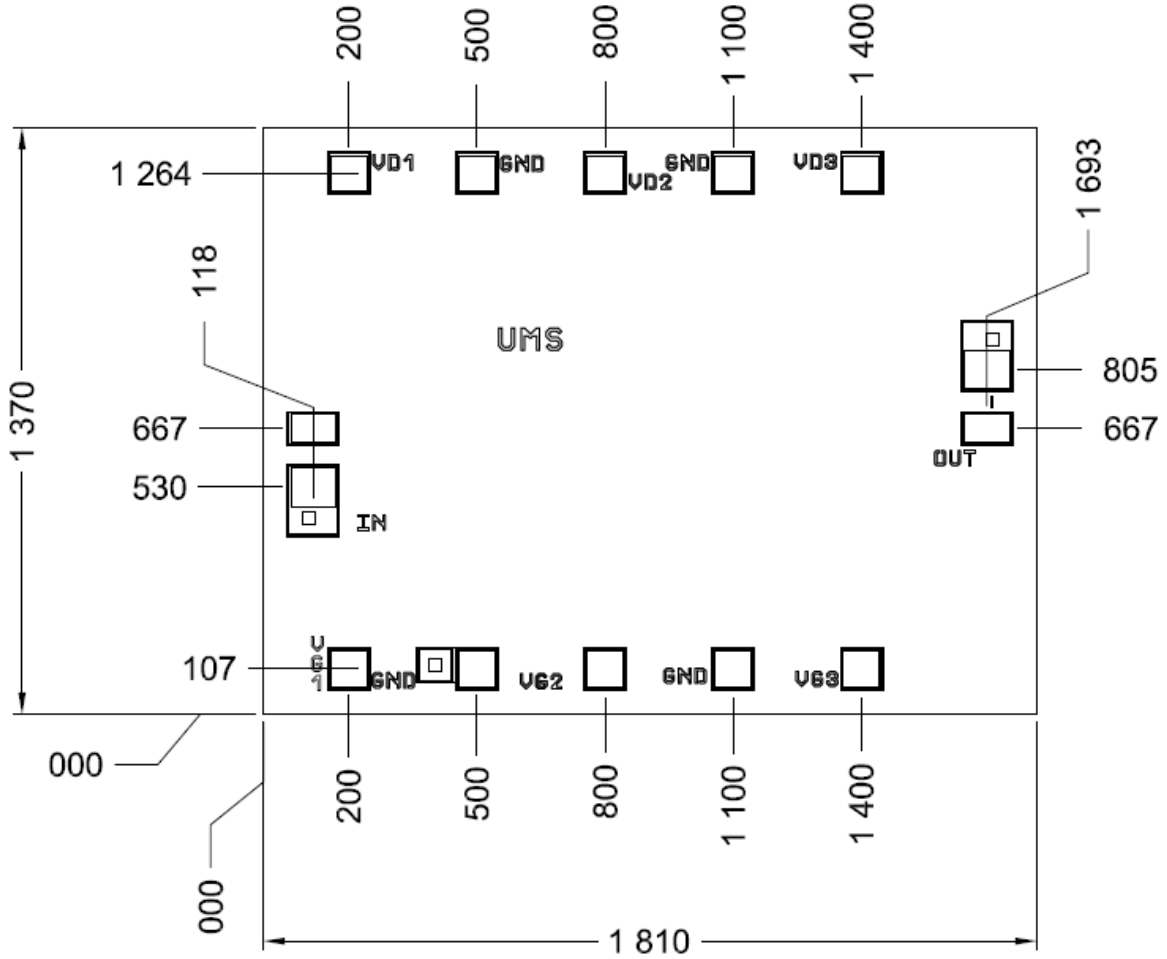
Mechanical data



All dimensions are in micrometers
Chip size = 1810x1370 ±35µm
Chip thickness = 100µm ±10µm
RF pads = 110 x 72µm²
DC pads = 100 x 100µm²
Chip width and length are given with a tolerance of ±35µm

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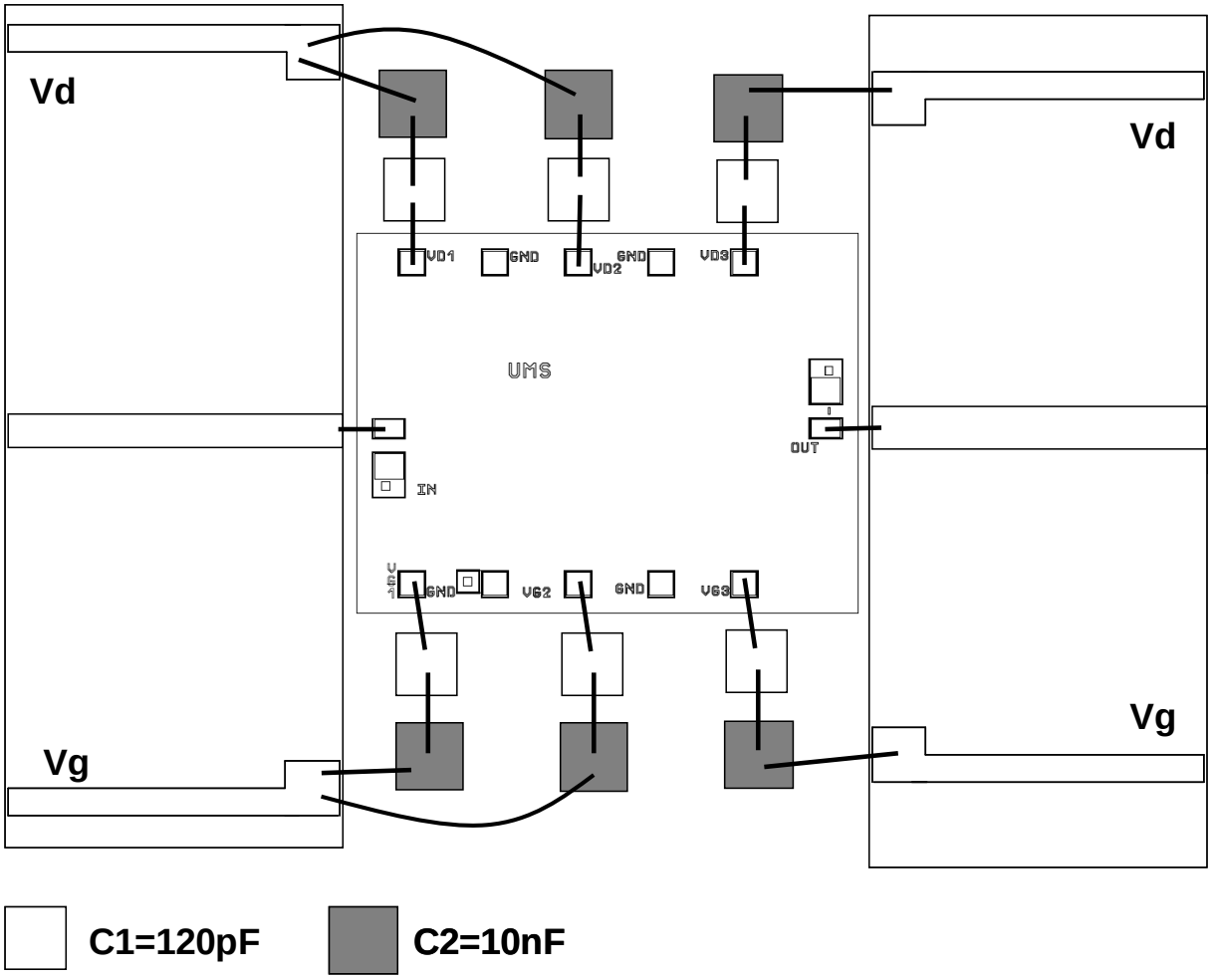
Recommended assembly plan



C1=120pF **C2=10nF**

Note:
Supply feed should be bypassed.
25µm wedge bonding is preferred.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
IN, OUT	RF	Not required	Inductance (Lbonding) = 0.3nH 400µm length with a wire diameter of 25 µm
VD1, VD2, VD3	Vd	120pF & 10nF	Drain Supply
VG1, VG2, VG3	Vg	120pF & 10nF	Gate Supply

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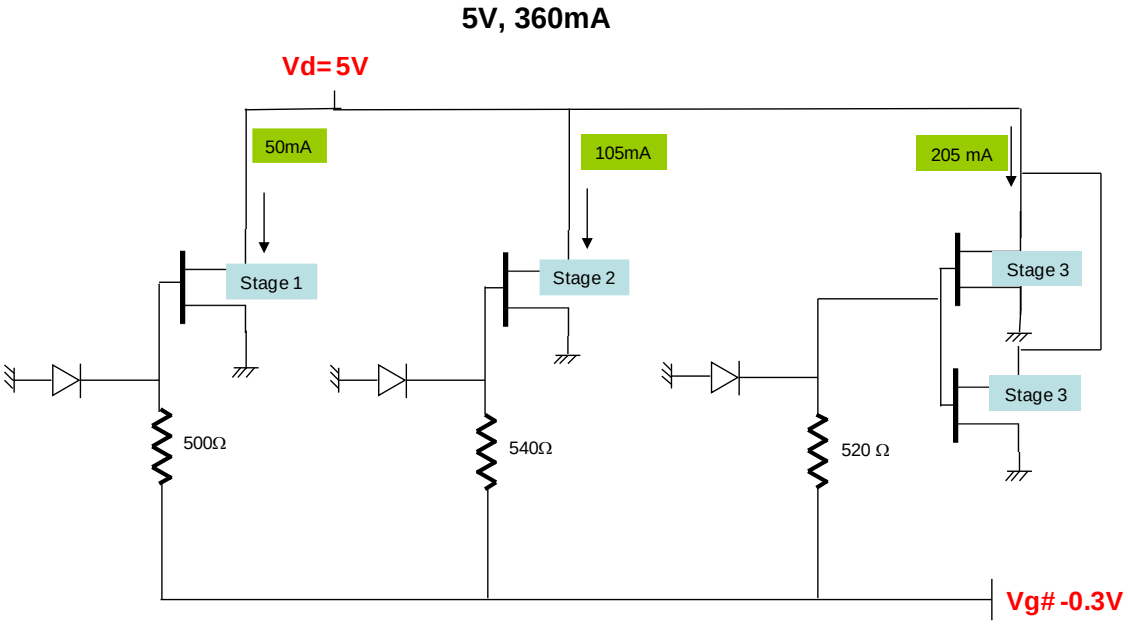
DC Schematic



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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Chip form:	CHA5266-99F/00

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